Frontiers in Heat and Mass Transfer (FHMT), 3, 043001 (2012)
DOI: 10.5098/hmt.v3.4.3001

Global Digital Central
ISSN: 2151-8629

Frontiers in Heat and Mass Transfer

Available at www.ThermalFluidsCentral.org

ADVANCED SPREADERS FOR ENHANCED COOLING OF HIGH POWER CHIPS

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ABSTRACT

Advanced spreaders for cooling a 10 x 10 mm underlying computer chip with a central hot spot (CHS) could remove > 85 W of dissipated thermal power at junctions' temperature < 100°C. The spreaders comprise a 1.6 - 3.2 mm thick Cu substrate and an 80-μm thick micro-porous copper (MPC) surface cooled by saturation nucleate boiling of PF-5060 dielectric liquid. Investigated are the effects of varying the heat flux at the chip's 1 and 4 mm^2 CHS and the impedance of thermal interface material (TIM) between the Cu substrate and underlying chip. Results confirmed the effectiveness of the MPC spreaders for cooling the chip and mitigating the effect of CHSs. With a TIM impedance of 0.19 °C-cm^2/W, the MPC spreader with a 3.2 mm-thick Cu substrate removes 90.1 W and 87.85 W for the chip with 1 and 4 mm^2 CHS when the heat flux ratio (HFR) at CHSs = 6. The chip maximum surface temperatures at the CHSs are 90.16°C and 96.6°C and the spreader's footprint areas are 25.5 and 25.25 cm^2, respectively. Decreasing the TIM impedance to 0.02°C-cm^2/W decreases the chip's maximum surface temperatures to 73.4 and 76.1°C, but slightly changes the removed thermal powers from the MPC surface to 90.3 W and 86.24W, respectively.

Keywords: *Immersion cooling nucleate boiling; dielectric liquids; central hot spot; micro-porous copper; thermal interface material; footprint area.*

1. INTRODUCTION

The continuing increases in the transistors density and modulation frequency for high power computer chips develop surface hot spots, at which the local heat flux could be as much as 1000 W/cm^2. The resulting high surface temperatures at the hot spots induce structural stresses, compromising the chip's service life and increasing its failure frequency. Thus, is it desirable to increase the removal rate of the thermal power dissipated by the chip and mitigate the effect of the surface hot spots, while maintaining acceptable junctions' temperature (≤ 85 – 125°C depending on the application, ITRS (2009)).

Nucleate boiling of dielectric liquids, such as FC-72, HFE-7100 and PF-5060, has been the subject of many investigations for potential application to immersion cooling of high power chips, Anderson and Mudawar (1989); Liu et al. (2001); Honda and Wei (2003); Lin and Banerjee (2008); El-Genk et al. (2007); El-Genk and Saber (2008); El-Genk (2012); Rainey and You (2000); Chang and You (1997). Besides their relatively low saturation temperatures (54 - 61°C at atmospheric pressure), these liquids are chemically inert, environmentally friendly and compatible with many structural materials of interest. These highly wetting liquids, however, cause an excursion in surface temperature prior to nucleate boiling incipience, El-Genk and Bostanci (2003); Jung and Kwak (2006); Parker and El-Genk (2005); Reed and Mudawar (1997). Such an excursion is undesirable because they could markedly increase the junctions' temperature of the chip.

Porous, micro-porous, macro-structured, and macro- and micro-finned surfaces and surfaces with micro-porous coatings have been shown to enhance nucleate boiling of dielectric liquids, Reed and Mudawar (1997), Chang and You (1997); Launay et al. (2006); Liu et al. (2001); El-Genk and Parker (2005); Ferjančič et al. (2006); El-Genk and Ali (2010). The measured enhancements in the nucleate boiling heat transfer coefficient on these surfaces, compared to plane Cu, have been attributed to increases in the surface density of active sites for bubbles nucleation. Some of these surfaces have been shown to either eliminate or markedly reduce the excursion in surface temperature prior to nucleate boiling incipience.

Recent experiments by the authors investigated nucleate boiling of PF-5060 dielectric liquid on micro-porous copper (MPC) surfaces of different thicknesses (80 - 197 μm). These surfaces are deposited using electrochemical processes on 10 x 10 mm and 1.68 mm-thick Cu substrates, El-Genk and Ali (2010); Shin and Liu (2004); Shin et al. (2003). Pool boiling experiments using these MPC surfaces demonstrated significant enhancements in the saturation nucleate boiling heat transfer coefficient for PF-5060 dielectric liquid, and either a decrease (≤ 15 °C) (Fig.2) or elimination of temperature excursions.

Figure 1 presents Scanning Electron Microscope (SEM) images of the 80-μm thick MPC surface, El-Genk and Ali (2010). They show patterned round and shallow depressions surrounded by dense structure of Cu micro-particles and clusters, ranging in sizes from a faction of a micron to a few microns. The Cu micro-particles and clusters are also present on the inside of the round depressions. These depressions increase the effective wetted surface area for nucleate boiling and the porous copper micro-structure increases the density of the active sites for bubbles nucleation. The combined contribution enhances nucleate boiling heat transfer on the MPC surfaces, El-Genk and Ali (2010).

Recent numerical analysis performed to investigate the application of nucleate boiling of PF-5060 dielectric liquid on MPC surfaces to immersion cooling of high power computer chips using MPC spreaders. The spreaders comprise a Cu substrate (1.6 – 3.2 mm thick) and 80-μm thick MPC surface layer, Ali and El-Genk (2012a and 2012b), cooled by saturation nucleate boiling of PF-5060 dielectric liquid. The MPC

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ISSN: 2151-8629

spreaders take advantage of the nucleate boiling enhancement on the MPC surface and the good heat spreading through the Cu substrates. The numerical analysis of Ali and El-Genk (2012a and 2012b) did not directly incorporate the effect of the TIM resistance between the Cu substrate and the underling chip, but used the values of the measured experimental values of the nucleate boiling heat transfer coefficient, h_{NB}, for PF-5060 liquid on 80-µm thick MPC (Fig. 2), El-Genk and Ali (2010). The pool boiling experiments are performed by controlling and incrementally increasing the input power and recording the surface heat flux and temperature after reaching steady state. Details of the experiments setup and conduct could be found elsewhere, El-Genk and Bostanci (2003); Parker and El-Genk (2005); Ali and El-Genk (2010).

1.1 Objectives

This paper extends the recent numerical analysis of Ali and El-Genk (2012a and 2012b) by investigating the effects of changing the TIM impedance and the local heat flux at the chip's 1 and 4 mm^2 central hot spot (CHS) on the performance of the MPC spreaders. The present numerical analysis uses TIM impedance of 0.02 and 0.19°C-cm^2/W and varies the ratio of the heat flux at the CHS to that of the chip's surface average outside the hot spot (HFR) from unity (uniform heat dissipation) to 6. These analysis parameters are for the purpose of quantifying their effects and do not necessarily represent specific actual applications.

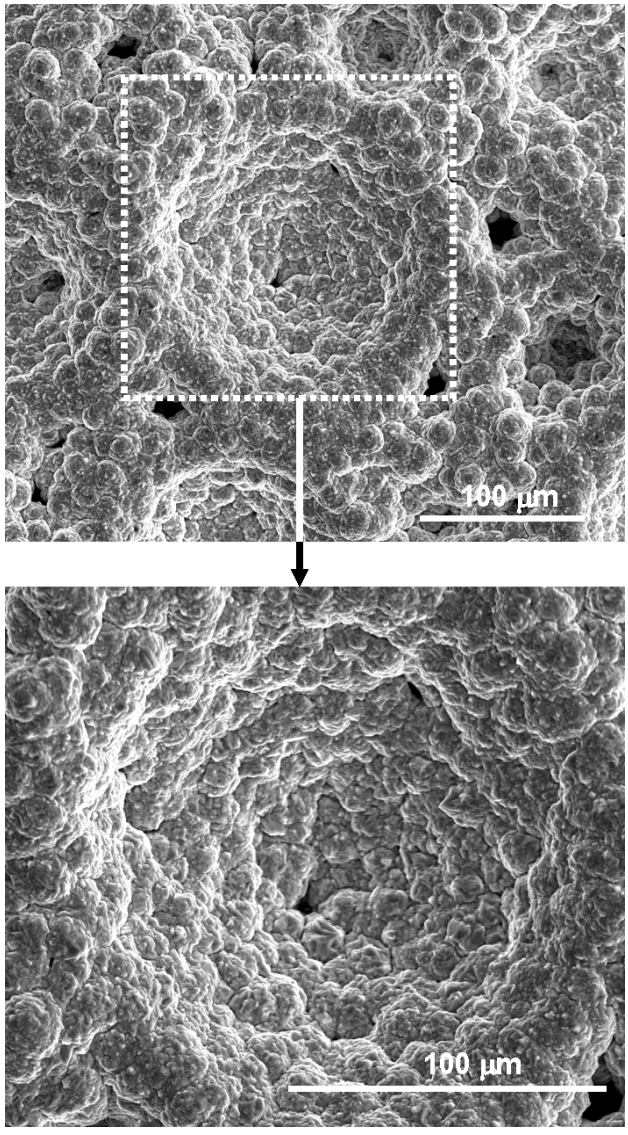

Fig. 1 SEM Images of the 80-µm thick MPC Surface.

In the present numerical analysis, the calculated results include: (a) the total thermal power dissipated by the underlying chip and removed by the MPC spreaders; (b) the footprint area and the total thermal resistance of the spreaders; (c) the spatial temperature distributions at the chip and the spreaders' surfaces, and (d) the individual thermal resistances for heat spreading by the Cu substrates, heat conduction in the MPC surface layer saturated with dielectric liquid, and saturation nucleate boiling on the MPC surface of the spreaders. The results are also compared to those calculated for plane Cu spreaders of the same thicknesses as the Cu substrates of the MPC spreaders. The next section presents and discusses the experimental saturation pool boiling curves obtained by the authors for PF-5060 dielectric liquid on the 80-µm thick MPC and on plane Cu surfaces of the same footprint dimensions (10 x 10 mm) at 0.085 MPa.

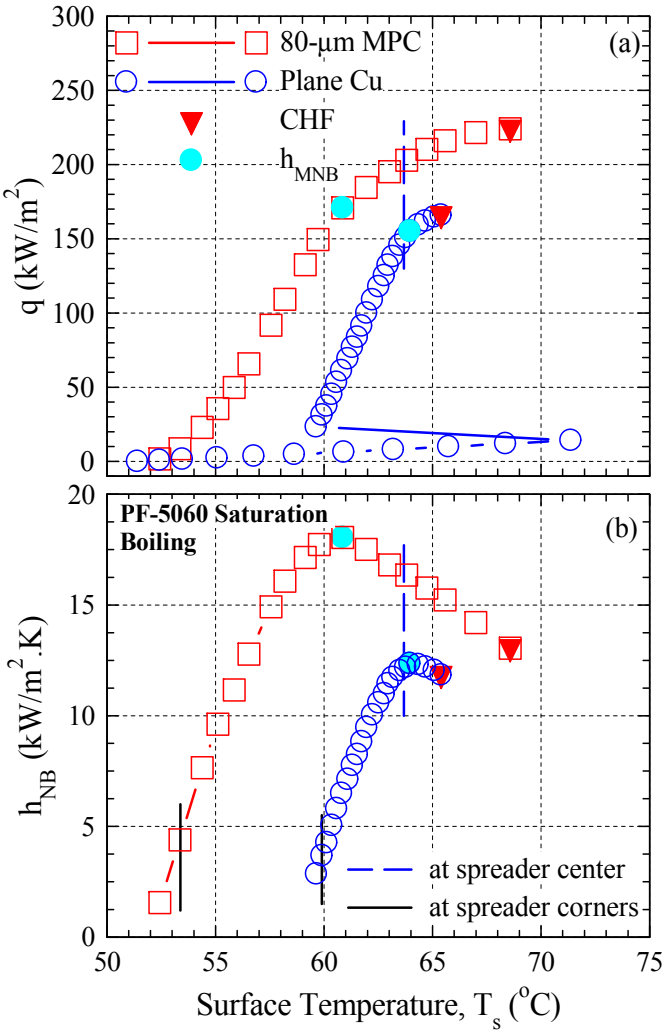

Fig. 2 Saturation pool boiling and h_{NB} curves for PF-5060 dielectric liquid at 0.085 MPa on an 80-µm thick MPC and plane Cu surfaces, El-Genk and Ali (2010).

2. NUCLEATE POOL BOILING CURVES

The experimentally obtained saturation boiling curves of PF-5060 dielectric liquid on the 80-µm thick MPC and plane Cu surfaces are compared in Fig. 2a. The MPC surface is deposited on a 10 x10 mm and 1.6 mm-thick Cu substrate and plane Cu surface of the same footprint dimensions is prepared with 1500 emery paper. The pool boiling experiments with PF-5060 dielectric liquid are performed in our laboratory at the University of New Mexico in Albuquerque, New Mexico, where the local elevation is ~ 1700 m (ambient pressure ~

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0.085 MPa). At this elevation, the saturation temperature of PF-5060 liquid (51.4°C) is lower than at sea level or 0.1 MPa (54°C), 3M (2012). The experimental boiling curves in Fig. 2a are used to determine those of the nucleate boiling heat transfer coefficient, h_{NB} (Fig. 2b).

The filled triangle symbols in Figs. 2a and 2b indicate the Critical Heat Flux (CHF) and the filled circle symbols indicate the maximum nucleate boiling heat transfer coefficient, h_{MNB}. CHF, caused by the departure from nucleate boiling, is typically associated with a large surge in surface temperature and the transition to film boiling. Thus, CHF is an operation limit to avoid in practical and industrial applications in which the maximum design heat flux is typically kept at 50 – 90% of CHF.

The values of h_{NB} in Fig. 2b increase with increased input power in the experiments due to the increase in the density of the active sites for bubbles nucleation on the MPC and plane Cu surfaces. At h_{MNB}, near the end of the fully developed nucleate boiling regime (Fig. 2a), all potential sites for bubbles nucleation become active, with little bubbles coalescence at or near the surface. Thus, h_{MNB} is much higher than that at CHF and the corresponding surface temperature is much lower (Figs. 2b). Beyond h_{MNB}, increasing input power promotes lateral coalescence of growing and rising bubbles at and near the heated surface. The added thermal resistance increases the surface temperature and decreases the value of h_{NB}, until reaching CHF (Fig. 2b).

The saturation boiling experimental curves in Figs. 2a and 2b demonstrate the enhancement in nucleate boiling of PF-5060 dielectric liquid on the 80-µm thick MPC surface (Fig. 1), compared to that on plane Cu. The values of h_{MNB} and CHF on the MPC surface (Fig. 1) are 18.1 and 224.1 kW/m^2 and occur at surface temperatures of 60.86°C and 68.6°C (Fig. 2a). On plane Cu, however, the values of h_{MNB} and CHF are 12.36 and 165.83 kW/m^2 and the corresponding surface temperatures are 64°C and 65.4°C. Fig. 2a also shows a 20°C excursion in surface temperature prior to the incipience of nucleate boiling on plane Cu. By contrast, the excursion in surface temperature on the MPC is nil. At CHF, h_{NB} for saturation boiling of PF-5060 liquid on the 80-µm thick MPC surface is ~13 kW/m^2 K; ~72% of h_{MNB} (18.1 kW/m^2 K) and occurs at a 7.74°C higher surface temperature than at h_{MNB} (~68.6 °C). The MPC surface temperature at h_{MNB} is 60.86°C (Fig. 2b). For immersion nucleate boiling cooling applications, it is desirable to operate at or near h_{MNB}. On the left side of the h_{NB} curves (Fig. 2b), the lower surface temperatures help decreasing the junctions' temperature of the underlying chip.

The saturation nucleate boiling heat coefficient curves for PF-5060 liquid in Fig. 2b are used in the present numerical thermal analyses of the MPC and the plane Cu spreaders for cooling a 10 x 10 mm chip with 1 and 4 mm^2 CHS (Fig. 3). The MPC spreaders comprise a 1.6, 2.4 or 3.2-mm thick Cu substrate and an 80-µm-thick MPC surface (Fig. 3) and the plane Cu spreaders have the same thicknesses as the Cu substrates of the MPC spreaders. The next section describes the problem statement and the boundary conditions used in the performed 3-D numerical thermal analyses of these spreaders.

Table 1. THERMFLOW^{TM}T558 phase-change, 25.4 µm thick polymer foils TIM, Thermflow (2012).

Thermal impedance @70°C (°C-cm^2/W)	Applied pressure (kPa)	Melting point (°C)
0.190	69	45
0.020	172	
0.013	345	

3. PROBLEM STATEMENT AND CONDITIONS

The MPC spreader is t_{sp} thick (Fig. 3a) and the 10 x 10 mm chip centered below the spreader, L_{sp} x L_{sp} (Fig. 3b), has either a 1 or 4 mm^2 square CHS. Saturation nucleation boiling of PF-5060 dielectric liquid cools the MPC surface of the spreader. The Cu substrate, t_{cu}, is either1.6, 2.4 or 3.2 mm-thick and that of the MPC surface layer, t_{MPC}, is 80 µm thick. The effective thickness and the thermal impedance of the TIM between the Cu substrate and underlying chip, TI_{TIM}, depend on the applied pressure (Table 1).

The THERMFLOW^{TM} T558 TIM used in the numerical analysis is a phase-change, electrically nonconductive, and thermally enhanced polymer for high power chips and electronic packaging applications, Thermflow (2012). This solid material at room temperature becomes soft at high temperatures (> 45°C), and conforms to the matting surfaces of the interface with a light clamping pressure. The impedance of TIM is 0.19°C-cm^2/W at a clamping pressure of 69 kPa and 70°C and 0.02°C-cm^2/W at a 172 kPa clamping pressure, Thermflow (2012). For a conservative consideration, the base-case numerical analyses of the MPC and plane Cu spreaders use TIM impedance of 0.19°C-cm^2/W. The effect of decreasing this impedance to 0.02°C-cm^2/W on the spreaders' performance is also investigated.

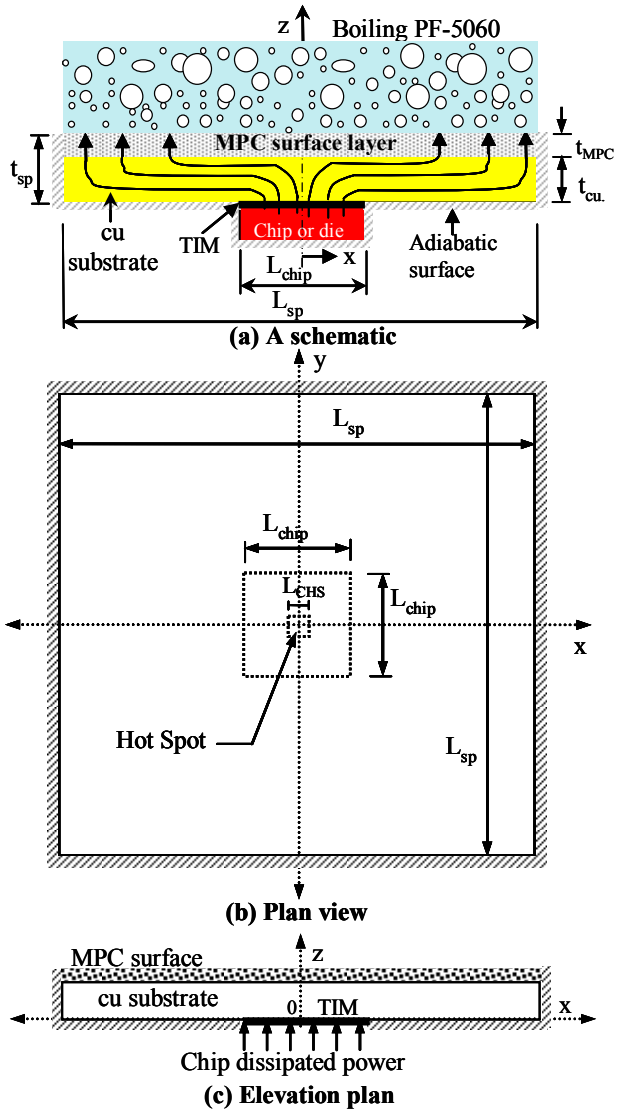

Fig. 3 A Schematic and a cross-sectional view of the MPC spreader.

In addition to the dimensions of the spreaders' footprints, the numerical analyses calculate the thermal powers removed by the spreaders and the spatial temperature distributions at their surfaces and the surface of the underlying chip. The calculated results also include the individual thermal resistances for the heat spreading in the Cu substrate, heat conduction in the MPC layer, and saturation boiling of the PF-5060 dielectric liquid. The total thermal resistances of the MPC

spreaders, R_{TOT}, are the sum of these three thermal resistances plus that of the TIM, R_{TIM}. For the plane Cu spreaders, the total thermal resistances are the sum of those of the TIM, heat spreading, and saturation boiling.

Although the heat removed from the sides and bottom of the spreaders could partially contribute to cooling the underling chip, conservatively the present numerical analyses assume these surfaces adiabatic (Figs. 3a - 3c). In practical applications, the heat transfer coefficients at these surfaces, likely by forced convection of air, are not well characterized. Thus, the calculated values of the removed thermal powers by the MPC and plane Cu spreaders in the present analyses would be lower and the corresponding chip maximum surface temperatures would be higher than in actual applications.

The thermal conductivity of Cu (400 W/m K), the effective thermal conductivity of the 80-μm thick MPC surface layer saturated with PF-5060 liquid (~191.63 W/m K) and the thermal conductance of TIM, Thermflow (2012), are specified in the input to the numerical thermal analyses of the MPC spreaders. The effective thermal conductivity of the 80-μm thick MPC surface layer is calculated in terms of its effective volume porosity (0.521) and the thermal conductivities of Cu and the PF-5060 dielectric liquid, El-Genk and Ali (2010); 3M (2012).

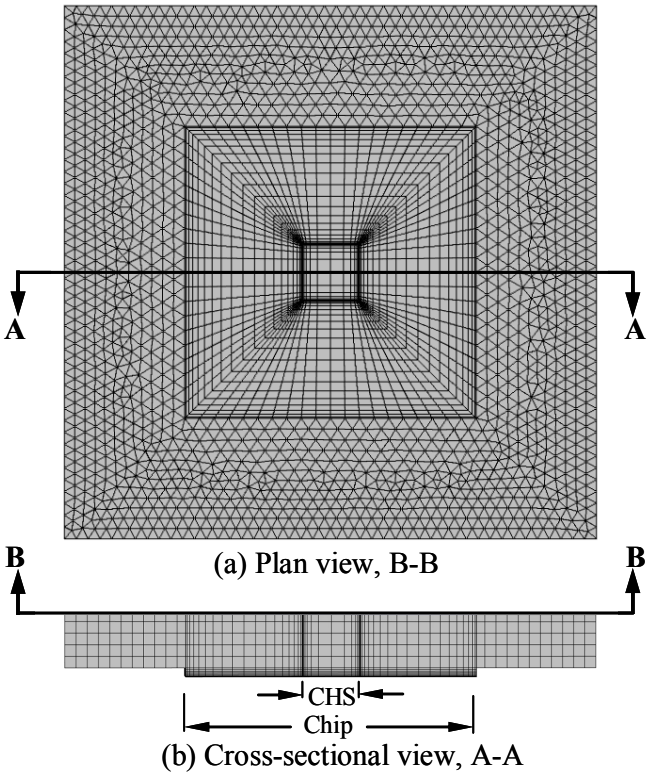

Fig. 4 Numerical mesh grid used in the present numerical thermal analyses of the Spreaders.

The thermal powers removed from the spreaders' surfaces by saturation boiling of PF-5060 and the spreaders' footprint areas are calculated, subject to the following limits: (a) h_{NB} at the center of the spreader surface is that determined in the pool boiling experiments of El-Genk and Ali (2010) at 90% of CHF (Fig. 2b) and (b) h_{NB} at the corners of the spreader top surface is that measured in the pool boiling experiments at a 1^oC higher surface temperature than that at incipient boiling (Fig. 2b). The local heat flux at the CHS of the underlying chip is assumed uniform, but varied from 2 - 6 times the average surface heat flux of the chip outside the hot spot. For comparison, numerical thermal analyses are also performed for an underling chip without a CHS (uniform heat dissipation or HFR = 1). The steady-state numerical thermal analyses of the MPC spreaders (Fig. 3) involve 3-D conduction (x,y,z) in the Cu substrate and in the 80-μm MPC surface layer. However, the results showed that heat conduction in the MPC surface layer is effectively one-dimensional (Fig. 3a). This is because the effective thermal conductance of this thin layer, saturated with PF-5060 liquid (2.39×10^6 W/m^2 K), is higher than that of the 1.6 - 3.2 mm thick Cu substrate (1.25×10^5 - 2.5×10^5 W/m^2 K).

The 3-D numerical analyses of the MPC and plane Cu spreaders (Fig. 3) are performed using the commercial software, COMSOL multi-physics version 4.0a, COMSOL MULTIPHYSICS (2010). This finite elements software solves the steady-state heat conduction in the Cu substrate and the MPC surface layer using a stationary iterative solver with a generalized minimum residual algorithm (GMRES). With an implemented tolerance of 1.0×10^{-4}, the fine numerical mesh grid ensures the solution convergence and the accuracy of the results.

The implemented numerical meshing in thermal analyses of the MPC and plan Cu spreaders is shown in Fig. 4. The implemented numerical grid comprises quadrilateral mesh elements in the 10 x 10 mm central section of the spreader, directly above the underlying chip, and hexahedral elements in the rest of the spreader. Figure 4a shows the applied numerical mesh grid elements at the surface of the spreader. The cross-sectional view in Fig. 4b shows the numerical grid used in the Cu substrate and the MPC surface layer. The total number of mesh grid elements used in the thermal analyses of the MPC spreader increases as the thickness of the Cu substrate increases. A total of 45,000 elements are used in the numerical thermal analysis of the MPC spreader with a 1.6-mm thick Cu substrate and as much as 350,000 elements for the MPC spreader with a 3.2-mm thick Cu substrate.

The thermal analyses of the MPC and the plane Cu spreaders are carried out using iterative procedures. First, initial values of the spreader's footprint dimensions and the dissipated thermal power by the underlying chip are assumed. These values changed incrementally until the values of the h_{NB} at the center of the spreader surface equals that corresponding to 90% of CHF (Fig. 2b). Then, the numerical thermal analyses continue to incrementally increase the values of both the dissipated power by the underlying chip and the footprint dimensions of the spreader until also h_{NB} at the corners of the spreader surface equals that corresponding to a 1^oC higher surface temperature than measured in the boiling experiments at incipient boiling (Fig. 2b). When both desired values of h_{NB} at the center and the corners of the spreader are reached and a convergence of the numerical solution is achieved, the calculations are terminated. Calculations are also performed using only a quarter of the spreader with symmetry boundary conditions without a change in the numerical results. A typical case took ~ 10 minutes on a recent personal computer to complete.

The accuracy of numerical calculations is verified by examining the error in the overall energy balance calculations. With a solver tolerance of 1.0×10^{-4}, the error in the overall energy balance is ~ 0.1%. To examine the sensitivity of the numerical solution convergence and the accuracy of the results to the number of numerical mesh elements used in the numerical analysis, calculations are repeated using a finer numerical grid of 600,000 elements. There were insignificant changes in the solution convergence and the calculated results.

4. RESULTS AND DISCUSSION

The performed thermal analyses of the MPC and plane Cu spreaders are for steady-state condition. They calculate the spreaders' footprint areas and thermal powers removed; the temperature distributions at the surface of the spreaders and that of the underlying chip; the chip maximum temperature at CHS and the individual thermal resistances for heat spreading in Cu substrates, heat conduction in TIM and the MPC surface layer, and saturation nucleate boiling at the top surface of the spreaders. The analyses varied the values of: (a) the CHS area (1 and 4 mm^2) and local heat flux ratio, HFR, from 1 - 6 and (b) the thickness of the Cu substrate (1.6, 2.4 and 3.2 mm), and the thermal impedance of TIM.. The performance results of the spreaders with a

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TI_{TIM} = 0.19°C-cm^2/W are presented in Figs. 5 – 12 and those in Figs. 13 -17 show the effect of using smaller TIM impedance of 0.02 °C-cm^2/W.

4.1 Thermal Power Removed

The results for HFR = 2 and 6, CHS areas of 1 and 4 mm^2 and Cu substrate thicknesses of 1.6 and 3.2 mm are compared in Figs. 5a – 5d. Increasing the thickness of the Cu substrate increases the removed thermal power by and the footprint area of the MPC spreaders. Conversely, increasing HFR at CHSs slightly decreases the thermal powers removed from the spreaders' surfaces and their footprint areas. These effects are more pronounced for the underlying chip with 4.0 mm^2 CHS and HFR = 6 (Figs. 5b and 5d). The total thermal powers removed and the footprint areas of the plane Cu spreaders are significantly smaller than those of the MPC spreaders (Figs. 5a – 5d).

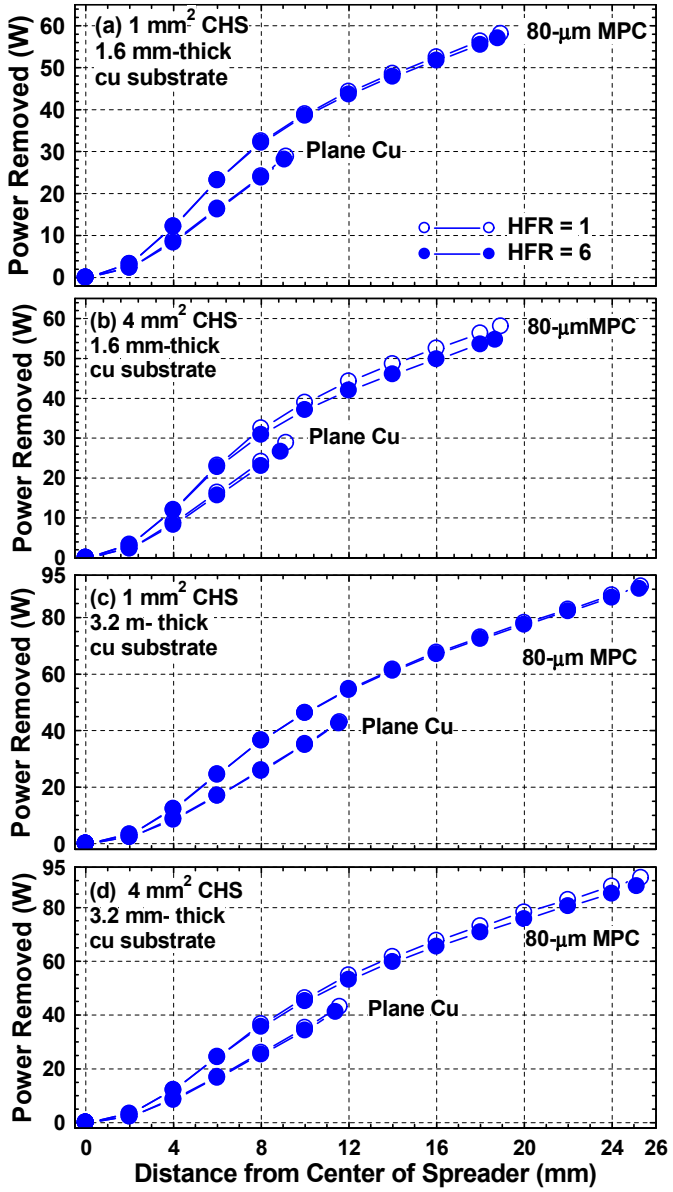


Fig. 5 Comparisons of the thermal powers removed using MPC and plane Cu spreaders.

A measure of spreader performance is the ratio of its thickness to width, t_{sp}/L_{sp}; the smaller the ratio the higher the spreader performance. The ratios of 0.0444 (Fig. 5a) and 0.0653 (Fig. 5d) for MPC (or *composite*) spreaders with 1.6 and 3.2 mm thick Cu substrates, respectively, are less than half those for plane Cu spreaders of the same thicknesses as the Cu substrates of MPC spreaders; 0.098 and 0.1474, respectively.

The MPC spreader with a 1.6 mm thick Cu substrate has a footprint area of 14.14 cm^2 and removes 56.95 W for the underlying chip with a 1 mm^2 CHS when HFR = 6(Fig. 5a). With no CHS (or uniform heat dissipation by the underlying chip (HFR = 1) these values are 14.33 cm^2 and 58.05 W, respectively. The values for the plane Cu spreader that is 1.6 mm thick are only 3.29 cm^2 and 28.1 W for the chip with 1 mm^2 CHS when HFR = 6 and 3.35 cm^2 and 28.78 W when there is no CHS (HFR = 1) (Fig. 5a).

For the MPC spreader with a 1.6 mm thick Cu substrate, increasing the CHS area from 1 to 4 mm^2, while keeping HFR = 6, slightly decreases the thermal power removed to 54.7 W and the spreader's footprint area to 13.95 cm^2 (Fig. 5b). When HFR = 6 and the CHS area is 1 and 4 mm^2, the MPC spreaders with 3.2-mm thick Cu substrate have larger footprint areas of 25.5 and 25.25 cm^2 and remove as much as 90.1 W and 87.85 W, respectively (Figs. 5c and 5d).

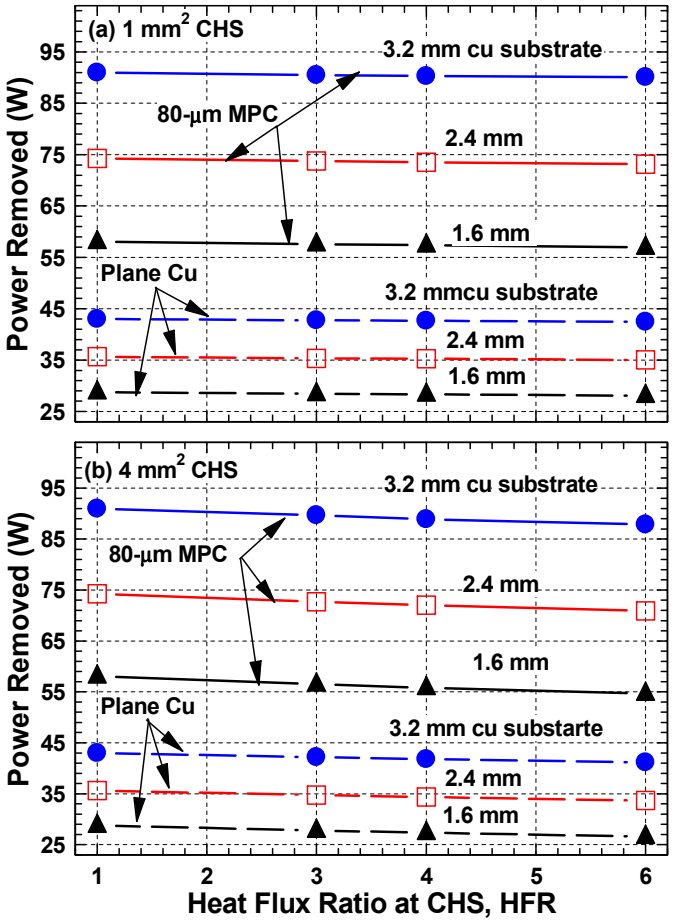


Fig. 6 Effects of CHS area and HFR and Cu substrate thickness on the thermal powers removed by MPC and plane Cu spreaders.

4.2 Effect of HFR at CHS on Spreaders' Performance

The thermal powers removed by the MPC spreaders with different Cu substrate thicknesses are plotted in Figs. 6a and 6b versus the HFR at the CHS in the underlying chip. Results for the plane Cu spreaders are also shown in these figures for comparison. With a 1 mm^2 CHS, increasing HFR from 1 (uniform heat dissipation) to 6 decreases slightly the thermal power removed by the MPC spreader with a 3.2-mm thick Cu substrate from 91.0 W to 90.1 W, compared to 58.05 and 56.95 W for the MPC spreader with a thinner substrate of 1.6 mm. For the same CHS area of 1 mm^2, the 3.2 mm and 1.6 mm thick plane Cu spreaders have smaller footprint areas and remove much less thermal

powers than the MPC spreaders: 43 W and 28.78 W when HFR = 1 and 42.47 W and 28.1 W when HFR = 6 (Fig. 6a). The results for the underlying chip with 4 mm^2 CHS are similar, except that the removed thermal powers by the MPC and plane Cu spreaders and their footprint areas are slightly smaller (Fig. 6b). With a 4 mm^2 CHS area, the MPC spreader with a 3.2 mm thick Cu substrate removes 87.85 W when HFR = 6. This power is significantly higher than the 41.16 W removed by the plane Cu spreader of almost the same thickness (Fig. 6b). In addition to the total thermal power removed and the spreader' footprint area, the HFR at CHS affects the maximum and the spatial distribution of the chip surface temperature.

4.3 Chip Surface Temperature Distribution

The plane Cu and MPC spreaders effectively decrease the chip surface temperature and mitigate the effect of the CHS areas on the local maximum temperature of the chip at CHS (Figs. 7a and 7b). The MPC (or *composite*) spreaders remove much more thermal powers and have larger footprint areas than the plane Cu spreaders, but increase the maximum surface temperature of the underlying chip at CHS. However, the ratio of the chip maximum to the average surface temperature is only a fraction of the HFR at the CHS (Fig. 7). Increasing the Chip's CHS area and the thickness of the Cu spreaders, or the Cu substrates of the MPC spreaders, increase the chip maximum temperature at CHS.

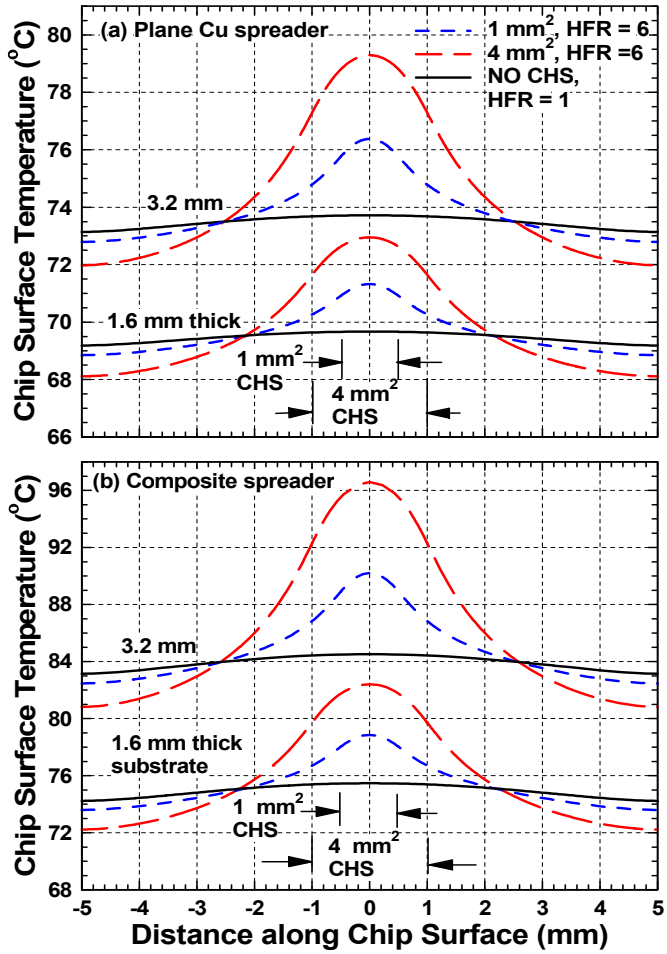


Fig. 7 Effects of CHS area and HFR and thickness of Cu substrate on the chip's surface and maximum temperatures.

With a 3.2 mm thick plane Cu spreader, when HFR = 6 the calculated maximum surface temperatures of the chip at the 1 and 4 mm^2 CHSs are 76.37°C and 79.29°C. These temperatures are only ~ 2.65 and 5.57°C higher, respectively, than that with a uniform heat dissipation, 73.72°C (HFR = 1). For the MPC spreader with a 3.2 mm thick Cu substrate, the chip maximum surface temperature at the 1 and 4 mm^2 CHS, when HFR = 6 (Fig. 7b), are 91.16 and 96.6°C, respectively, compared to 84.5°C for the chip with a uniform heat dissipation (Fig. 7b). Decreasing the thickness of the plane Cu spreader or the Cu substrate of MPC spreader from 3.2 to 1.6 mm markedly decreases the chip's maximum surface temperature and the temperature differential across the chip (Figs. 7a and 7b). It also decreases the thermal power removed and the spreader's footprint area. The next subsection compares the calculated performance surfaces of the plane Cu and MPC (or *composite*) spreaders at the same conditions (Figs. 8).

4.4 Spreaders' Performance Surfaces

The performance surfaces for the MPC (or *composite*) and plane Cu spreaders are compared in Figs. 8a and 8b. These surfaces are grids compromised of equal-thickness lines of the Cu spreaders or the Cu substrate of the MPC spreaders (1.6, 2.4 and 3.2 mm), and intersecting lines of the HFR at the CHS in the underlying chip (1 - 6). The performance surfaces in Fig. 8a are for a chip with a 1 mm^2 CHS and those in Fig. 8b are for a chip with a 4 mm^2 CHS. The performance surface for the MPC (or composite) spreaders is much wider than for the plane Cu spreaders of almost the same thicknesses.

Increasing the CHS area expands the performance surface of the MPC spreaders, but only slightly that of the plane Cu spreaders (Figs. 8a and 8b). The thermal powers removed by the MPC spreaders are ~ 2 times those removed by the plane Cu spreaders of almost the same thicknesses, when the CHS area is 1 mm^2 (Fig. 8a). However, the corresponding chip maximum surface temperatures are 5.79 – 13.36°C higher than with the plane Cu spreaders (Figs. 8a and 8b). This is because the thermal powers removed by MPC (or *composite*) spreaders are higher and the footprint areas are larger than those of the plane Cu spreaders.

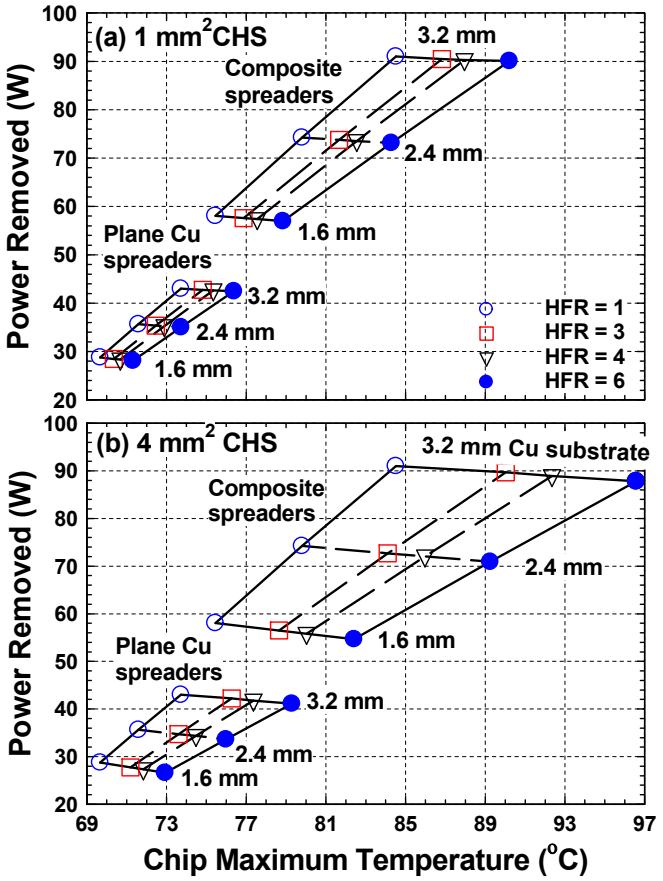


Fig. 8 Performance surfaces for MPC and plane Cu spreaders.

For a MPC spreader with a 1.6 mm thick Cu substrate, when HFR = 6 the local heat flux at the 1 mm^2 and 4 mm^2 CHS of the underlying chip is 325.43 and 273.3 W/cm^2, respectively. For the same HFR, increasing the thickness of the Cu substrate of the MPC spreader to 3.2 mm increases the local heat flux at the 1 mm^2 and 4 mm^2 CHS to 514.85 and 439.25 W/cm^2, respectively (Figs. 8a and 8b). With plane Cu spreaders, the removed thermal powers and the local heat fluxes at the Chip's CHSs are much lower than with the MPC spreaders. For a 1.6 mm thick plane Cu spreader, when HFR = 6 the local heat flux at the chip's 1 and 4 mm^2 CHSs is 160.6 W/cm^2 and 133 W/cm^2, respectively.

For the same HFR, increasing the thickness of the plane Cu spreader to 3.2 mm increases the local heat flux at the 1 and 4 mm^2 CHS of the chip to 242.7 W/cm^2 and 205.8 W/cm^2, respectively (Figs. 8a and 8b). The distinct differences in the performance of the MPC (or *composite*) and plane Cu spreaders affect their total thermal resistances and the maximum surface temperatures of the underlying chip. These effects and the values of the individual thermal resistances as well as the total thermal resistances of the plane Cu and MPC (or *composite*) spreaders are discussed next.

4.5 Spreaders' Thermal Resistances

The total thermal resistance, R_{TOT}, of the MPC spreaders is the sum of those for: (a) saturation boiling, R_{boil}, at the spreader surface, (b) heat conduction in the 80-μm MPC surface layer saturated with PF-5060 dielectric liquid, R_{MPC}, (c) heat conduction in the TIM between the Cu substrate and the underling chip, R_{TIM}, and (d) heat spreading in the Cu substrate, R_{sp}, as:

$$R_{TOT} = \left(T_{chip,\max} - T_{sat}\right)/Q = R_{TIM} + R_{sp} + R_{MPC} + R_{boil}. \quad (1)$$

The individual thermal resistances in this equation are defined as:

$$R_{TIM} = TI_{TIM}/A_{chip}, \quad (2a)$$

$$R_{sp} = \left(T_{chip,\max} - \overline{T}_{cu}\right)/Q - R_{TIM}, \quad (2b)$$

$$R_{MPC} = \left(\overline{T}_{cu} - \overline{T}_{s,MPC}\right)/Q, \quad (2c)$$

$$R_{boil} = \left(\overline{T}_{s,MPC} - T_{sat}\right)/Q. \quad (2d)$$

The average surface temperatures of the Cu substrate, $\overline{T}_{Cu}$, and the MPC surface layer, $\overline{T}_{s,MPC}$, are expressed, respectively, as:

$$\overline{T}_{cu} = \left(\int_{-0.5L_{sp}}^{+0.5L_{sp}}\int_{-0.5L_{sp}}^{+0.5L_{sp}} T_{cu}(x,y)\,dx\,dy\right)/L_{sp}^2, \quad (3a)$$

$$\overline{T}_{s,MPC} = \left(\int_{-0.5L_{sp}}^{+0.5L_{sp}}\int_{-0.5L_{sp}}^{+0.5L_{sp}} T_{s,MPC}(x,y)\,dx\,dy\right)/L_{sp}^2. \quad (3b)$$

For the plane Cu spreader, the total resistance is given as:

$$R_{TOT} = \left(T_{chip,\max} - T_{sat}\right)/Q = R_{TIM} + R_{sp} + R_{boil}. \quad (4)$$

While the R_{TIM} is independent of the total thermal power removed by the spreaders, Q, (Eq. 2), the values of R_{boil}, R_{MPC}, Rsp, and hence the spreader's total resistance, R_{TOT} depend on the thermal power removed, Q, the chip maximum surface temperature at CHS, and the average top surface temperatures of the Cu substrate and the MPC surface layer. Note that for the same TI_{TIM}, increasing the chip's footprint area would decrease the TIM's thermal conduction resistance, R_{TIM}. The individual and total thermal resistances for the plane Cu and MPC (or *composite*) spreaders are plotted in Figs. 9a and 9b versus the HFR, for the underlying chip with 4 mm^2 CHS. The results in these figures are for different thicknesses of the Cu substrate in the MPC spreaders and of the plane Cu spreaders (1.6, 2.4 and 3.2 mm). The heat spreading resistance, R_{sp}, is practically independent of the thickness of the plane Cu spreaders, but increases linearly with increasing the HFR (Fig. 9a). For the MPC (or *composite*) spreaders, however, the heat spreading resistance, R_{sp} increases slightly as the thickness of the Cu substrate increases (Fig. 9b). For both the MPC and plane Cu spreaders, R_{sp} increases linearly with the HFR.

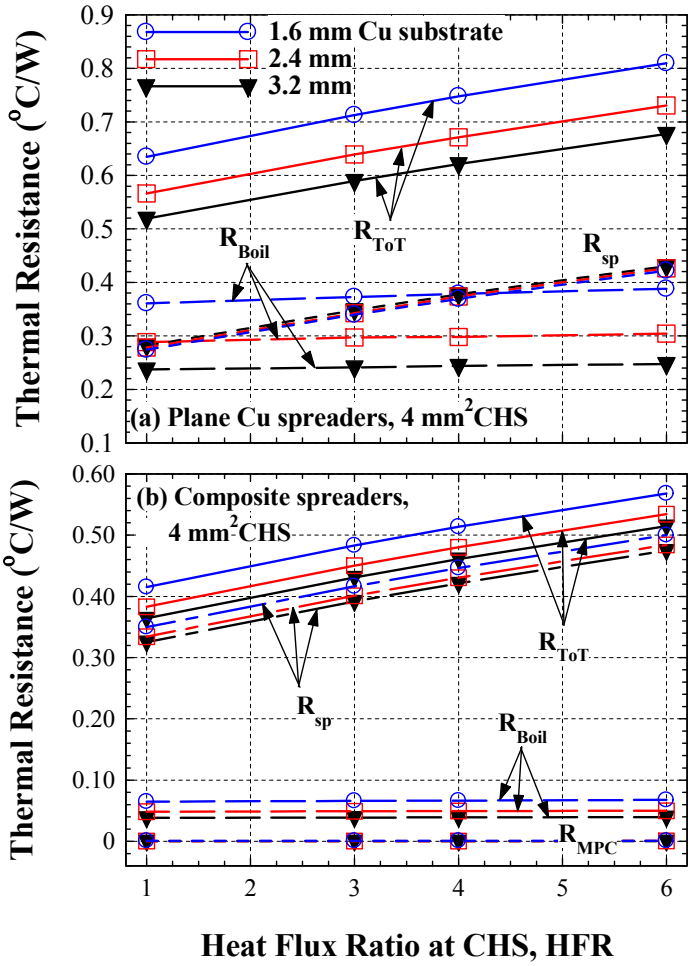


Fig. 9 Thermal resistances for MPC and plane Cu spreaders.

The boiling resistance, R_{Boil}, is almost independent of the HFR for the CHSs of the underlying chip, but that for the MPC surface layer is much lower than that for saturation boiling of PF-5060 dielectric liquid on plane Cu (Figs. 9a and 9b). This is because the values of nucleate boiling heat transfer coefficients on MPC are much higher than that on plane Cu (Fig. 2b) and the corresponding surface temperatures are lower (Fig. 2b). On the other hand, the larger footprint areas of MPC (or *composite*) spreaders increase their resistances for heat spreading. However, these resistances are much lower than for the plane Cu spreaders of almost the same thickness. The plane Cu spreaders remove much less thermal powers and have smaller footprint areas than the MPC spreaders (Fig. 9a). R_{TIM} is constant (0.19°C/W) and independent of the HFR for the underlying chip as well as the thermal power removed from the spreader surface. It depends on the surface area of the underlying chip, which in the present analysis is constant 1 cm^2.

The total thermal resistances, R_{TOT}, of the spreaders increase as either the HFR for the Chip's CHS increases or the thickness of the Cu substrate in the MPC spreaders (Fig. 9b) or the plane Cu spreaders decreases (Fig. 9a). The highest total resistance in Fig. 9a is that of the 1.6 mm thick plane Cu spreader when HFR = 6 (0.81°C/W). This resistance is 42.6% higher than that of the MPC spreader (0.568 C/W) with the same Cu substrate thickness of 1.6 mm (Fig. 9b). When HFR = 6, increasing the thickness of the plane Cu spreader to 3.2 mm decreases its total thermal resistance to 0.677°C/W (Fig. 9a). This

resistance is 31.6% higher than that of the MPC (or *composite*) spreader (0.515°C/W) with the same Cu substrate thickness of 3.2 mm (Fig. 9b).

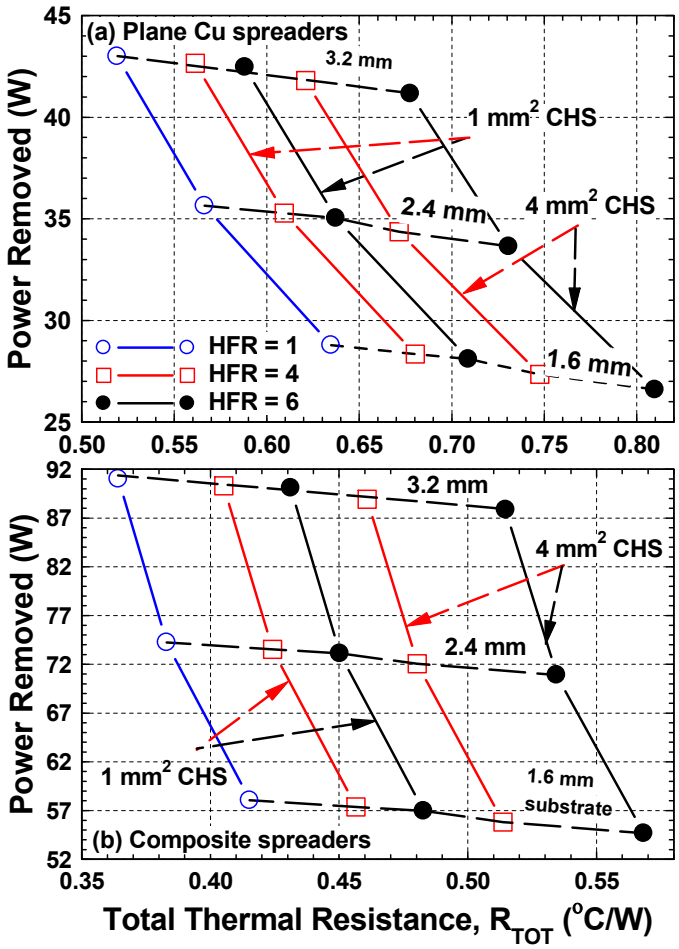


Fig. 10 Removed Thermal Power versus Total Thermal Resistance for Plane Cu and MPC Spreaders.

For both the plane Cu and MPC (or *composite*) spreaders, the increases in the total thermal resistance are associated with decreases in the thermal power removed and the spreaders' footprint areas (Figs. 10 and 11). For the same area and HFR of CHS of the underlying chip, the total thermal resistances of the plane Cu spreaders are consistently higher and the removed thermal powers are lower than those for the MPC spreaders Figs. 10a and 10b). Increasing the area and HFR of the CHS decrease the removed thermal powers and increase the spreaders' total thermal resistances (Figs. 10a and 10b). For an underlying chip with 4 mm^2 CHS and HFR = 6, the thermal powers removed by the plane Cu and the MPC spreaders are the lowest and the corresponding total thermal resistances are the highest.

Decreasing the area or HFR of the CHS and / or increasing the thickness of the plane Cu spreaders or the Cu substrates in the MPC (or composite) spreaders, increase the thermal powers removed from the spreaders' surfaces and decrease their total thermal resistances. The highest thermal powers removed and the lowest total thermal resistances are those of the MPC spreaders when the heat dissipation by the underlying chip is uniform (HFR = 1) and the Cu substrate is 3.2 mm thick (Fig. 10b). For this Cu substrate, the thermal power removed by the MPC spreader and the corresponding total thermal resistance are 87.85 W and 0.515°C/W, when the area and HFR of the CHS are 4 mm^2 and 6, respectively.

The thermal power removed from the surface of the MPC spreader by saturation boiling of PF-5060 dielectric liquid decreases to 54.66 W and the total thermal resistance increases to 0.568°C/W when the thickness of Cu substrate decreases to 1.6 mm (Fig. 10b). By comparison, when the area and HFR of the CHS are 4 mm^2 and 6, the thermal power removed by the 1.6 mm thick plane Cu spreader is only 26.6 W and its total thermal resistance is as much as 0.81°C/W.

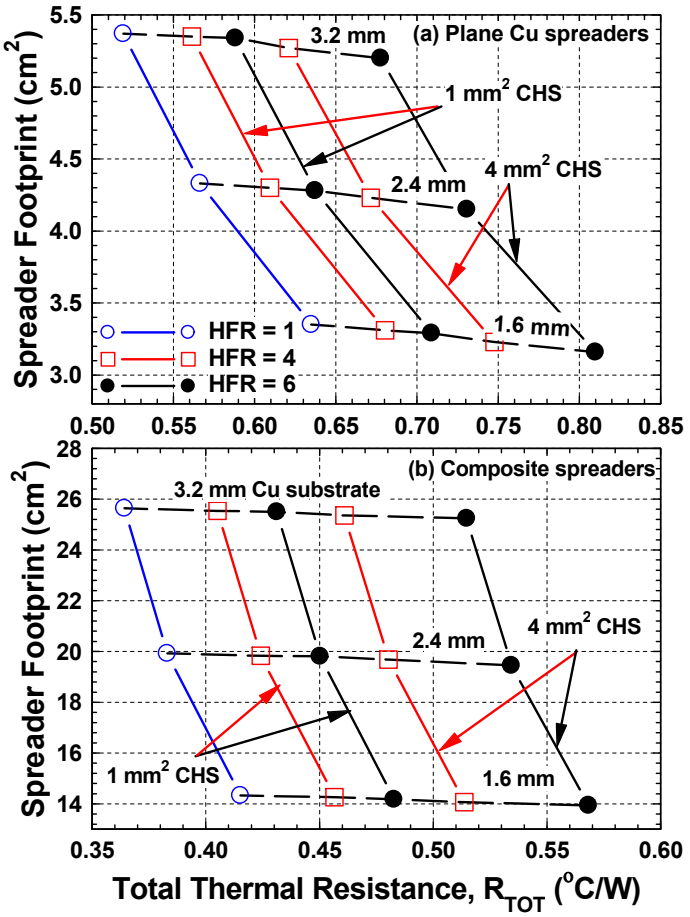


Fig. 11 Calculated footprint area versus the total thermal resistance for the plane Cu and MPC spreaders.

4.6 Spreaders' Surface Areas

The increases in the total thermal resistances of the spreaders are associated with decreases of both the thermal powers removed and the footprint areas (Figs. 10 and 11). Figures 11a and 11b plot the calculated footprint areas of the plane Cu and MPC (or *composite*) spreaders versus their total thermal resistances. While the footprint areas of the MPC spreaders are larger than those of the plane Cu spreaders, their total thermal resistances are lower. This is because the thermal powers removed by the MPC spreaders are markedly higher than by the plane Cu spreaders (Figs. 10a and 10b).

The footprint area of the MPC spreader with a 3.2 mm thick Cu substrate is 25.25 cm^2, when the area and HFR of the CHS in the underlying chip are 4 mm^2 and 6, respectively (Fig. 11b). When the CHS area decreases to 1 mm^2 the footprint area of this same MPC spreader increases only slightly to 25.5 cm^2. However, the spreader's total thermal resistance decreases from 0.515 to 0.431°C/W (Fig. 11b). The footprint areas of the 3.2 mm thick plane Cu spreader are 5.2 and 5.34 cm^2 when HFR = 6 and the CHS area is 1 and 4 mm^2, respectively. The corresponding total thermal resistances for this spreader are 0.588 °C/W and 0.677°C/W (Fig. 11a), while the removed thermal powers are 42.47 W and 41.16 W, respectively (Fig. 10a).

The smallest footprint areas and total thermal resistances and the largest thermal powers removed are those of the MPC (or *composite*) spreaders when the heat dissipated by the underlying chip is uniform (i.e., HFR = 1 in Fig. 11b). For this condition, the MPC spreaders with 2.4 mm and 3.2 mm-thick Cu substrates remove 74.26 W and 91.0 W and have total thermal resistances of 0.383°C/W and 0.364°C/W, respectively (Fig. 11b). For the plane Cu spreaders of almost the same thicknesses, the removed thermal powers are lower, 35.65 and 43.0 W

and the total thermal resistances are higher, 0.566 and 0.519°C/W, respectively (Fig. 11a), than those of the MPC spreader (Fig. 11b).

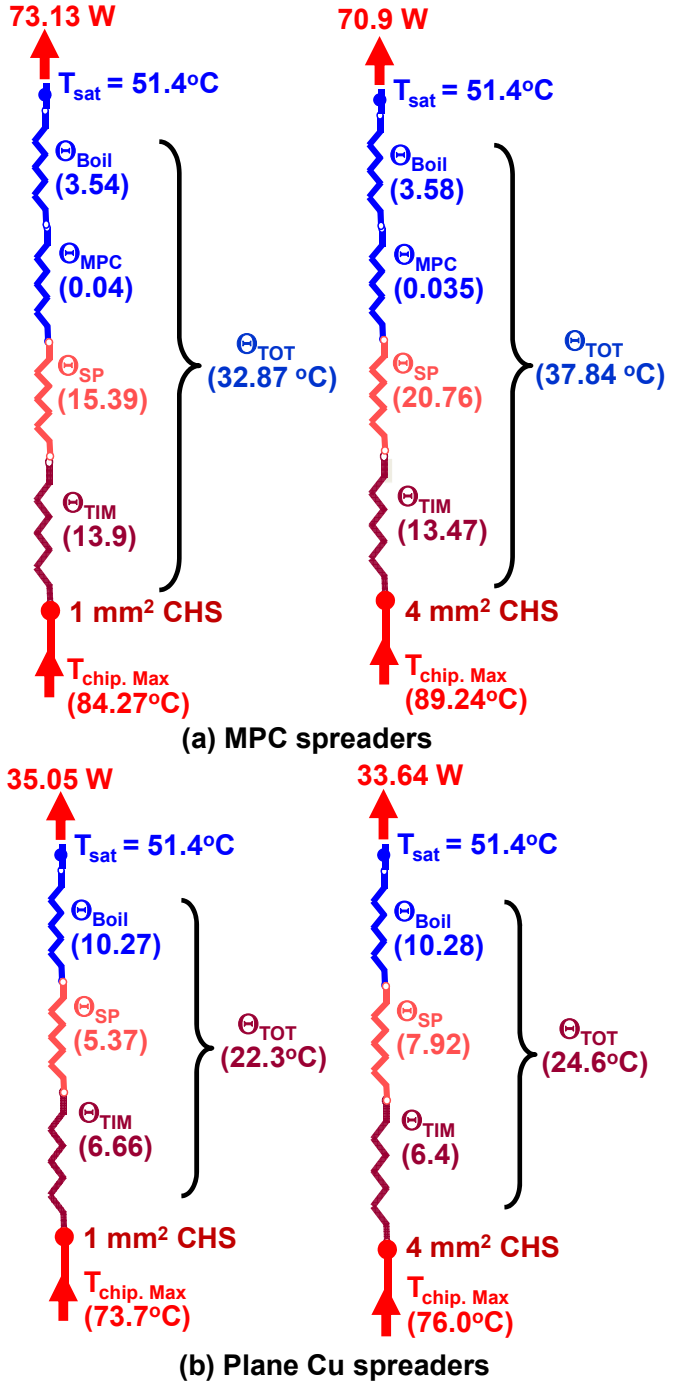


Fig. 12 Chip maximum surface temperatures and removed thermal powers by (a) MPC and (b) plane Cu spreaders [HFR = 6, t_{Cu} = 2.4 mm, TI_{TIM} = 0.19°C-cm²/W and CHS = 1 and 4 mm²].

4.7 Calculated Chip Surface Temperature

This section compares the calculated contributions of the various thermal resistances to the total thermal resistances of the plane Cu and MPC spreaders and hence, the maximum surface temperatures of the underlying chip at the CHSs. The thickness of the Cu spreaders and that of the Cu substrate of the MPC (or *composite*) spreaders is the same; 2.4 mm (Figs. 12a and 12b). The results in these figures are for a 10 x 10 mm chip with 1 and 4 mm² CHSs and HFR = 6. Results show that the primary contributor to the total thermal resistances of the MPC spreaders is that of heat spreading in the Cu substrate, R_{sp}, followed by R_{TIM}, R_{boil}, and then R_{MPC}, a distance fourth (Figs. 9b and 12b). By contrast, the primary contributor to the total thermal resistances of the plane Cu spreaders is $R_{boil,}$ followed a distance second by R_{TIM} and then R_{sp} (Fig. 9 and 12a). This is because of the low nucleate boiling heat transfer coefficient of PF-5060 dielectric liquid on plane Cu (Fig. 2b) and the small footprint areas of the plane Cu spreaders.

For the underlying chip with 1 mm² CHS, the thermal power removed from the top surface of the MPC spreader by saturation nucleate boiling of PF-5060 dielectric liquid is 73.13 W and the maximum surface temperature at the CHS is 84.27°C (Fig. 12a). This temperature reflects a total rise above the saturation temperature of PF-5060 dielectric liquid (51.4°C in Albuquerque, NM), Θ_{TOT} = 32.87°C. The total thermal resistance of this spreader, R_{TOT} = 0.45°C/W, is the sum of those for heat spreading in the Cu substrate (0.208°C/W), heat conduction in TIM (0.19°C/W), saturation boiling on the 80-μm thick MPC surface (0.048°C/W), and heat conduction in the MPC surface layer (0.00055°C /W) (Figs. 9b and 12a). The latter is negligibly small, contributing only 0.04°C to the increase in the chip maximum surface temperature. The largest contribution to the maximum temperature at the chip's CHS is that of heat spreading, Θ_{sp} = 15.39°C, in the 2.4 mm thick Cu substrate, followed close second by that of heat conduction in TIM, Θ_{TIM} = 13.9°C, then saturation boiling at the spreader's top surface, Θ_{Boil} = 3.54°C (Fig. 12a).

Figure 12a also shows the results for the same MPC spreader, but chip's CHS area of 4 mm². With this CHS area, the removed thermal power decreases to 70.9 W, but the chip's maximum surface temperature at CHS increases to 89.24°C. The contributions to this temperature due heat spreading and saturation boiling are Θ_{sp} = 20.76°C and Θ_{Boil} = 3.58°C, while those due to heat conduction in TIM and MPC top surface layer are Θ_{TIM} = 13.47°C and Θ_{MPC} = 0.035°C (Fig. 12a). With the 4 mm² CHS area, the total thermal resistance of the MPC spreader is 0.5337°C/W and the underling chip experiences a total temperature rise of Θ_{TOT} = 37.84°C above the saturation temperature of the PF-5060 liquid. The total resistance of this spreader (Fig. 9b) is the sum of those for heat spreading in the 2.4 mm thick Cu substrate (0.293°C/W), conduction in TIM (0.19°C/W), saturation boiling at the spreader's MPC surface (0.05°C/W) and heat conduction in the MPC surface layer (0.0005°C/W). In Fig. 12a, the heat flux at the 1 mm² and 4 mm² CHS of the underlying chip is ~ 417.9 W/cm² and 354.5 W/cm², respectively.

With plane Cu spreader of the same thickness as the Cu substrates of the MPC spreader (2.4 mm), the total thermal powers removed for the underlying chip with 1 and 4 mm² CHSs and HFR = 6 are only 35.05 and 33.64 W (Fig. 12b). The corresponding chip maximum surface temperatures are 73.7°C and 76.0°C, respectively. For the chip with 1 mm² CHS, the total thermal resistance of the 2.4 mm thick plane Cu spreader is 0.636°C/W and 0.731°C/W when the chip has a larger CHS of 4 mm² (Fig. 9a). These resistances are much higher than those of the MPC spreaders of almost the same thicknesses and which remove more than twice the thermal powers of the plane Cu spreaders.

Unlike for the MPC spreaders, the primary contributor to the total thermal resistances of the plane Cu spreaders in Fig. 12b is that of saturation boiling at the top Cu surface, R_{Boil}, followed by heat conduction in the TIM, $R_{TIM,}$ or heat spreading, R_{sp} (Fig. 9a). For the 2.4 mm thick plane Cu spreader, when the CHS area in the 10 x 10 mm underlying chip is 1 mm² (Fig. 12b), R_{Boil} = 0.293°C/W, R_{TIM} = 0.19°C/W and R_{sp} = 0.153°C/W (Fig. 9a). The total contribution to the chip maximum surface temperature (73.7°C) is the sum of those due saturation boiling, Θ_{Boil} = 10.27°C, heat conduction in TIM, Θ_{TIM} = 6.66°C and heat spreading, Θ_{sp} = 5.37°C (Fig. 12b). Increasing the Chip's CHS area to 4 mm² increases R_{Boil} to 0.304°C/W and R_{asp} to 0.3056 °C/W, but R_{TIM} is unchanged at 0.19°C/W (Fig. 9a). Also, the chip maximum surface temperature at CHS increases to 76°C, which reflects the increase in the thermal resistance due to heat spreading, Θ_{sp} = 7.92°C, while the thermal resistances due saturation boiling of PF-5060 dielectric liquid at the plane Cu spreader surface, Θ_{Boil} = 10.28°C

and heat conduction in TIM, Θ_{TIM} = 6.4°C change only slightly (Fig. 12b). In this figure, the local heat flux at the 1 and 4 mm^2 CHS in the underlying chip cooled with the 2.4 mm thick plane Cu spreader is 200.3 and 168.2 W/cm^2. In actual applications, the chip maximum surface temperatures could be lower and the removed thermal powers could be higher than those calculated in the present analyses. This is because the analyses *did not* account for the heat removed from the sides and bottom surface of the spreaders, likely by forced air convection (Fig. 3).

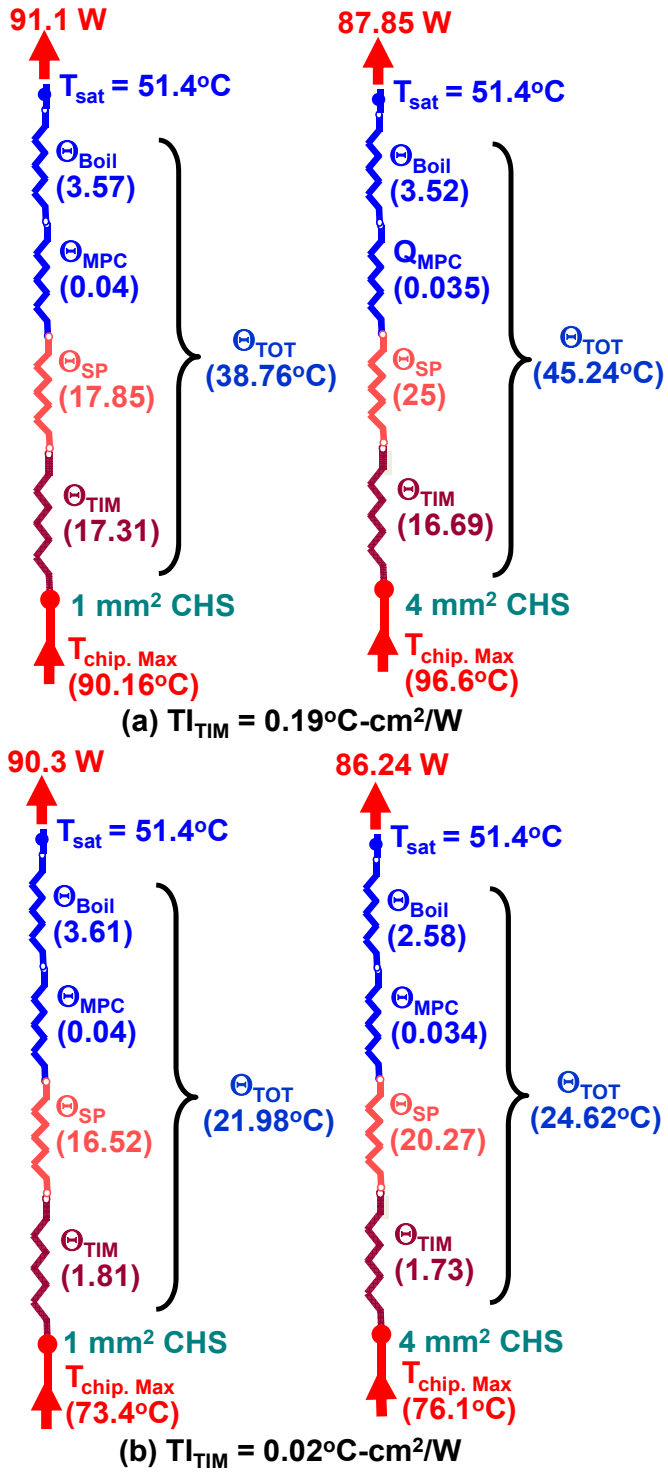


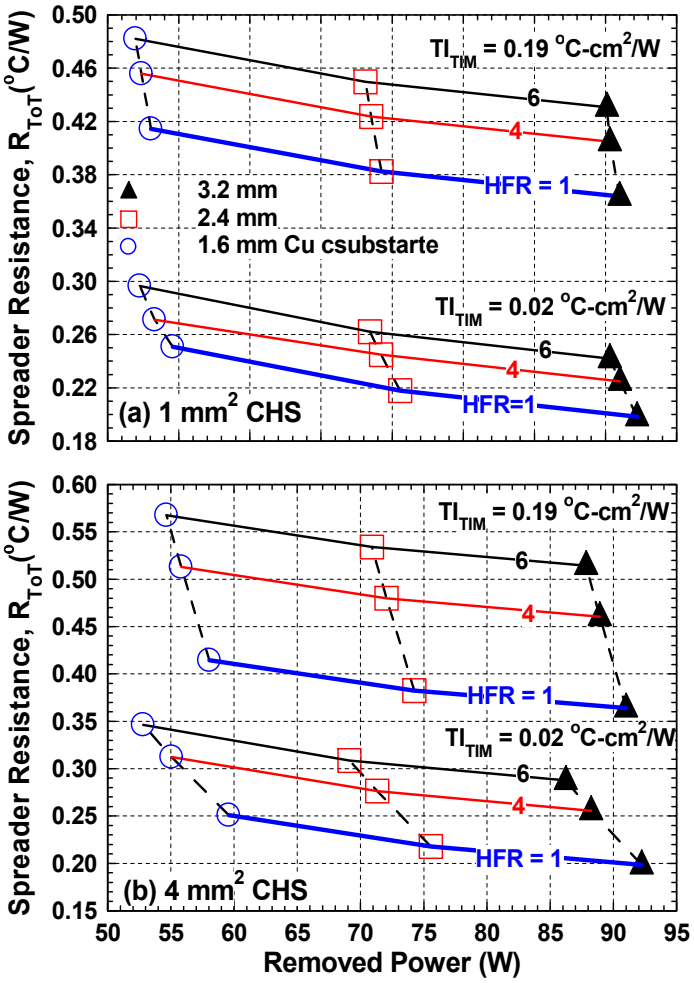
Fig. 13 Effect of TI_{TIM} on chip maximum surface temperature and removed thermal power by MPC spreaders; (a) TI_{TIM} = 0.19°C-cm^2/W and (b) TI_{TIM} = 0.02°C-cm^2/W [HFR = 6, t_{Cu} = 3.2 mm, and CHS = 1 and 4 mm^2].

The saturation temperature of PF-5060 dielectric liquid in Figs. 12a and 12b (51.4°C) is that in Albuquerque, NM at 0.085 MPa (51.4 °C). It is 3.1°C lower than at sea level or an ambient pressure of ~0.1 MPa. At that pressure, the increases in the nucleate boiling heat transfer coefficients at the top surface of the MPC and plane Cu spreaders, compared to those in Fig. 2b at ~0.085 MPa, would slightly increase the thermal powers removed and chip's surface temperatures at CHSs.

As indicated earlier, the results presented in Figs. 5 – 12 are for a thermal impedance of the TIM between the Cu substrate and the underlying 10 x 10 mm chip of 0.19°C/W. The next section presents the performance results for the MPC spreaders with a smaller TIM resistance of 0.02°C/W. This impedance is achievable by increasing the clamping pressure from 67 KPa to 1.72 MPa (Table 1).

4.8 Effect of Decreasing TIM Resistance

Performance results of the MPC spreaders with a 3.2 mm thick Cu substrate are presented for the underling chip with 1 and 4 mm^2 CHS and TIM impedance of 0.19°C-cm^2/W (Fig. 13a) and 0.02°C-cm^2/W (Fig. 13b). Comparing the results for the MPC spreaders in Figs. 12a and 13a, with the same TI_{TIM}, clearly show that increasing the thickness of the Cu substrate from 2.4 to 3.2 mm increases the thermal power removed by 24.6% and 23.9% and the corresponding chip maximum surface temperature at the 1 mm^2 and 4 mm^2 CHS by only ~ 7% and 8.25% to 90.16°C and 96.6°C, respectively (Fig. 13a). The largest contributor to the chip maximum temperature at CHS is heat spreading in the Cu substrate, followed by heat conduction in TIM, and saturation boiling at spreader surface.



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ISSN: 2151-8629

Fig. 14 Effect of TI_{TIM} and Chip's CHS area and HFR on MPC spreaders' total thermal resistances and removed powers.

Decreasing the TI_{TIM} between the Cu substrate and the underlying chip markedly decreases the chip's maximum temperatures at CHSs and only slightly the thermal powers removed by the MPC spreaders with the same Cu substrate thickness of 3.2 mm, but for different areas of the CHS in the underlying chip (Figs. 13a and 13b). Fig. 13a is for TI_{TIM} = 0.19°C-cm^2/W and Fig. 13b is for TI_{TIM} = 0.02°C-cm^2/W. Figure 13b shows that for underlying chips with 1 and 4 mm^2 CHS, the thermal powers removed by the MPC spreaders are 90.3 W and 86.24 W, compared to 91.1 W and 87.85 W in Fig. 13a. The corresponding chip's maximum surface temperatures at CHSs of 73.4°C and 76.1°C (Fig. 13b) are significantly lower than those of 90.16°C and 96.6°C in Fig. 13a. The chip's maximum surface temperatures at CHSs in Fig. 13b are much lower than those recommended by the chip manufactures ($\leq$ 85 - 125°C, depending on application [1]). The following subsections present additional performance results of the MPC spreaders with smaller TI_{TIM} of 0.02°C-cm^2/W (Figs. 14 - 17).

4.9 Spreader Total Thermal Resistance and Footprint area

Results in Figs. 14a and 14b show that decreasing TI_{TIM} from 0.19°C-cm^2/W to 0.02°C-cm^2/W decreases the total resistance of the MPC spreaders by ~ 38 – 44%, depending on the area and HFR for the CHS in the underling chip; it only slightly decreases the removed thermal powers by the MPC (or *composite*) spreaders. Results also show that increasing the chip's CHS area from 1 mm^2 (Fig.14a) to 4 mm^2 (Fig. 14b) decreases the total thermal resistances of the MPC spreaders, and slightly increases the removed thermal powers. The calculated changes, however, depend on the value of HFR at CHS. The performance results of MPC spreaders for the chip with CHSs (HFR = 2 - 6) are compared to those for the chip without CHSs (HFR =1).

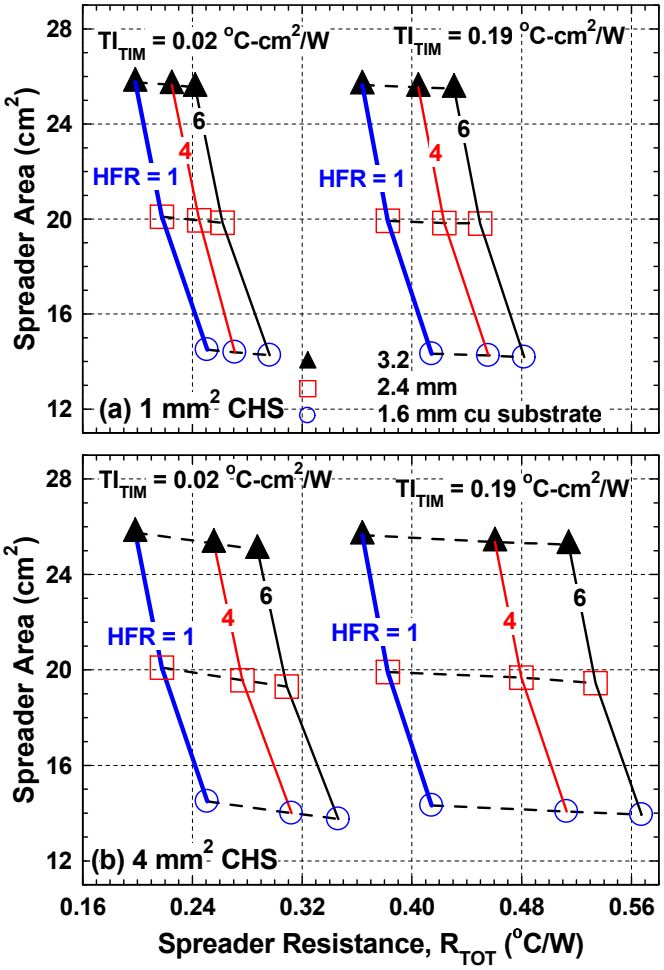

Fig. 15 Effects of TI_{TIM} and chip's CHS's area and HFR on footprint area of MPC spreaders.

With uniform heat dissipation by the underling chip (or HFR = 1), the MPC spreaders have the lowest total thermal resistances, $R_{TOT,}$ and remove the highest thermal powers, Q. Increasing HFR at CHSs to 2 - 6 increases both R_{TOT} and the removed thermal powers for the MPC spreaders. The effect of increasing HFR at the chip's CHS is more pronounced for the larger CHS area of 4 mm^2 (Fig. 14b). Increasing the thickness of the Cu substrates in the MPC spreaders decreases their total resistances because of the increase in the removed thermal powers and the decrease in the thermal resistances for heat conduction in TIM and heat spreading in the Cu substrate (Figs. 14a and 14b).

The removed thermal powers by the MPC spreaders increase and R_{TOT} decrease as TI_{TIM} and or the thickness of the Cu substrate increases, and the area and /or the HFR of the CHS decreases (Figs 14a and 14b). The increases in R_{TOT} depend on the footprint areas of the MPC spreaders. Figs. 15a and 15b show that for the same CHS area in the underlying chip, R_{TOT} of the MPC spreader increases, while its footprint area decreases as the thickness of the Cu substrate increases. Decreasing TI_{TIM} markedly decreases R_{TOT}, but only slightly increases the footprint area of MPC spreader. Decreasing the HFR at the chip CHS also decreases R_{TOT} and increases the footprint area of the MPC spreader; these effects, however, are more pronounced for the underlying chip with the large CHS area of 4 mm^2 (Fig. 15b).

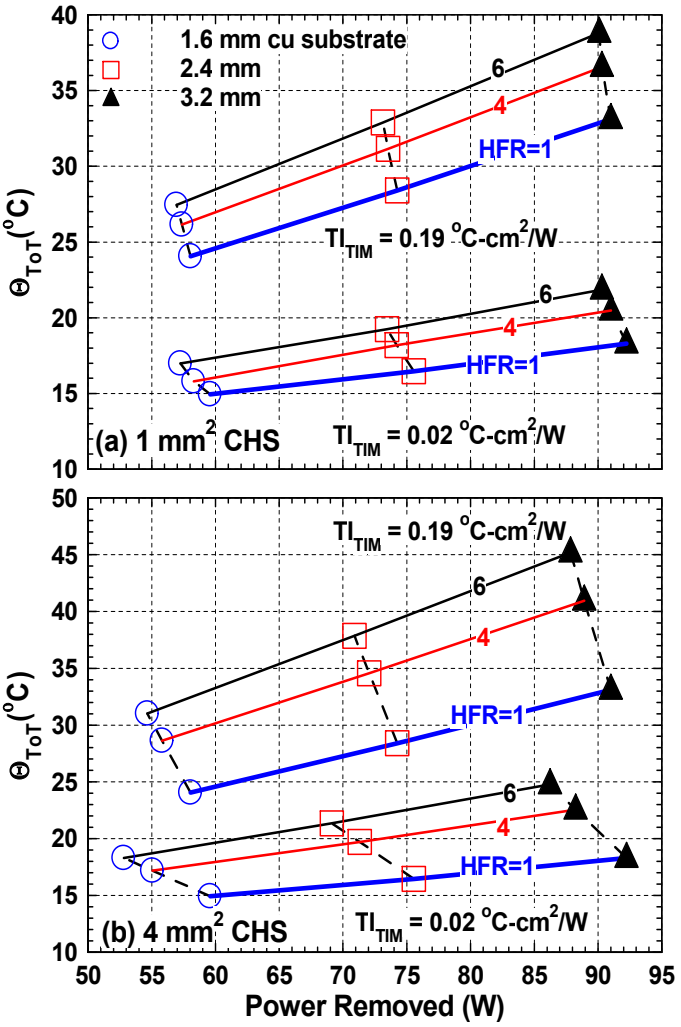

Fig. 16 Effects of the TI_{TIM} and CHS's area and HFR on the rise in surface temperature of underlying chip.

4.10 Total Rise in Chip Maximum Temperature

Figures 16a and 16b plot the calculated total rise in the chip maximum surface temperature at CHSs, Θ_{TOT}, above that of saturation boiling of PF-5060 at the MPC top surface of the spreaders (Figs. 12 and 13). This temperature rise is the sum of those due to nucleate boiling, heat conduction in MPC surface layer and the TIM, and heat spreading in the Cu substrate. The values of Θ_{TOT} for the MPC spreaders correlate directly with the removed thermal powers and decrease as the area and HFR of the CHS in underlying chip and/or the thickness of the Cu substrate decrease (Figs. 16a and 16b). Decreasing the Cu substrate thickness decreases the temperature rise due heat spreading (Fig. 9b), decreasing both Θ_{TOT} and the removed thermal powers by the MPC spreaders (Figs.12a, 13a and 16). For the same Cu substrate thickness and HFR and area of CHS, decreasing TI_{TIM} from 0.19°C-cm^2/W to 0.02°C-cm^2/W markedly decreases Θ_{TOT} for the MPC spreaders and hence, the chip's maximum surface temperature at CHS (Figs. 16 and 17**).**

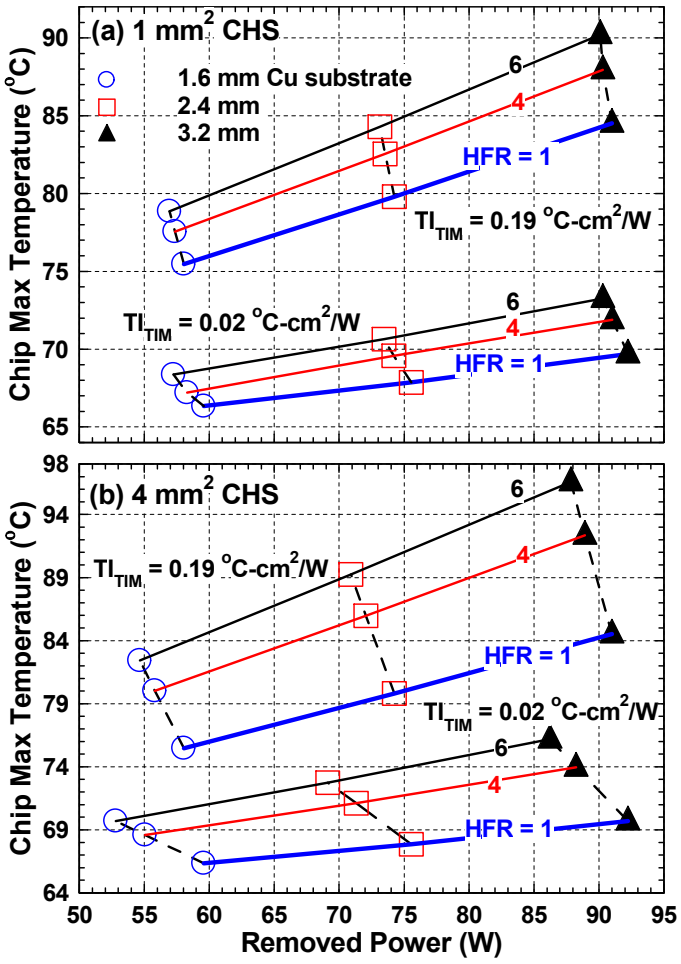

Fig. 17 Effects of TI_{TIM} and the chip's CHS area and HFR on of the chip maximum surface temperature.

4.11 Chip Maximum Surface Temperature

The results in Figs. 17a and 17b are of the maximum surface temperature at CHS of the underlying 10 x 10 mm chip with MPC spreaders cooled by saturation nucleate boiling of PF-5060 dielectric liquid. This temperature at the chip's CHS directly correlates with the removed thermal power by the MPC spreader. It is highest for the spreader with 3.2 mm thick Cu substrate and CHS area and HFR of 4 mm^2 and 6, respectively (Fig. 17b), and lowest for the chip with a uniform heat dissipation (HFR = 1).

Decreasing the TI_{TIM} from 0.19°C-cm^2/W to 0.02°C-cm^2/W decreases the chip's maximum surface temperature at CHS by as much as ~ 10.5 – 21°C, depending on the thickness of the Cu substrate and the area and HFR of the CHS (Figs. 17a and 17b). For the chip with 4 mm^2 CHS, the maximum surface temperature at the CHS is a few degrees higher and the removed thermal power by the MPC spreader is a few watts lower than for the chip with 1 mm^2 CHS.

When TI_{TIM} = 0.02°C-cm^2/W and Cu substrate thickness is 3.2 mm, the calculated chip maximum surface temperatures are $\leq$ 76°C and the removed thermal powers by MPC spreaders are > 86 W, regardless of the area and HFR for CHSs in the underling chip (Figs. 17a and 17b).

Figures 18a and 18b present cross-sectional views of the MPC spreader and the underlying chip, which show the temperature contours in the 3.2 mm thick Cu substrate and the underlying chip with 4 mm^2 and HFR of 6 for the CHS. The results in Fig. 18a are for TI_{TIM} = 0.02°C-cm^2/W and those in Fig. 18b are for TI_{TIM} = 0.19°C-cm^2/W. Not that the chip maximum surface temperature at CHS in Fig. 18a and 19a is > 20.46°C lower that in Figs. 18b and 19b, but also the removed thermal power from the top surface of the MPC speeder is also lower (Fig. 13). Figures 19a and 19b show plane view of the calculated temperature contours at the top surface of the underling 10 x 10 mm chip with 4 mm^2 and HFR = 6 for the CHS. The dotted squares at the center of the images in Figs. 19a and 19b are of the 2 mm x 2 mm CHS.

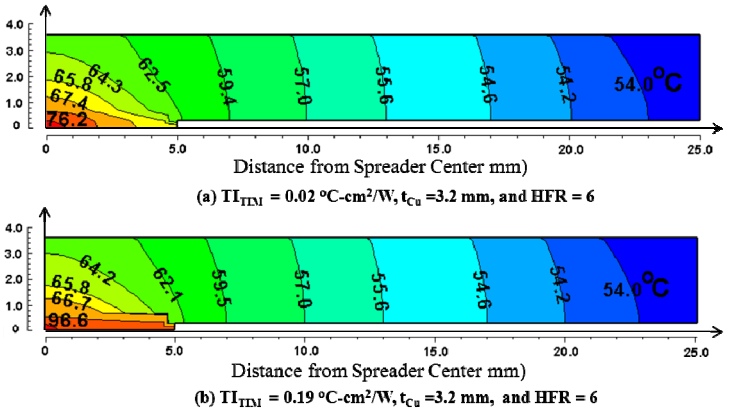

Fig. 18 Effect of TIM impedance on calculated temperature contours at mid-section of MPC spreaders for cooling 10 x1 0 mm underlying chip with 4 mm^2 CHS.

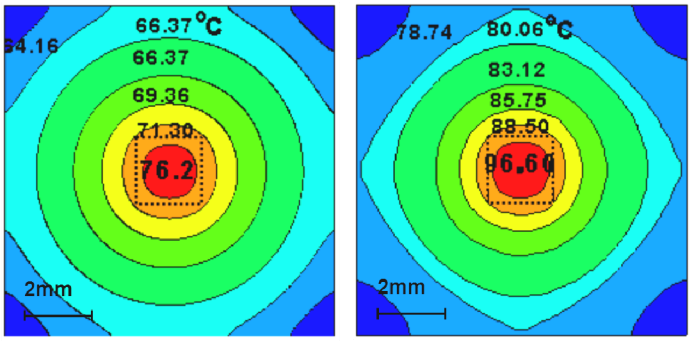

Fig. 19 Calculated temperature contours at top surface of 10 x1 0 mm chip with 4 mm^2 CHS and cooled using MPC spreader.

5. SUMMARY AND CONCLUSIONS

Numerical thermal analyses are performed to investigate the potential of Cu spreaders with MPC surface for immersion cooling of a 10 x 10 mm underlying computer chip with a center hot spot and

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ISSN: 2151-8629

removing > 85 W at junctions' temperatures < 100°C. These spreaders comprise a 1.6 - 3.2 mm thick Cu substrate and 80-µm thick MPC surface cooled by saturation nucleate boiling of PF-5060 dielectric liquid. These spreaders take advantage of the enhancement in nucleate boiling of PF-5060 dielectric liquid on the 80-µm thick MPC surface layer and the good heat spreading in the Cu substrate. The MPC surface layer could easily be deposited onto Cu substrate using conventional electrochemical deposition processes.

The performed numerical analyses investigated the effects of the local heat flux at the chip's 1 and 4 mm^2 CHS and the impedance of the thermal interface material (TIM), between the Cu substrate and underlying chip, on the spreaders' total thermal resistance and thermal power removed as well as the Chip's maximum temperature at CHS. The analyses varied the heat flux ratio at the CHSs (HFR) from 2 to 6 times that of the chip's surface average outside the hot spot. The values of the impedance of the TIM material between the Cu substrate and the underlying chip are 0.19 and to 0.02°C--cm^2/W.

Calculated are the spreaders' total thermal resistances, footprint areas and thermal powers removed. Also calculated are the individual thermal resistances for saturation boiling at the spreaders' surface, heat conduction in the MPC surface layer, heat spreading in Cu substrate, and heat conduction in TIM. In addition, the spatial temperature distributions at the chip and spreaders' surfaces and the chip's maximum surface temperature at CHS are calculated and compared. The performance results of the MPC spreaders are compared to those of plane Cu spreaders of the same thickness as the Cu substrates in the MPC spreaders and to those with no CHS in the underlying chip (HFR = 1 or uniform heat dissipation).

The results clearly demonstrate the effectiveness of the MPC spreaders for immersion nucleate boiling cooling of underlying 10 x 10 mm chip with CHS areas of 1 and 4 mm^2, and HFR of as much as 6 at CHSs. Increasing the CHS area and HFR decrease the removed thermal powers and increase the total thermal resistances of the MPC spreaders. Increasing the Cu substrate thickness increases the thermal powers removed and decreases the total thermal resistances of the MPC spreaders. The removed thermal powers by these spreaders are highest and the total thermal resistances are lowest when the heat dissipation by the 10 x 10 mm underlying chip is uniform (HFR =1). When the CHS area and HFR are 4 mm^2 and 6, the thermal power removed by the MPC spreader with 3.2 mm thick Cu substrate is 87.85 W and the corresponding total thermal resistance is 0.515°C/W.

When the CHS area of the underlying chip decreases to 1 mm^2, while keeping the HFR at 6, the MPC spreader with 3.2 mm thick Cu substrate removes 91.1 W and has a total thermal resistance of 0.425°C/W. The largest contributor to this resistance is that of heat spreading in the Cu substrate (0.1976°C/W), followed by that of heat conduction in TIM (0.19°C/W) and saturation boiling (0.039°C/W). The thermal resistance of MPC layer is significantly small (0.00044°C/W).

When HFR = 6, decreasing the thickness of the Cu substrate in the MPC spreader to 2.4 decreases the thermal power removed for the 10 x 10 mm underlying chip with 1 and 4-mm^2 CHSs to 73.13 and 70.9 W, respectively. The corresponding chip maximum surface temperatures at these CHSs are 84.27°C and 89.24°C, respectively. In electronics cooling applications, the TI_{TIM} of 0.02°C-cm^2/W would effectively decrease the chip's maximum surface temperature, while negligibly decreasing the thermal powers removed by the MPC spreaders. The performance of the plane Cu spreaders of the same thickness as the Cu substrates in the MPC spreaders is markedly inferior. The total thermal resistances of the plane Cu spreaders are consistently higher and the removed thermal powers are lower than those using the MPC spreaders.

The effectiveness of the MPC spreaders for immersion cooling is demonstrated in terms of increasing the removed thermal powers for the 10 x 10 mm underlying Chip with CHS to in excess of 85W, decreasing the total thermal resistance for maintaining acceptable chip maximum surface temperatures at CHS of < 100°C. The MPC spreaders mitigate the effect of the CHSs by limiting the increase in the chip's maximum surface temperature to only a few degrees, even when the HFR at the CHSs is 6 times that of the chip's surface average outside the CHSs. It is worth noting that in immersion cooling applications, the chip's maximum surface temperature could be somewhat lower than those calculated in the present analysis, which *did not* take credit for the heat removal, likely by forced convection of air, from the sides and bottom surfaces of the spreaders and the die.

ACKNOWLEDGEMENTS

This research is funded by the University of New Mexico's Institute for Space and Nuclear Power Studies.

NOMENCLATURE

A	surface or footprint area (cm^2)
CHF	critical heat flux (W/cm^2) or (kW/m^2)
CHS	central hot spot
HFR:	heat flux ratio at CHS
Cu	Copper
h	heat transfer coefficient (W/cm^2K) or (kW/m^2 K)
L	width (cm) or (mm)
MPC	micro-porous copper
Q	thermal power removed from spreader surface (W) or (kW)
x, y, z	cartésien coordinats (Fig. 3)
R	thermal resistance (°C/W)
t	thickness (mm) or (µm)
T	temperature (°C) or (K)
TI	thermal impedance (°C-cm^2/W)
TIM	thermal interface material
Greek symbols	
Θ	temperature rise (°C) or (K)
ρ	density (kg/m^3)
σ	surface tension (N/m)
Subscripts	
Boil	saturation nucleate boiling
Chip	computer chip, chip surface
Cu	Copper
ℓ	liquid
NB	nucleate boiling
Max	maximum
MNB	maximum nucleate boiling
MPC	micro-porous Cu
s	surface
sat	saturation
sp	spreader, Cu substrate
TIM	thermal interface material
TOT	total
v	vapor

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