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A Novel Polymorphic Topology with Hybrid Control Strategy Based LLC Resonant Converter for Ultra-Wide Input Voltage Range Applications

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ABSTRACT

To realize effective utilization of renewable energy sources, a novel polymorphic topology with hybrid control strategy based LLC resonant converter was analyzed and designed in this paper. By combining the merits of a full bridge LLC resonant converter, three-level half bridge LLC resonant converter, and variable frequency control mode, the converter realizes an intelligent estimation of input voltage by automatically changing its internal circuit topology. Under this control strategy, different input voltages determine different operation modes. This is achieved in full bridge LLC mode when the input voltage is low. If the input voltage rises to a certain level, it operates in three-level half bridge LLC mode. These switches are digital and entirely carried out by the DSP (Digital Signal Processor), which means that an auxiliary circuit is unnecessary, where a simple strategy of software modification can be utilized. Experimental results of a 500W prototype with 100V~600V input voltage and full load efficiency of up to 92% are developed to verify feasibility and practicability. This type of converter is suitable for applications with an ultra-wide input voltage range, such as wind turbines, photovoltaic generators, bioenergy, and other renewable energy sources.

KEYWORDS

Renewable energy sources; power converter; ultra-wide input voltage range; multi-levels operation mode; hybrid control strategy; soft switching

1 Introduction

With the further developments in society and the economy, energy demand is dramatically increasing, and non-renewable energy sources, such as fossil energy, are becoming increasingly exhausted. The energy crisis is getting worse. More scholars are paying attention to new energy technologies, such as photovoltaic generators and fuel cells, and renewable energy sources have become widely used in recent years [1–4]. Compared with traditional energy, the development and utilization of renewable energy is useful measures in solving the energy crisis and environmental pollution. However, due to the influence of natural factors such as climatic conditions, many renewable energy generation units' power characteristics show discontinuity, poor stability, low utilization rate, and a wide output voltage range. Therefore, it is necessary to design an energy converter that can work in a wide input range in order to realize the efficient utilization of renewable energy sources.

In Fig. 1, zero-voltage switching (ZVS) topologies are preferable for the isolated second stage to enhance efficiency. In particular, the multi resonance LLC topology has several advantages over ZVS topologies. These advantages include:

a) Primary side switches can realize zero -voltage switching (ZVS) in the full load range.
b) Secondary rectifying diodes can realize zero- current switching (ZCS), thus reducing the switching loss.
c) Only the capacitor is applied as the output filter compared with the traditional LC filter.
d) Since there is no filtering inductance on the secondary side of the converter, the voltage stress of the full bridge rectifier diode is only the output voltage.
e) Simple structure due to the absence of clamp circuit.
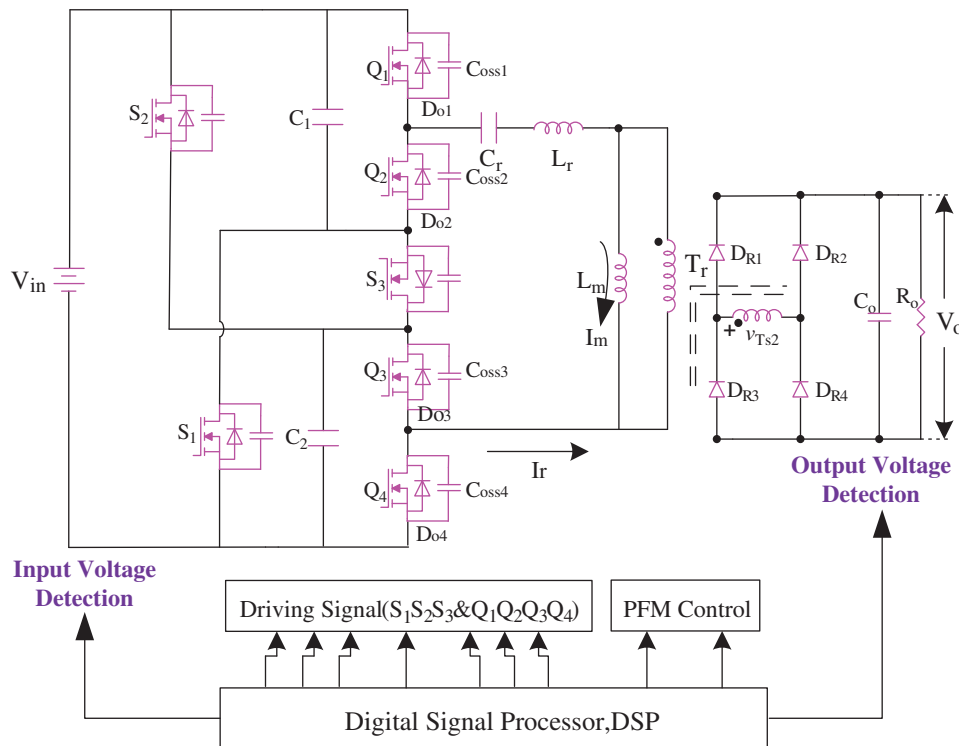f) Low EMI radiation.

Figure 1: Polymorphic topology converter

LLC resonant converters can realize high efficiency, high power density, and low cost of power conversion, which have been analyzed and studied as the topology of this paper [5–9].

The LLC resonant converter has become a hot research topic in the past two decades. Generally speaking, the LLC resonant converter operates through a variable-frequency (VF) control strategy, and its operating frequency range is limited. Therefore, it is not suitable for applications with a wide input voltage range. To solve this problem, some scholars have proposed various improvement methods for LLC resonant converters based on a new topology and control strategy.

In [10], a multilevel working mode half bridge LLC resonant converter has been proposed, which can operate in two-level modes according to the input voltage. However, there is not a smooth transition between

the two modes. Besides, the selection of transformer ratio, series resonant capacitance, leakage inductance, and other parameters lack sufficient theoretical bases.

A full bridge three-level LLC resonant converter is presented in Reference [11]. Although this converter operates in both three-level and two-level modes, as well as a wide input voltage range with a constant switching frequency control strategy, not all switches have a voltage stress half of the input voltage in three-level mode. Besides, both modes are difficult to control.

In [12], an LLC resonant converter with two series transformers was proposed, and its input voltage range can reach a maximum and minimum input voltage ratio of six. However, the parametric design process can be quite complicated.

Summarizing the existing literature on LLC resonant converter with a wide input voltage range, we have found that there is a lack of a relatively simple and accurate design method. This paper's main contribution is to propose a novel polymorphic topology with hybrid control strategy-based LLC resonant converter for ultra-wide input voltage range applications. The converter integrates two different high efficiency DC-DC converters to solve high pressure stress and low conversion efficiency. For the polymorphic converter, the internal circuit structure can be automatically changed. It is suitable for maximum efficiency of the two independent input voltage ranges of 100V~300V and 300V~600V. To save costs, the total number of power components (active and passive) of the two converters remains the same, sharing the same resonant cavity and high frequency transformer. When the circuit topology changes, the voltage stress of each switch will be half of the input voltage, and the advantages of soft switching remain unchanged. In this paper, the specific working principle and design idea are detailed. A 500W prototype with an input voltage range of 100V~600V and an output voltage of 48V have been built, which verifies the validity and applicability of the converter.

2 Principle and Working State Analysis of Polymorphic Topology

A novel polymorphic topology converter, which integrates two DC-DC topological structures, has been realized by a series of interface circuits composed of MOSFET as switches and DSP (Digital Signal Processor). With different input voltages, the converter's circuit structure changes by controlling the on and off of the MOSFET. As shown in Fig. 1, the topological structures and working mode of the two DC-DC converters are determined by the switches. When S_1, S_2 are off, and S_3 is on, a three-level half bridge LLC resonant converter suitable for input voltages of 300~600V is available; when S_1, S_2 are on, and S_3 is off, a full bridge LLC resonant converter with input voltage 100V~300V is built. In Fig. 1, the three MOSFETs S_1, S_2, and S_3 are switches, C_1 and C_2 are input filter capacitors, the four MOSFETs Q_1~Q_4 are main power switches while D_{o1}~D_{o4} and C_{oss1}~C_{oss4} are their parasitic diodes and capacitors, respectively. The primary side resonance inductance L_r (including the primary side leakage inductance of transformer), the resonant capacitance C_r, and the excitation inductance L_m constitute the resonant cavity. Since the resonant capacitor is in series on the primary side circuit, it also plays a role of isolation. The transformer excitation inductance enables the parallel connection between L_m and the transformer. N is the ratio of primary and secondary side turns of transformer T_r. The ultra-fast recovery diodes D_{R1}~D_{R4} of the secondary side constitute a full bridge rectifier circuit. C_o is the output filter capacitor, and R_o is the load resistance.

PFM (Pulse Frequency modulation) has been adopted in both two working modes. The ePWM1A, ePWM1B, ePWM2A, and ePWM2B of DSP output the drive signals with fixed duty cycle and dead zone time. The main power switches S_1, S_2, S_3, and S_4 are driven by the control circuit for energy conversion. The working principles of the two modes are listed as follows:

2.1 300V~600V High Line Input (Three-Level Half Bridge LLC, Mode1)

When the input voltage is high, a novel ZVZCS three-level half bridge LLC resonant converter is used on the primary side, as given in Fig. 2, which turns on S_3 while S_1 and S_2 is off. Two input divider equalization capacitors C_1 and C_2 in series are connected in parallel with the input voltage V_{in}, providing a midpoint potential to clamp the switches so the voltage stress is $V_{in}/2$ and facilitating the realization of soft switching. The four main power switches Q_1, Q_2, Q_3, and Q_4 are connected in series to form a three-level half bridge structure. In appearance, it is similar to the conventional three-level half bridge DC-DC converter. Nevertheless, its driving signal pulse modulation mode of the main switch is different, which results in a substantially different working principle and performance from the conventional three-level circuit. The driving signals of the four primary switches and the three switches are in Fig. 3. Q_1 and Q_4 are of the same set of driving signals; Q_2 and Q_3 are also of the same set. The driving signals of Q_1 and Q_4 are complementary, so are Q_2 and Q_3, and their duty cycle is 50% (regardless of dead-time). The output voltage is controlled by changing the switching frequency, which means the PFM modulation is applied instead of the traditional PWM modulation. Before the analyzing, we have made the following assumptions:
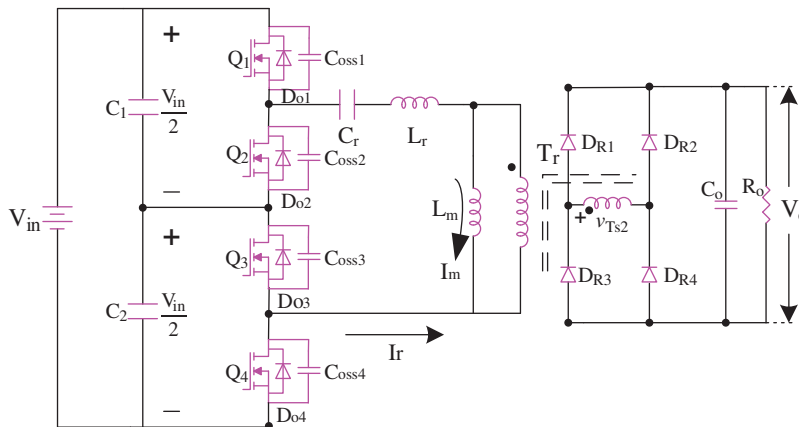

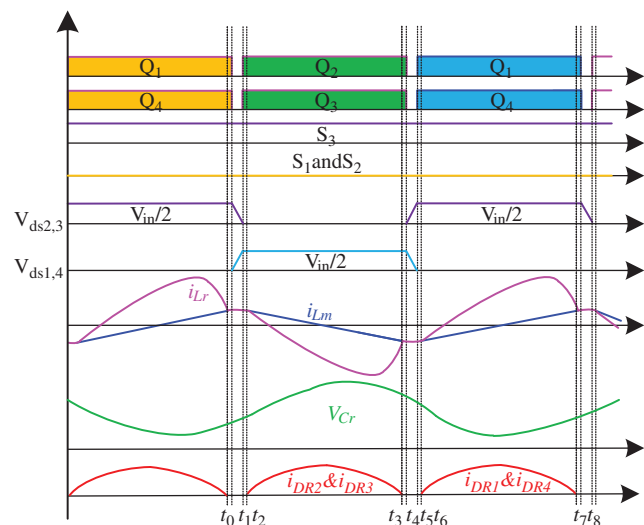**Figure 2:** ZVZCS TLHFLLC power architecture

Figure 3: Key waveforms of the ZVZCS TLHFLLC

    a) The capacity of two input capacitors in series is infinite, replaced by two $V_{in}/2$ voltage source.

    b) All power switches and diodes are ideal devices.

    c) All capacitors, inductors, and transformers are ideal devices.

    d) Output capacitance C_o is considered to be infinite and is replaced by the constant voltage source V_o.

    e) The circuit has been working in a stable state.

The switching cycle of the converter can be divided into eight stages. The main work waveform, as shown in Fig. 3, shows that the waveforms of the first half of the cycle and the second half are symmetrical. Therefore, only half of the cycle (five of the eight stages) is analyzed below, corresponding to the five equivalent circuits shown in Fig. 4. The working processes are described as follows:

Stage 1 [Fig. 4a, before t_0]: Before t_0, Q_1 and Q_4 turn on. At the same time, Q_2 and Q_3 are turned off. The resonant inductance current i_{Lr} is positive and flows through Q_1 and Q_4. The excitation inductive current i_{L_m} linearly increase due to the input partial voltage capacitance C_1 and C_2, $V_{ds2,3} = V_{in}/2$, $V_{ds1,4} = V_{in}/2$. Meanwhile, the secondary diodes D_{R1} and D_{R4} will turn off automatically due to the zero-crossing current. So, there will be almost no reverse process. This working state of the diode is defined as the zero-current switching (ZCS). The voltage spike on the diode operating in the ZCS state is almost zero. L_r, C_r, and L_m resonate together.

Stage 2 [Fig. 4b, t_0–t_1]: Turn off Q_1 and Q_4 at t_0. At this point, the resonant current i_{L_r} charges C_{oss1} and C_{oss4} and discharges C_{oss2} and C_{oss3}. Q_1 and Q_4 shut off with zero voltage due to the buffering of C_{oss1} and C_{oss4}. The resonant current i_{L_r} rises with the sine wave, and then decreases after reaching its peak, and the excitation current i_{L_m} linearly increases at the same time. When the resonant current i_{L_r} and excitation current i_{L_m} are equal, the voltages at both ends of the excitation inductance L_m are no longer clamped by the output voltage V_o. The resonant capacitor C_r, resonant inductance L_r, and excitation inductor L_m participate in the resonance, and the three-element resonance occurs. Since the excitation inductance L_m is much larger than the resonant inductance L_r, the current variation in this segment is relatively smooth, and the resonant current i_{L_r} can be regarded as a constant value. In this state, the output capacitance C_o continues to provide energy for the load R_o. The equations of i_{L_r}, V_{C_r}, and i_{L_m} are as follows:

$$i_{L_r}(t) = I_m \tag{1}$$

$$V_{C_r}(t) = V_{C_r}(t_1) + \frac{I_m(t - t_1)}{C_r} \tag{2}$$

$$i_{L_m}(t) = I_m \tag{3}$$

where I_m is the peak value of excitation inductance current, and $V_{C_r}(t_1)$ is the initial value of resonant capacitor C_r at t_1.

Stage 3 [Fig. 4c, t_1–t_2]: At t_1, the voltage of parasitic capacitance C_{oss1} and C_{oss4} of Q_1 and Q_4 rises to $V_{in}/2$, and the voltage of parasitic capacitance C_{oss2} and C_{oss3} of Q_2 and Q_3 drops to 0, At this time, Q_2 and Q_3 can be turned on with zero voltage. Since this period is short, we can approximate that both i_{L_r} and i_{L_m} remain unchanged. There is no current in the primary and secondary sides of the transformer, and the load R_o is still powered by the output capacitor C_o. The parasitic capacitance of Q_2 and Q_3 begins to discharge until its voltage becomes 0.

Stage 4 [Fig. 4d, t_2–t_3]: From t_2, the resonance current i_{L_r} and excitation current i_{L_m} begin to decline, and i_{L_r} and i_{L_m} start to become unequal. When the rectifier diodes D_{R2} and D_{R3} are conducting, as indicated by Kirchhoff's current law, the secondary diode current $i_D = n(i_m - i_r)$ flows forward from zero. The voltage on the secondary side of the transformer is clamped by output voltage V_o, and the voltage at both ends of the excitation inductance L_m is clamped to $-nV_o$ by output voltage V_o. At this time, only the resonant

capacitor C_r and resonant inductor L_r participate in the resonant cavity, when three-element resonance becomes two-element resonance. The equations of i_{L_m}, V_{C_r}, and i_{L_m} are as follows:
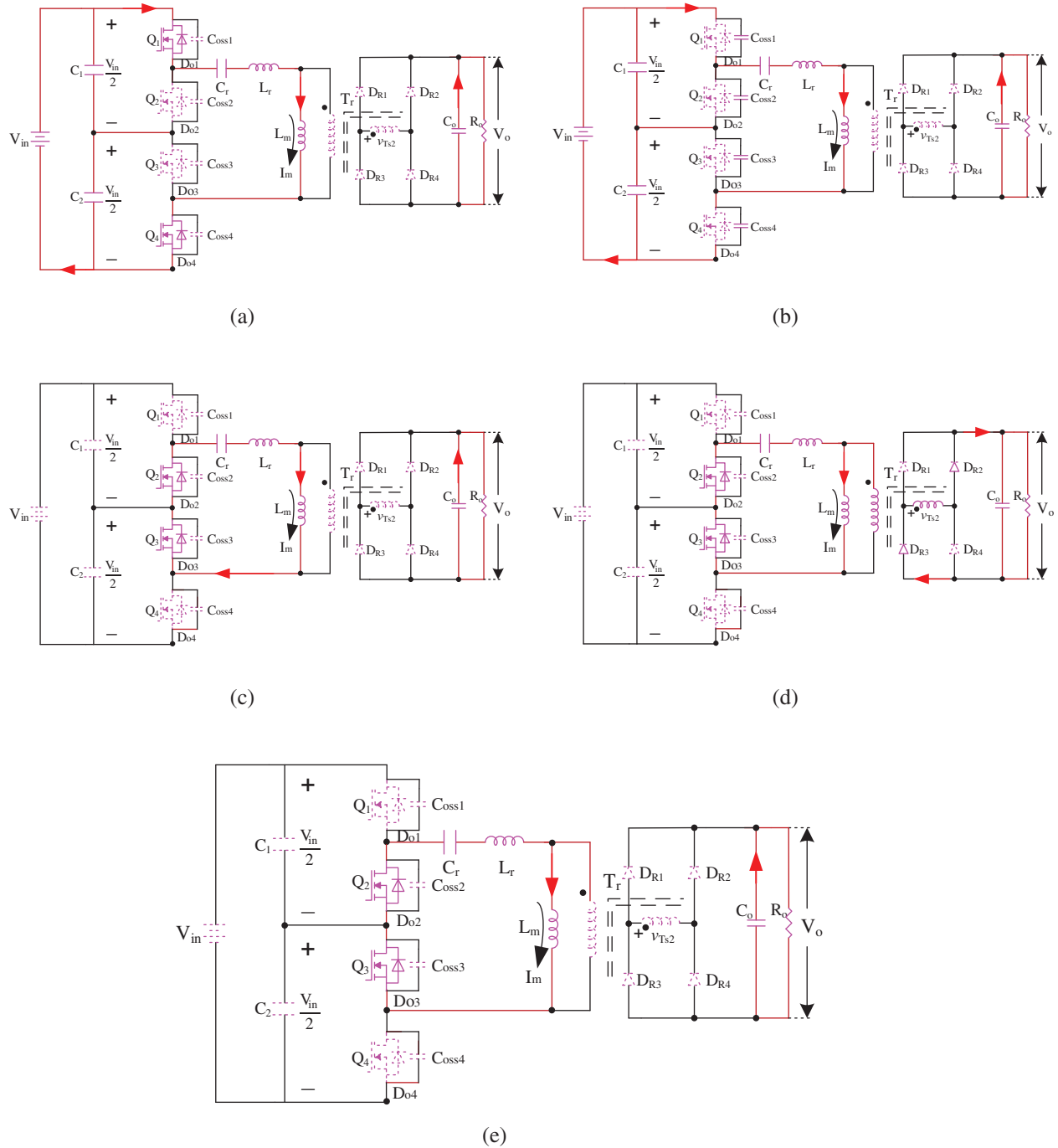

(a)

(b)

(c)

(d)

(e)

Figure 4: Equivalent circuits for different time intervals in half of the switching cycle: (a) Stage 1; (b) Stage 2; (c) Stage 3; (d) Stage 4; (e) Stage 5

$$i_{L_r}(t) = I_m \cos \omega_r(t - t_2) - [nV_o - V_{C_r}(t_1)] \sin \omega_r(t - t_2)/Z_r \tag{4}$$

$$V_{C_r}(t) = I_m Z_r \sin \omega_r(t - t_2) + nV_o + [nV_o - V_{C_r}(t_1)] \cos \omega_r(t - t_2) \tag{5}$$

$$i_{L_m}(t) = I_m - nV_o(t - t_2)/L_m \tag{6}$$

where n is the transformer primary to secondary turn ratio, $\omega_r = 1/\sqrt{L_r C_r}$, $Z_r = \sqrt{L_r/C_r}$.

Stage 5 [Fig. 4e, t_3–t_4]: When the excitation current i_{L_m} is equal to the resonant current i_{L_r} at t_3-t_4, the secondary rectifying diodes D_{R1} and D_{R4} stop conducting, realize zero-current switching (ZCS), and begin to bear the reverse voltage. During this period, resonance current i_{L_r} decreases to 0 in the positive direction and then increases in the negative direction. Thus, resonance current i_{Lr} starts to charge the excitation inductance L_m again, and the excitation current i_{L_m} linearly increases (negative).

After t_4, the first half cycle of the converter's working state ends, and the second half cycle begins. The working state of the second half cycle is symmetrical with the first half cycle (t_0-t_4), and they will not be repeated here.

2.2 100V~300V Low Line Input (Full Bridge LLC, Mode 2)

When the input voltage is low, the traditional full bridge LLC resonant converter is in work, which operates by turning on S_1~S_2 and turning off S_3. Due to the use of three-level technology, the maximum voltage of the primary side MOSFETs is only 300V, so it is unnecessary to change the type and parameters of the primary side switch. In addition, the full bridge LLC resonant converter still adopts the same parameters of the resonant cavity. Therefore, the two circuit topologies within the entire input voltage range work through the same set of circuit components, which saves costs and maximizes economic returns.

Since the operating principle and design analysis, including the optimum for ZVS parameters, have been well developed and introduced in the literature [13,14], detailed analysis of this converter has omitted for conciseness.

3 Influence of Wide Input Voltage Range on LLC Converter

As the switching frequency f_s varies closer to the resonant frequency f_r under the VF control strategy, the fundamental harmonic approximation (FHA) method is used to obtain the voltage gain characteristics [15–18]. The following is a specific derivation process.

3.1 Limitations of Voltage Gain Characteristics

The resonant network equivalent circuit of the LLC resonant converter is shown in Fig. 5. V_{in} is the basic wave of the input voltage, and R_{eq} is the equivalent resistance when the load converts to the primary side.
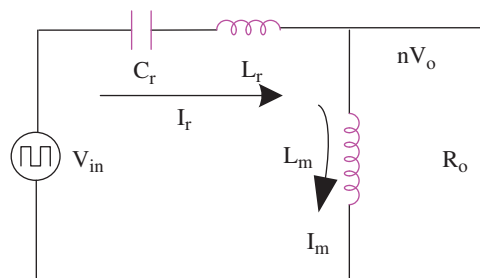

Figure 5: Equivalent circuits for resonant tank

The resonant network is composed of resonant capacitor C_r, resonant inductor L_r and transformer excitation inductor L_m, so there are two resonance frequencies f_r and f_m as shown in Eqs. (7) and (8).

$$f_r = \frac{1}{2\pi\sqrt{L_r \times C_r}} \tag{7}$$

$$f_m = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{8}$$

According to Fig. 5, the LLC resonant converter's voltage gain function is derived from the fundamental wave analysis method (FHA) as:

$$M_g = \left\|\frac{nV_o}{V_{in}}\right\| = \left\|\frac{jw_sL_m//R_{ac}}{jL_rs + j\dfrac{1}{C_rs} + jw_sL_m//R_{ac}}\right\| \tag{9}$$

$$M_g(f_n) = \frac{nV_o}{V_{in}} = \left|\frac{\dfrac{R_{ac}\cdot j\omega L_m}{R_{ac} + j\omega L_m}}{\dfrac{1}{j\omega C_r} + j\omega L_r + \dfrac{R_{ac}\cdot j\omega L_m}{R_{ac} + j\omega L_m}}\right| = \frac{1}{\sqrt{\left[1 + \dfrac{1}{L_n}\left(1 - \dfrac{1}{f_n^2}\right)\right]^2 + \left[Q\left(f_n - \dfrac{1}{f_n}\right)\right]^2}} \tag{10}$$

where L_n is the inductance ratio between magnetizing inductance L_m and the resonant inductance L_r, f_n is the normalized frequency ratio between the switching frequency f_s and resonant frequency f_r, Q is the quality factor of resonant tank, R_{ac} is the equivalent ac load resistance, and ω is the switch angle frequency.

Input impedance Z_{in} of the resonance network is as follows:

$$Z_{in}(s) = \frac{1}{C_rs} + L_rs + sL_m//R_{ac} \tag{11}$$

If the characteristic impedance Z_o is used to normalize, the input impedance Z_n after normalization can be obtained by:

$$\begin{cases} Z_o = \sqrt{\dfrac{L_r}{C_r}} = 2\pi f_r L_r = \dfrac{1}{2\pi f_r C_r} \\ Z_n = \dfrac{Z_{in}}{Z_o} = \dfrac{jL_nf_n}{1 + jL_nf_nQ} + \dfrac{1 - f_n^2}{jf_n} \end{cases} \tag{12}$$

It can be concluded from Eq. (10) that the values of each group of L_n and Q correspond to different voltage gain curves $M_g(f_n)$. If we select L_n and Q as a set of specific values, we can obtain a resonant network's voltage gain curve, as shown in Fig. 6. When the square wave voltage passes through the resonant network, the phase difference will be generated between the current and voltage waveform, enabling the switches to realize zero-voltage switching (ZVS), that is to say, the input impedance presents sensibility. The LLC working area can be divided into two parts according to the opening state of the switches (ZVS and ZCS). The peak point of the gain curve is the boundary point of ZVS and ZCS. If the imaginary part of Z_n is 0, the perceptual boundary condition of input impedance can be obtained, as shown in "ZVS boundary line" in Fig. 6, the right side of the boundary line is the region where ZVS can be realized. In the ZVS region, the regulation range of switching frequency ($f_{n\_min} \sim f_{n\_max}$) limits the value of the resonant network's voltage gain, thereby limiting the range of input voltage adaptation. In the design, the maximum voltage gain obtained at the lowest switching frequency shall meet the gain

demand at the minimum input voltage; the minimum voltage gain obtained at the highest switching frequency shall meet the gain demand at the maximum input voltage. Besides, within the ZVS region, the slope of the voltage gain curve decreases with increasing f_n, which means that the regulating range of switching frequency extends with increased input voltage. A high switching frequency is required to obtain a small enough voltage gain to maintain the output voltage's stability during the high voltage input. In practice, switching frequency is often limited by switching devices. The over-high frequency will also bring problems such as switching loss, voltage and current waveform oscillation, and electromagnetic interference (EMI), which is another essential factor to limiting the input voltage range.
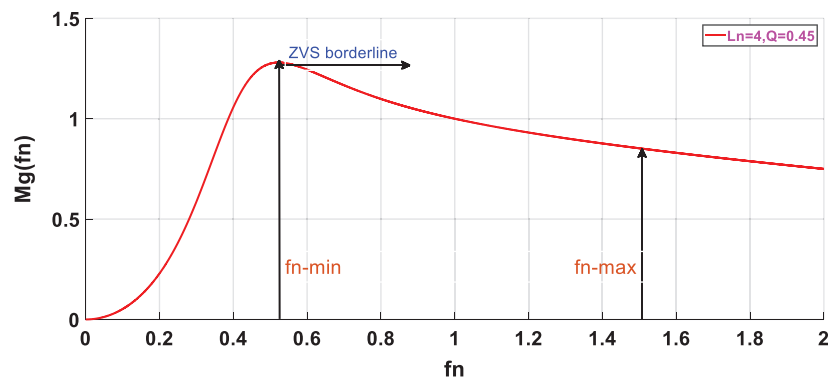

Figure 6: The voltage gain curves of resonant tank under L_n and Q

3.2 Influences of L_n and Q on Voltage Gain Characteristics

According to Eq. (10), the resonant network's voltage gain of the LLC converter is affected by L_n and Q, determining the input voltage range of the converter. Therefore, it is necessary to select an appropriate L_n and Q to meet the requirements of the adaption range of the input voltage in the design. Fig. 7 shows the resonant network voltage gain curve with the same L_n and different Q. According to this Fig. 7, in the region of $f_n < 1$, the voltage gain increases with decreasing Q. The maximum gain also increases, so that the resonant network can adapt to a smaller input voltage. However, in the region of $f_n > 1$, the voltage gain increases with decreasing Q. The slope of the gain curve becomes smaller, which means that with decreasing Q, the adjustment range of switching frequency becomes larger and larger during the high voltage input. Meanwhile, the minimum voltage gain obtained at the highest switching frequency becomes larger, and the upper limit of the input voltage adaptation range decreases.
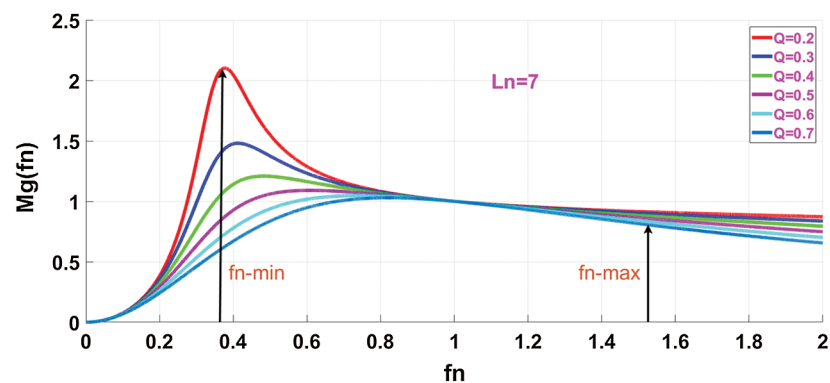

Figure 7: The voltage gain curves of the resonant tank under different Q

Fig. 8 shows the voltage gain curve of the resonant network under the same Q and different L_n. As can be seen from Fig. 8, in the region of $f_n < 1$, voltage gain increases with decreasing L_n, and the maximum gain also increases, so that the resonant network can adapt to a smaller input voltage. In the region of $f_n > 1$, the voltage gain decreases with decreasing L_n; the slope of the gain curve increases with the decrease of L_n. It shows that with decreasing L_n, the frequency adjustment range of the high voltage input becomes smaller, and the minimum voltage gain obtained at the maximum switching frequency becomes smaller, so that the resonant network can adapt to the higher input voltage.
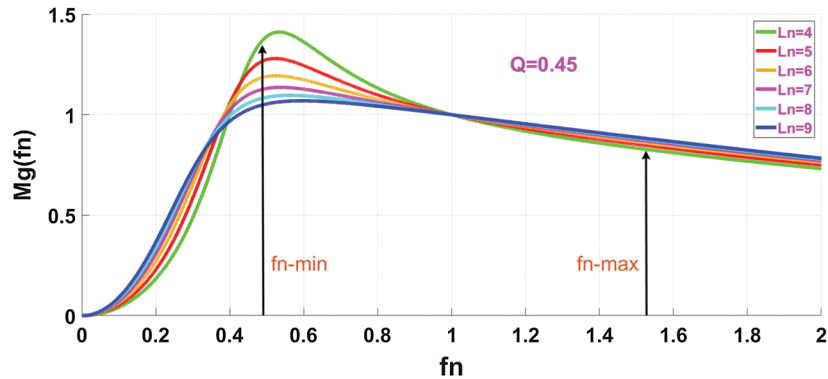

Figure 8: Voltage gain curves of the resonant tank under different L_n

On the whole, using a small Q can only expand the lower limit of the input voltage range, but not the upper limit. So, reducing Q to expand the input voltage range of the LLC converter is not considered. Therefore, it is often used to reduce L_n in the design to expand the upper and lower limits of the input voltage range for the LLC converter.

Based on the above theoretical analysis, it is concluded that the adjustment range of resonant frequency $(f_{n\_min} \sim f_{n\_max})$ determines the effective range of the resonant network's voltage gain $(M_{g\_min} \sim M_{g\_max})$. In the design, the maximum voltage gain of the resonant network should meet the requirement of the minimum input voltage of the resonant network, and the minimum voltage gain should meet the requirement of the maximum input voltage. The LLC converter was designed with a small L_n to acquire a wide input voltage range while maintaining high efficiency.

4 Parametric Consistency Design for the Polymorphic Topology LLC Resonant Converter

The design of the resonant cavity's parameters of the LLC resonant converter includes the resonant inductor L_r, the resonant capacitor C_r, and the excitation inductor L_m. For the polymorphic topology LLC resonant converter proposed in this paper, it needs to meet the following two requirements: (1) Adaptation to a wide input voltage range; (2) Soft switching realization within the full load range (ZVS at the primary MOSFETs and ZCS at the secondary diodes). The LLC converter's parameters need to be defined before designing, such as input and output voltage ranges, the maximum output power, and the resonance frequency. Therefore, the input voltage range is 100V~600V, and the nominal value is 300V. The output voltage and maximum output power are 48V and 500W, respectively. In this design, the resonant frequency f_r is selected to be 180 kHz. The following are the step-by-step design procedures illustrated in Fig. 9.

Before it is designed, the initial parameters of the LLC resonant converter should be defined, such as the input and output voltage range, the maximum output power, and the maximum resonant frequency. Then, the

input voltage of the LLC converter varies from $V_{in\_min} = 100V$ to $V_{in\_max} = 600V$, with a nominal value of $V_{in\_nom} = 300V$. In this design, $f_r = 180kHz$ was chosen.
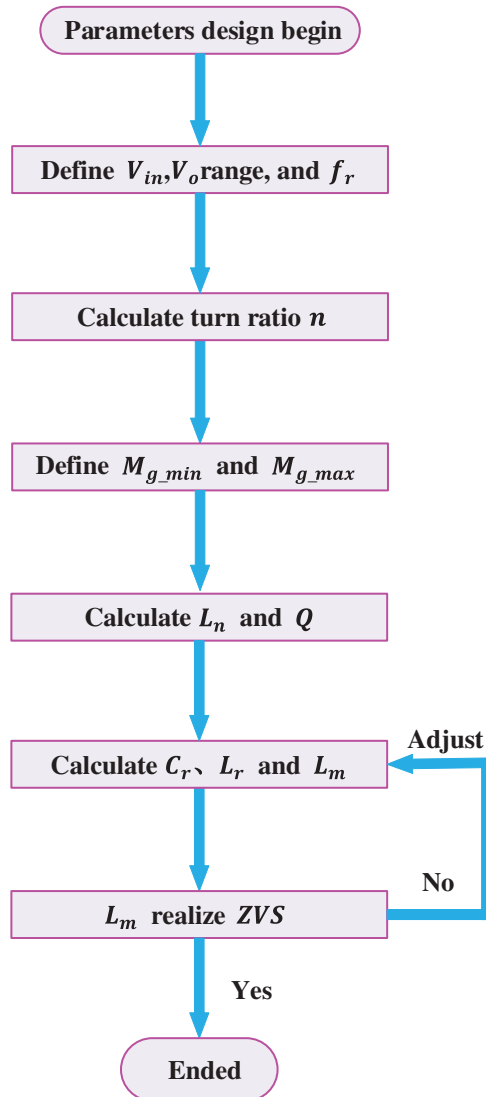

Figure 9: Flow chart of LLC parameter design

a) Selecting the Transformer Turns Ratio n

Due to gain of the LLC resonant converter being constant at 1 for f_r and independent of load, its resonance gain was set to 1, enabling a freer design of resonance parameters and leaving more space for the design of the LLC resonance parameters. Under the premise of realizing soft switching, the switching frequency will be lower, the loss will be less, and the working efficiency will be higher.

The transformer turns ratio should be selected at the resonant frequency, where the gain is unity. It can be calculated as:

$$n = M_g \times \frac{V_{o\_nom}}{V_o + V_F} \tag{13}$$

where V_F is the diode voltage drop of the output rectifier.

b) Define Maximal and Minimum Voltage Gain

After the theoretical turn ratio was determined, the maximum and minimum voltage gains were calculated according to the input voltage range to ensure that the output voltage can be adjusted.

$$M_{g\_min} = n \cdot \left(\frac{V_o + V_F}{V_{in\_max}}\right) \tag{14}$$

$$M_{g\_max} = n \cdot \left(\frac{V_o + V_F}{V_{in\_min}}\right) \tag{15}$$

c) Calculating L_n and Q

The resonant cavity parameter design of the LLC resonant converter includes resonant inductance L_r, resonant capacitor C_r, and excitation inductance L_m. The inductance ratio L_n and quality factor Q determine the magnitude of them, so the design of the resonant cavity's parameters is about to select the values of L_n and Q. From previous research regarding voltage gain characteristics under VF mode, the selection of the parameters L_n and Q directly influence the converter's input voltage range. Therefore, based on the traditional design method of parameters, this paper will present the influence of the critical parameters L_n and Q on the gain curve. Then, combined with an index system for key parametric value restrictions, we will select a reasonable set of parameters, verified by back substitution equations, and constantly optimized, to finally determine L_n and Q. In this design, we have assigned $L_n = 7$, $Q = 0.45$.

d) Calculating C_r, L_r, and L_m

The resonant capacitor value is given by:

$$C_r = \frac{1}{2\pi Q f_r R_{ac}} \tag{16}$$

Once the value of the resonant capacitor is determined, the resonant inductor value and the transformer magnetizing inductor value can be calculated by using Eqs. (17) and (18).

$$L_r = \frac{1}{(2\pi f_r)^2 C_r} \tag{17}$$

$$L_m = L_n \times L_r \tag{18}$$

e) ZVS Requirements

To achieve ZVS at f_r with a duty cycle of 0.5, L_m must meet the inequality Eq. (19). If it is not satisfied, the dead time in Eq. (19) should be set again or, the aforementioned design should be tuned.

$$L_m < \frac{nV_o t_{dead}}{4 f_r V_{in\_max} C_{oss\_pri}} \tag{19}$$

where C_{oss_pri} is the equivalent output parasitic capacitor of primary switches, and t_{dead} is the dead-time of upper and lower switches.

Based on the above steps, the most reasonable resonant parameter values have been finally obtained. The wide input adaptability of the novel polymorphic topology LLC resonant converter will be verified in the following experiments.

5 Implementation Scheme of Polymorphic Topology Switching Control Strategy

Since the circuit topology of hybrid mode LLC is different under different input voltages, an appropriate topology switching strategy is needed to make the LLC switch between different topologies. Besides, the strategy will prevent the circuit from producing excessive impact oscillation, which will create an unstable system or destroy the circuit. Since the topologies of the three-level half bridge and the full bridge circuit are derived from the full bridge topology, no additional devices are necessary, and the switching between topologies can be realized by using its own MOSFET as the switch, which reduces the cost. In circuit simulation, devices usually start when the input voltage exceeds a certain switch point. However, in practice, due to the ripple or sudden change of input voltage, the switching signal will continuously oscillate. To avoid this situation, we must set a certain difference in the switching voltage. For the polymorphic topology introduced in this chapter, there are two switches in it. The first is the switching between full bridge variable frequency control and full bridge constant frequency control, and the second is the switching between full bridge constant frequency control and half bridge variable frequency control.

This section will introduce the control strategy and solution of the polymorphic topology control circuit shown in Fig. 10, which implements two operating modes of the converter at different input voltage levels to improve the wide range adaptability of the LLC converter.
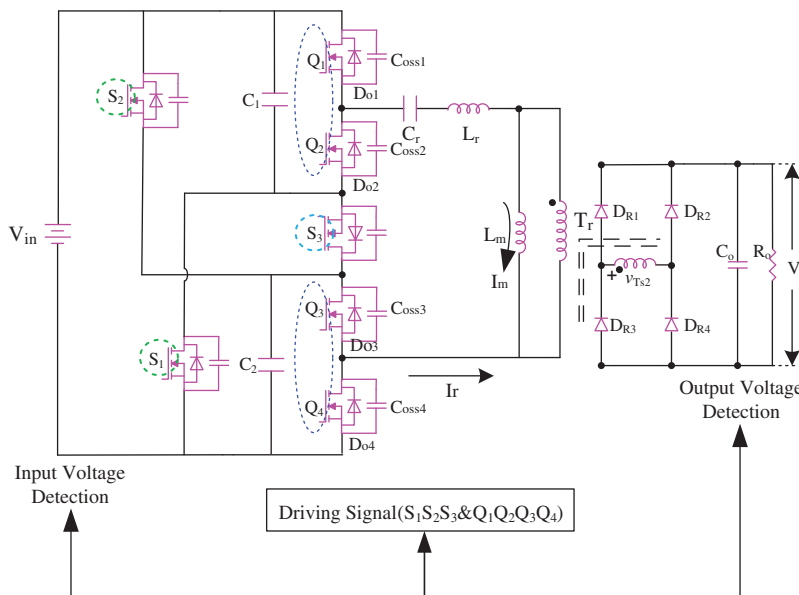

Figure 10: Polymorphic topology control circuit

Usually, polymorphic mode switching circuits rely on switches. Conventional switches are hardware latches and relays. These two kinds of switches have shortcomings: The hardware latch needs an inconvenient manual operation, and the speed of relay switching is too slow to withstand pressure and volume conflict. Besides, the durability of the relay's contact is inferior, and its maintainability is poor. The polymorphic topology circuit studied in this paper uses MOSFETs of the circuit itself as the

switches. It does not need to add an additional auxiliary circuit, reducing the number of components to a minimum while maximizing cost-effectiveness.

In general, once the input voltage exceeds the voltage of the settled switching point, the circuit should be immediately activated. If the circuit is reconfigured, the energy stored in the circuit components will not be released. So, the extreme high dv/dt and di/dt may occur during the switching process. To eliminate this negative impact, we need to develop a more flexible control strategy. The proposed control strategy in this paper adopts the concepts of cutting off power input, outputting energy consumption, and topological switching. For example, when the converter circuit is switched from full bridge LLC to three-level half bridge LLC, the switching process is divided into three stages: 1) $S_1 \sim S_3$ and $Q_1 \sim Q_4$ are simultaneously turned off to be isolated from the input power; 2) Then wait until the output load consumes up the energy stored in the circuit; 3) Finally, open S_3 and $Q_1 \sim Q_4$ at the same time. The whole switching process will be completed. The entire switching process takes time, but the output capacitance C_o is large enough to power the output load R_o. In practice, a hysteresis comparison link should be added to the detection of switching point voltage to avoid incorrect switching of the converter's operation mode caused by detection error.

5.1 Generation of the Drive Signal

For the analog circuit, the generation of switching action of polymorphic topology is quite complicated. The original drive signal must be stopped, and a new drive signal must be generated. In this paper, DSP is adopted for full digital control to sample and monitor the input voltage. When the input voltage is lower than the set value, full bridge LLC topology is adopted; when the input voltage rises to a certain level, the topology switches to a three-level half bridge LLC. The specific generation mode of the drive signal is as follows:

The time-varying sawtooth pulse is generated by the period counter (TBCTR), and the enhanced pulse width modulation module ePWM1 (EPWM1A, EPWM1B) is used to control Q_1 and Q_2, the ePWM2 (EPWM2A, EPWM2B) is used to control Q_3 and Q_4, and the ePWM3 (EPWM3A, EPWM3B) and ePWM4(EPWM4A) are used to control S_1, S_2, and S_3, respectively.

The whole control process is divided into two parts: When the topology of the converter's circuit is in the full bridge or three-level half bridge, ePWM1 and ePWM2 generate drive signals as shown in Fig. 11a respectively, and the driving signals of the tube are consistent at this time. When the circuit topology is switching, the drive signal shown in Fig. 11b is implemented to generate permanent on and off signals.
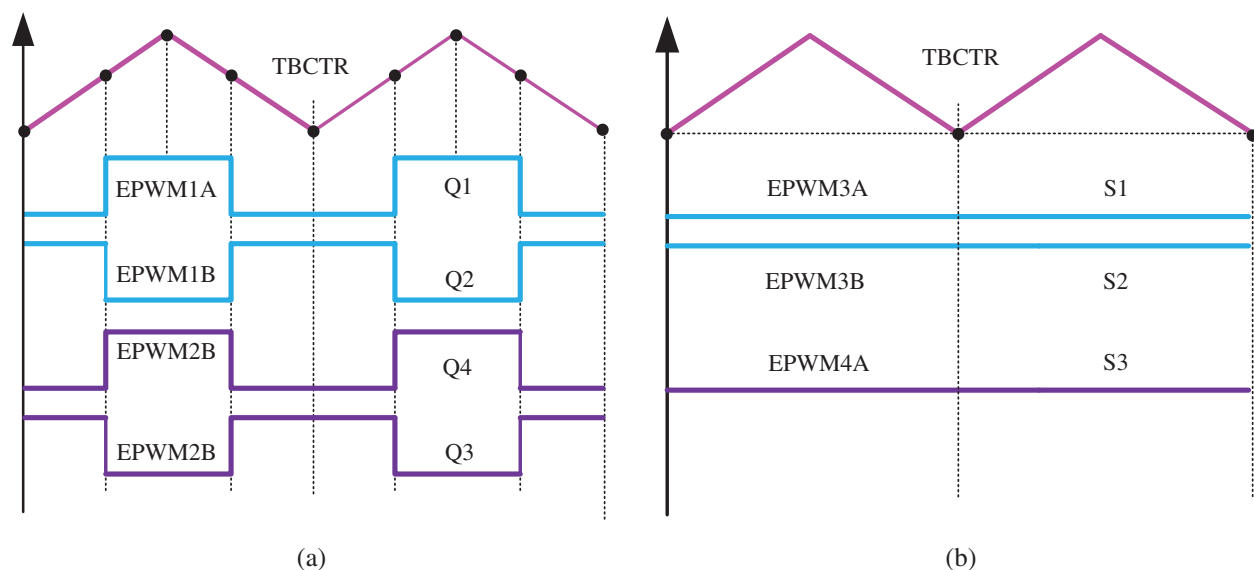

(a)   (b)

Figure 11: Principles of generating driving signal. (a) Driving signals for $Q_1 \sim Q_4$ and (b) Driving signals for $S_1 \sim S_3$

5.2 Analysis of Switch State in the Process of Changing Topology

Q_1, Q_4 and Q_2, Q_3 form two pairs of bridge arms, respectively, in the primary circuit of the converter. The bidirectional fluidity of resonant current i_{Lr} enables two switches to simultaneously conduct for each working state. Suppose "1" and "0" are used to indicate the state of on and off, respectively. In that case, we will acquire the switching state of LLC converter shown in Tab. 1, considering that two switches of the same bridge arm cannot be connected at the same time, so S_1, S_2, and S_3 of different circuit topologies cannot also be concurrently connected.

Table 1: Driving states of the LLC converter

Status	S_1	S_2	S_3	Q_1	Q_2	Q_3	Q_4	V_d
1	1	1	0	1	0	0	1	V_{in}
				0	1	1	0	$-V_{in}$
2	0	0	1	1	0	0	1	V_{in}
				0	1	1	0	$-V_{in}$

When the switches are driven alternately according to the status 1 in Tab. 1, the circuit topology of the converter is full bridge LLC converter, and there are two kinds of input voltage V_{in} and $-V_{in}$ in the resonance network; When the switches are driven in status 2 in Tab. 1, the circuit topology of the converter is a three-level half bridge LLC converter, and there are also two kinds of input voltage V_{in} and $-V_{in}$ in the resonance network. In the two circuit topologies, the resonant network has the same input voltage. The LLC converter works in multi-levels mode, which also conforms to the consistent design requirements of LLC resonant parameters described above. Experimental results show that the topology switching control strategy is practical and straightforward.

6 Hardware Prototype and Experimental Verification

In this paper, hardware implementation of the prototype was carried out in the laboratory. A photograph of the experimental prototype and setup is shown in Fig. 12. A 500W experimental prototype, suitable for renewable energy sources and with the adoption of the proposed polymorphic topology control strategy for an ultra-wide input voltage range, has been established to verify analysis in this paper. The specification and main parameters used by the experimental prototype are summarized as follows: the input voltage is 100V~600V, the output voltage is 48V, and the maximum output current is 10.5A. The turn ratio of transformer is 18:6, which means the LLC resonant converter works in the stable condition at the ideally input voltage of 300V. The detailed design criteria are listed in Tab. 2.

A prototype converter was built and tested in the lab to verify the proposed method. The resonant frequency was chosen to be high to reduce the parasitic effects in the circuit. The experimental waveforms of a proposed converter are shown in Figs. 13a–13c. Most of the results have similarities with simulated and theoretical calculations. Fig. 13 shows the experimental waveforms of the Q_1 drive voltage (V_{GS1}), the voltage across Q_1 (V_{DS1}), resonant tank current (I_{Lr}), and resonant capacitor voltage (V_{Cr}) at $V_{out} = 48V$. As shown in Fig. 13a, the switching frequency $f_s = 78kHz$. The waveforms in Fig. 13b are given at $P_o = 100W$. Fig. 13c presents the waveforms at the maximum input voltage, while operating at the maximum frequency.

It can be seen from Fig. 14 that all primary side MOSFETs can achieve ZVS in the full load. The switches turn on in ZVS condition and turn off at a very low current. Therefore, the high frequency turn-on switching losses become negligible. There are no significant voltage spikes across the switches, which signify the ZVS turn-off transition. The MOSFET becomes switched off completely before the drain to

source voltage rises above zero. Due to ZVS, the losses of turn-off transition are reduced to a very small value. It is also seen that the voltage stress of the primary switches is half of the input voltage. This is because the low voltage rated MOSFET with low $R_{DS(on)}$ is employed to reduce conductivity losses.

Figure 12: Experimental setup

Table 2: Utilized components and parameters in the prototype

Components	Parameters
Input Voltage: $V_{in\_nom}(V_{in\_min} \sim V_{in\_max})$	300V (100V~600V)
Output Voltage: V_o	48V
Output Power at 48V: P_{o_nom}	500W
Output Current at 500W: I_{o_nom}	10.5A
Resonant Frequency: f_r	180 kHz
Maximum Switching Frequency: f_{max}	127 kHz
Ratio of L_m to L_r: L_n	7
Quality Factor: Q	0.45
Controller	TI's TMS320F28335,150MHz@Digital Signal Processor
Primary Switches: S_1~S_3 and Q_1~Q_4	Vishay Siliconix's IRFPC50PBF 650V,11A,$R_{DS(on)} = 0.60\Omega$

Table 2 (continued).

| Components	Parameters
Secondary Diodes: $D_{R1} \sim D_{R4}$	Vishay Siliconix's IRFPC50PBF 400V,60A
Transformer: T_r	TDK's PQ40/40-PC95 ferrite core Primary side series connection: Primary turns 3×18, 0.35 mm@TIW-B Secondary side series connection: Secondary turns 5×3, 0.35 mm@TIW-B; Magnetizing inductance:84uH
Resonant Capacitor: C_r	62nF,Faratronic's CBB capacitor 1000V
Resonant Inductor: L_r	12.6uH,TDK's EE42/20-PC95 ferrite core 5*8, 0.35 mm@TIW-B
Input Capacitor: $C_1 \sim C_2$	Samyoung's Electrolytic capacitor 550V, 2200uF
Output Capacitor: C_o	680uF,Nichicon's Electrolytic capacitor 100V, Qty:4
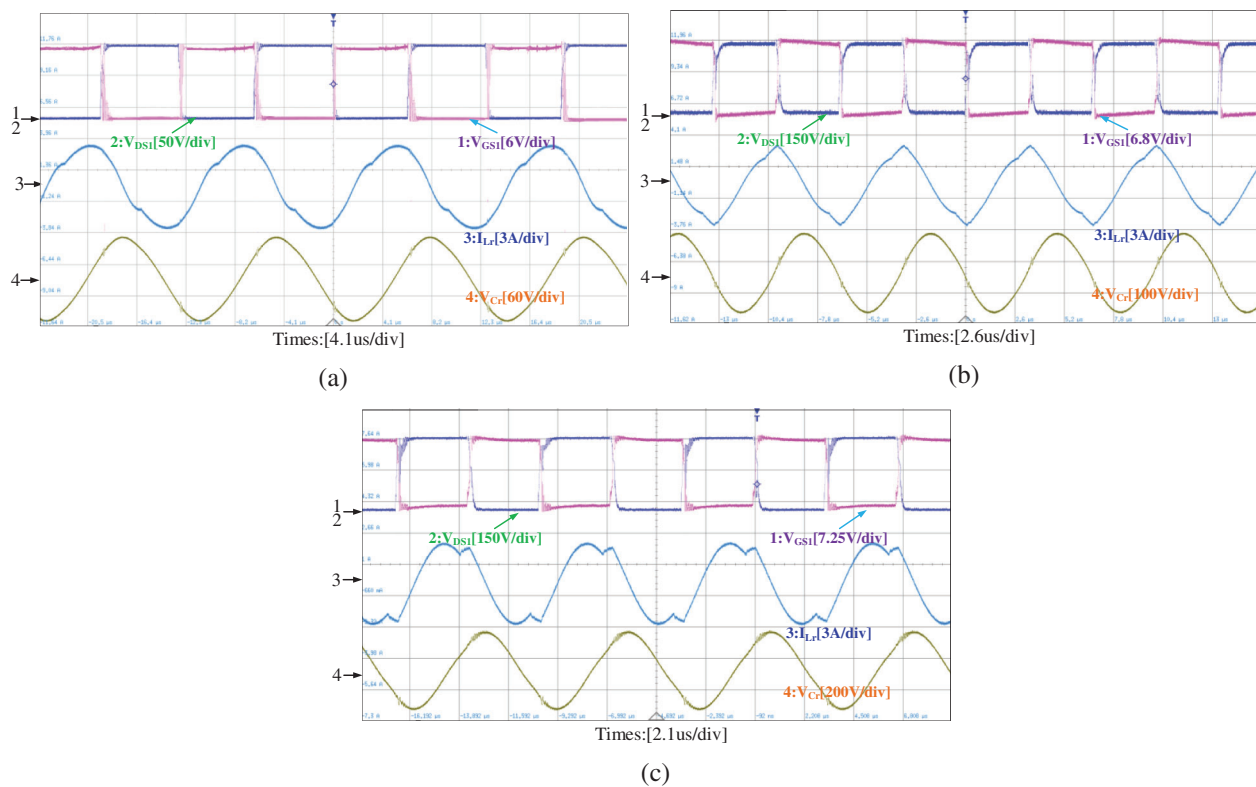
Figure 13: Experimental results with different input voltages: (a) Waveforms under input voltage 100V condition (V_{GS1}[6V/div], V_{DS1}[50V/div], I_{L_r}[3A/div], V_{C_r}[60V/div]); (b) Waveforms under input voltage 300V condition (V_{GS1}[6.8V/div], V_{DS1}[150V/div], I_{L_r}[3A/div], V_{C_r}[100V/div]); (c) Waveforms under input voltage 600V condition (V_{GS1}[7.25V/div], V_{DS1}[150V/div], I_{L_r}[3A/div], V_{C_r}[200V/div])

The efficiency curve of the system with different input voltage is shown in Fig. 15. The experimental result was obtained by HIOKI PW6001, where the full load was 500W. The overall efficiency of the converter is ideal, and peak efficiency can reach 92%.
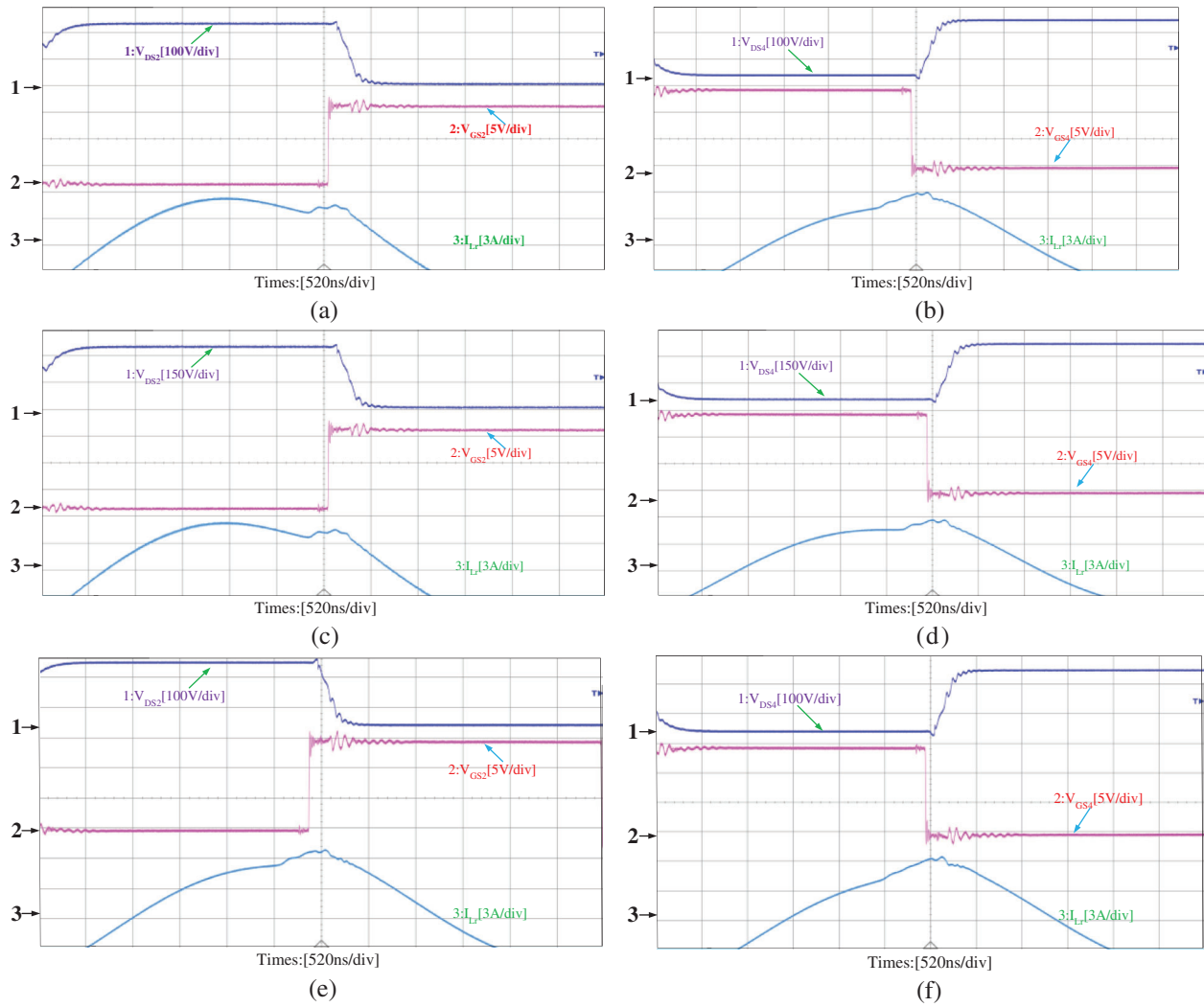
Figure 14: ZVS waveforms of switches Q_2 and Q_4 with the converter at full load: (a) $V_{in} = 200V$, waveforms of Q_2; (b) $V_{in} = 200V$, waveforms of Q_4; (c) $V_{in} = 300V$, waveforms of Q_2; (d) $V_{in} = 300V$, waveforms of Q_4; (e) $V_{in} = 400V$, waveforms of Q_2; (f) $V_{in} = 400V$, waveforms of Q_4
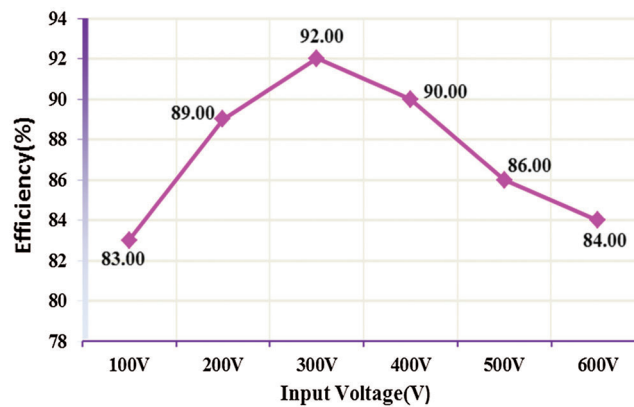

Figure 15: Efficiency curve of the prototype

7 Discussions and Conclusions

Currently, research literature is often focused on extending the input voltage range with higher efficiency, decreasing components count, and system complexity, and minimizing size, weight, losses, and stresses of component. To evaluate the characteristics of the proposed polymorphic topology, the performances of the proposed method and other different kinds of control techniques in recent years have been compared, as summarized in Tab. 3.

Table 3: Performance comparison of recent studies

Item	[19] 2013	[20] 2016	[21] 2017	[22] 2017	[23] 2018	[24] 2018	This work 2020
Circuit topology	Full, Half Bridge LLC	Dual Active Bridge(DAB) LLC	Full, Half Bridge LLC	Full Bridge LLC	Full Bridge CLL	Full Bridge LCC	Three Level Half Bridge LLC, Full Bridge LLC
Control strategy	Variable Frequency	Frequency Adaptive Phase Shift Modulation (FAOSM)	Variable Frequency, Phase Shift	Variable Frequency, Phase Shift	Variable Frequency, Phase Shift	Variable Frequency	Variable Frequency
Switching count	$4 \times$ MOSFETs $2 \times$ Diodes	$6 \times$ MOSFETs	$4 \times$ MOSFETs $2 \times$ Diodes	$4 \times$ MOSFETs $2 \times$ Diodes	$4 \times$ MOSFETs $4 \times$ Diodes	$4 \times$ MOSFETs $4 \times$ Diodes	$7 \times$ MOSFETs $4 \times$ Diodes
Voltage stresses of component	Input Voltage, V_{in}	Input Voltage, V_{in}	Input Voltage, V_{in}	Input Voltage, V_{in}	Input Voltage, V_{in}	Input Voltage, V_{in}	Half of Input Voltage, $V_{in}/2$
Input voltage	20V~80V	200V~400V	20V~120V	100V~200V	200V~400V	420V~640V	100V~600V
Efficiency	96%	N.A.	95.7%	96%	94%	NA	92%
Operation range with high efficiency	Narrow	Medium	Narrow	Narrow	Medium	Medium	Wide
System complexity	Medium	High	High	High	High	High	Simple

Note: N.A. = Not Applicable.

Tab. 3 shows the comparisons with other relevant literatures, while also showing the features and advantages of our work. Hence, through comparison and analysis, the novel polymorphic topology, was shown to be suitable for ultra-wide input voltage range applications.

In this paper, a novel LLC resonant converter with polymorphic topology and hybrid control strategy was proposed, for suitability in ultra-wide input voltage range applications. The novel polymorphic topology integrates the three-level half bridge LLC and the full bridge LLC. With the same set of circuit elements, the converter automatically changes its internal circuit topology according to the input voltage. In the wide input voltage and full load range, the converter has a narrow operating frequency range. All primary side MOSFETS can realize zero-voltage switching (ZVS), and the secondary side rectifier diodes can realize zero-current switching (ZCS). The polymorphic topological control strategy's performance was verified by a 500W power prototype with 100V~600V input voltage and 48V output voltage, whose full load conversion efficiency reached 92%. All theoretical analyses and characteristics of the novel polymorphic topology with hybrid control strategy based LLC resonant converter were verified by an experiment with a maximum and minimum input voltage ratio of 6. Therefore, the novel LLC resonant converter with polymorphic topology and hybrid control strategy is very suitable for ultra-wide input voltage range applications, like renewable energy sources. In future studies, more sophisticated control methods should be introduced to improve the converter's input voltage immunity.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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