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Design of a System to Generate a Four Quadrant Signal at High-Frequency

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ABSTRACT

In order to research biological cells, a well-established physical method can be used, that is electrorotation. To achieve electrorotation system, a signal oscillator or a signal generator is always needed. The signal generator is used for generating signals with phase shift and transfers it to the electro chamber. The frequency range of the output signal is generally between 20 Hz to 100 MHz for the signal generator, but for high frequency range, like 100 MHz to 1 GHz, the signal generator is hard to control and the linear properties for the output signal is not good enough to do the electrorotation. So design a signal generator to generate a signal with high frequency range is indispensable, and this is good for researching the biological cells in high frequency environment. The project finished by doing research for some available signal generators, like Phase-Locked Loop (PLL) and Direct Digital Synthesis (DDS), and the final system with high frequency output signal has been designed after the research. The frequency range of the output signal is between 100 MHz to 1.35 GHz, and the phase shift is 90 degree for the four output signals. The system finally designed is based on analogue circuit, all of the system blocks are designed in Cadence virtuoso software and the CMOS technology is 0.35um. It will affect the big data collection, processing and storing the result of the formation of the entire process

KEYWORDS

Phase-locked loop; direct digital synthesis; four quadrant signal; high-frequency

1. Introduction

1.1. Motivation

In order to research biological cells and study structure or physiology, some well-established physical methods can be used, like patch clamping, impedance measurement electron microscopy and so on. Electrorotation is one of these methods, and through this method we can measure the geometrical and electrical properties of individual cells without destroying the cells' structure. There are many applications of electrorotation, for example; it can be used to measure the geometrical properties of individual cells, and in different frequency fields, cells can be separated with each other by using the electrorotation technology, like different kinds of cells in our blood, and this is always used in medical industry.

To achieve electrorotation, a rotating field is needed. It is generated by using four electrodes positioned at right angles to each other and energized with phase-quadrature signals whose frequency is between 50 Hz to 1 GHz. Based on this, a system which generates phase-quadrature signals is chosen to design.

1.2. Aims

The main aim of this project is to design a signal generator, which looked at high frequency range. The frequency range of the output signal is desired between 100 MHz and 1 GHz, these four output signals should have 90 degrees phase shift with each other and their frequencies are all the same. The finished system design should as better as occupied in a single chip, and this is considered for power consumption and design cost. To achieve these two requirements, many methods can be used, like Phase Locked Loop (PLL), Direct Digital Synthesis (DDS), and some other structures with CMOS-level analogue circuits' combination. The research and the design will according to the requirements and these workable methods (PLL and DDS) will be compared with each other, then the final system of this project will be designed.

The design and test bench for all system blocks are in the software CADENCE, with CMOS 0.35um technology and design library PRIMILIBRF, analogueLib. The transistor used with all NMOS transistor and the component symbol is available in library PRIMILIBRF with name "nmos4". All "VDD" and "GND" components used in the design circuit are available in library analogueLib, generally the value of "VDD" is 3.3 V, "GND" is 0 V.

2. Background research

2.1. Dielectrophoresis

Dielectrophoresis, or DEP is a kind of phenomenon, which defines a force drives to dielectric particle when the dielectric particle passing through or existing in a non-uniform electric field. This kind of force does not affect the properties of dielectric particle, and dielectric particle also cannot be charged by the force. All of particles exhibit this kind of phenomenon when passing through or existing in a non-uniform electrical field by Park et al. (2012) and Fuhr, Glaser, and Hagedorn (2013). In addition, Pedro Pohl (1999) and Nicholas, Samueli, and Kim (1998) has proposed, the strength of this force depends on the medium type, properties of the particle, the shape and size of the particle and the frequency of

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the electric field. Consequently, an accurate or suitable electric field frequency can manipulate the movement of the particle greatly. So this property of dielectrophoresis can be used to achieve some applications and developments for biological cells by Tierney, Rader, and Gold (1991), for example; use suitable electric field frequency can manipulate dielectrophoresis force to do separation for biological cells, or do electrostatic rotation in the electric field.

There are many types of effective multiples for the particle, like dipole, quadruple, and so on. These classifications and designations are created for calculating the electric field force and torque on particle much more conveniently by Ponce, Molina, and MacCleery (2013) and Holzel and Lamprecht (2012). When a particle existing in a non-uniform electric field, the dipole moment will induce in the particle. This is because, when the particle is in a non-uniform electric field, the boundary of the particle will generates positive and negative charges,+q and –q. Behrhorst (1993) has proposed, Because of the electric field is non-uniformed, so the number of positive and negative charges on the particle surface is not uniformly distributed. In this reason, if the electric field is non-uniform, the particle will be unbalanced in this field, because of the force on each side of particle will be not same, in another word, a phenomenon will happen on this particle, which is dielectrophoresis by Jones and Washizu (1996) and Understanding Direct Digital Synthesis (DDS), 2013.

2.2. Electrorotation

Based on the last section, we know that when a particle passing through or existing in a non-uniform electric field, the particle will exhibit a phenomenon, which called dielectrophoresis. And if this electric field is applied for doing rotation, the particle will exhibit another phenomenon, which is called electrorotation. Electrorotation means that when a polarized particle placing in a rotating electric field, it will do a circular movement, called electrorotation. In another word, this rotating electric field applies a torque among this field and the dielectric particle in electric field is exhibited by this torque to do rotation movement.

For a dielectric particle placed in a non-uniform electric field, the particle will be induced by electrophoretic force and became a dipole electric particle, in this moment, we called dipole moment. This particle will produce potential in this electric field, which called electrostatic potential.

2.3. Signal generator

A four quadrant signal generator acts as an important part in the whole system, it generates four sine signals, for example; with different phases and quadrature with each other, it means every signal should has 90 degree phase difference, but the amplitude and frequency is same as input signal. Because of different particles having different properties, and measure requirements are different, the frequency of these signals should among a frequency range, not a single frequency value. Generally, a measure environment or electric field is required with frequency range of 1 MHz to 1 GHz, different frequencies will be used in different situations, and the design of signal generator will become much more difficult when the frequency becomes higher. This is because when frequency grows up, the output signal is hard to control, it will cause a distortion very easily and cannot do phase shift for signals. Therefore, design a signal generator with high frequency is most importantly and useful. Nowadays, many kinds of signal generators are designed to use in this system, for example; Phase Locked Loop (PLL), Direct Digital Synthesis (DDS), and so on. These two signal generators will be introduced in next chapter.

3. Design process of system

After doing the research of PLL and DDS systems, some new ideas came out for doing the design. In order to build a system to generate four signals with 90 degree phase shift, the simplest way is using one kind of technology to achieve, like digital technology or analogue technology, but not the combination of both. So I choose analogue technology to achieve the system. By using some basic analogue CMOS circuits, like differential pair and amplifier, the phase of the signal can be rotated and changed by 180 or 90 degrees. Then we can use a frequency doubler and frequency divider to control the frequency of the output signal, and also can achieve the function of four signals' output. In this chapter, I will introduce the system, which is designed in this project, and also analysis the function for each block, thus my design can be displayed in detail.

3.1. Initial idea

The block diagram of my initial design is shown in Figure 1.

As the diagram shows, one signal with 100 MHz (for example) inputs to the frequency doubler, the frequency will be doubled for the signal and goes into the LN single to differential amplifier. After that, two 200 MHz differential signals whose phase differences are 180 degree will be generated. Then these two differential signals will drop into frequency divider, which can divide the frequency into 100 MHz again, and this divider is constructed by two D-latches, when required to generate four signals with 90 degree phase difference, this structure is necessary. Each one of the D-latch outputs are two differential signals, first D-latch generates two signals whose phase are 0 degree and 180 degree, second D-latch generates two signals whose phase are 90 degree and 270 degree. The result will be shown and analyzed in next chapter.

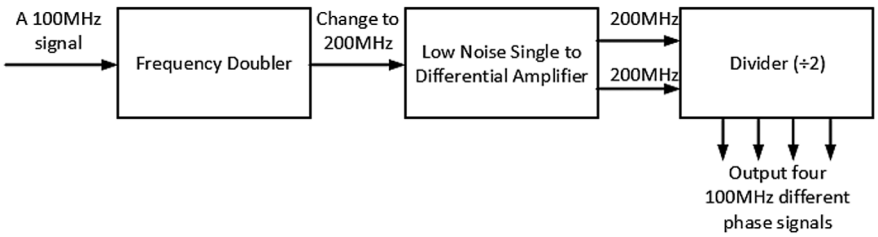

Figure 1. Initial design block diagram, with three blocks, can achieve the basic functions.

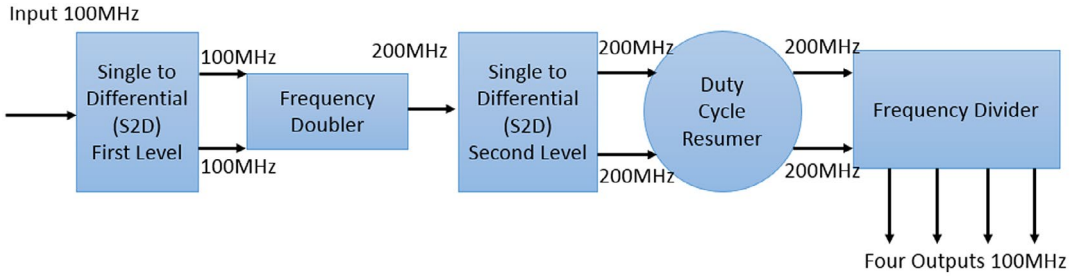

Figure 2. Advanced design system, it is based on the initial design block diagram; two new blocks are added in.

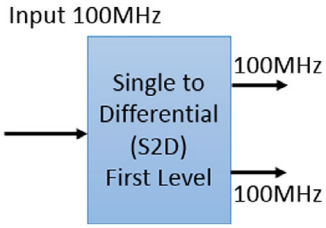

Figure 3. Block diagram of S2D, with input 100 MHz signal, the output signal are two differential signals with 100 MHz.

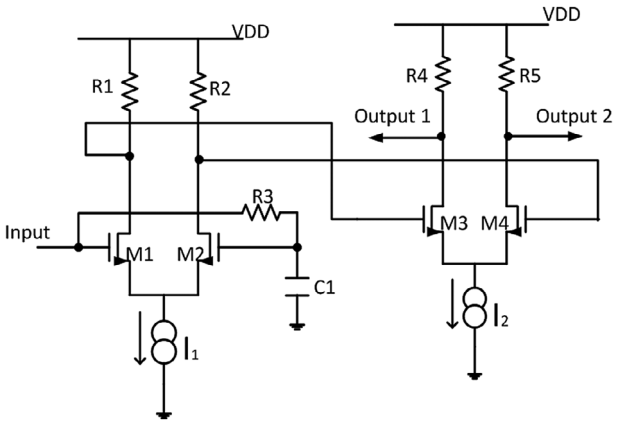

Figure 4. Schematic diagram of S2D, it is the circuit built for block S2D (first level).

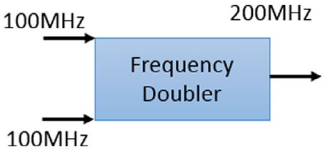

Figure 5. Block diagram of frequency doubler, output signal will have a doubled frequency.

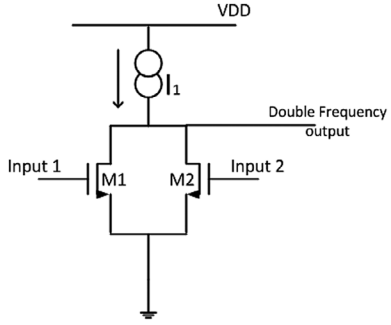

Figure 6. Circuit built for frequency doubler.

Note that all of blocks in this system are built with analogue circuit, and using CMOS transistor in 350 nm technology, simulation environment is in Cadence test bench.

3.2. Advanced design system

After trying the initial system, which was introduced in last section, I found it is not a completion design system. During the design range of these blocks, signal is not in good transfer properties when just use these blocks show in Figure 2, for example, the output signal of frequency doubler is very bad and could not display correct function when just single input for it, but when changing the input into differential form, the output will display better. Many situations like this have been corrected during the design and the new diagram for system design is shown in Figure 2.

From the figure we can see, it is different from the initial design system. The new block added, are single to differential block and duty cycle resumer. These two blocks are added for debugging circuit and making output signals under requirements. The analysis for these debugging details will be discussed in the next chapter. I will introduce each block with its circuit diagram and function next.

3.2.1. Single to differential amplifier (first level)

Figure 3 shows the block diagram of S2D. As the block diagram shows, the function for this block is generating differential output signals with single input signal, and the frequency of the signal will not change. The differential output means the two output signals' phase are different and with 180 degree phase shift.

With CMOS transistor and other analogue components, the single to differential amplifier is designed in Cadence schematic, which is shown in Figure 4.

3.2.2. Frequency doubler

For the reason of adding this block, it is matched up with the frequency divider, which is the last block of this system. In order to generate four signals with a different phase shift, we need a frequency divider to do this job, and if we want the output signal frequency kept the same as the input frequency, frequency doubler is added to this system. As the block diagram shows in Figure 5, it is used for doubling the frequency of input signal. The design of this block is using two NMOS transistors and a current source to connect them together and then the function of frequency doubler can be achieved. The design schematic circuit is shown in Figure 6.

As the schematic circuit shows, two NMOS transistor are connected together with a current source. The input ports are the two "Gate" poles of transistors and the "Drain" pole of these two transistors are connected together as the output port.

Figure 7. Block diagram of S2D (second level), same function as first level S2D.

With differential pair input signals, this circuit can be seen as "Current Control Module", and with different current passing through these two transistors at different times, a signal with double frequency can be synthesized at the output port. Thus, the function of frequency doubler can be achieved.

3.2.3. Single to differential amplifier (second level)

The function of second level S2D is same as the first level. The main difference is that we add a high pass filter at the input of the first circuit, which is same as the first circuit of first level S2D.

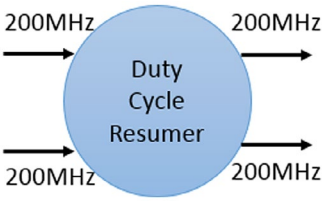

Figure 9. Block diagram of duty cycle resumer; it does not change frequency of the input signal.

The block diagram of second level S2D is shown in Figure 7. Because the input signal of the frequency divider is required as two differential signals, so this block is used to changing the single input signal to differential signals. The schematic circuit of the high pass filter and the second level S2D are shown in Figure 8.

This picture shows the high pass filter and the design circuit of second level S2D. The high pass filter is added to control the DC point of the input signal, and the voltage source is acted

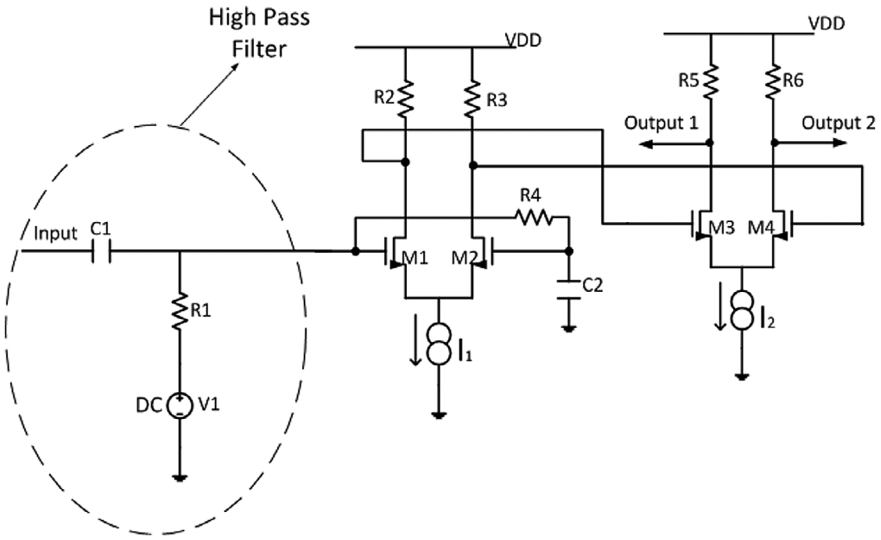

Figure 8. Schematic circuit of second level S2D, the circle marked part is a high pass filter, which added at the input port of the second level S2D, used for adjusting the dc point of the input signal.

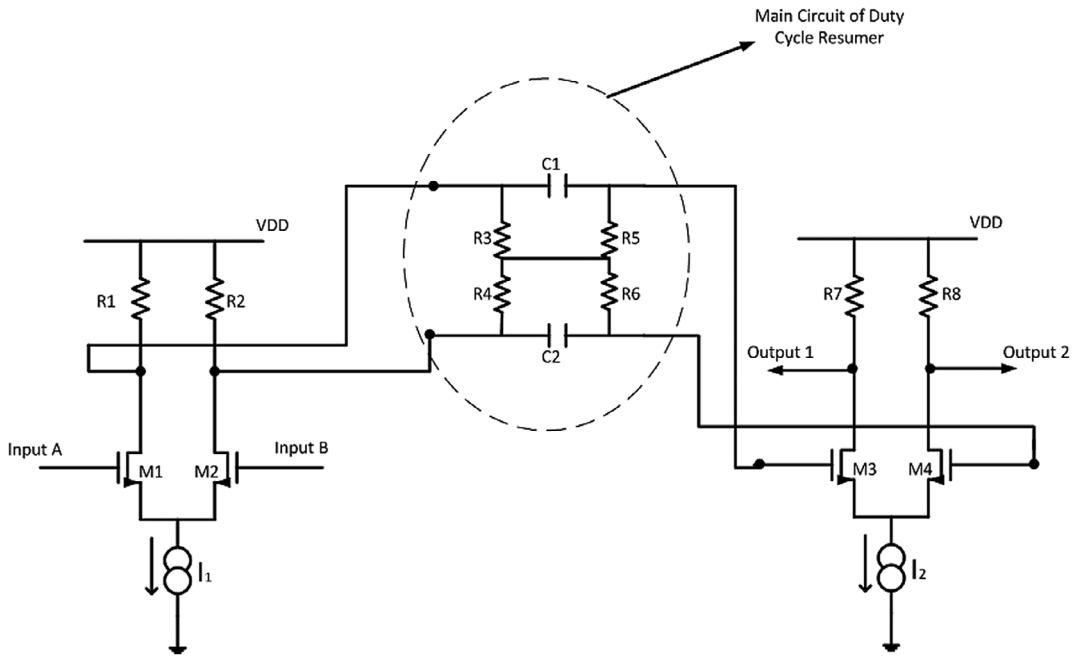

Figure 10. Circuit of duty cycle resumer, the circle marked out is the main part of the duty cycle resumer, and it is built between two amplifiers.

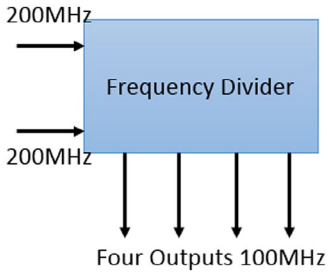

Figure 11. Block diagram of frequency divider, with differential input signals, it will generate four signals with 90 degree phase shift and the frequency will be divided by 2.

as a "Refresher," which can be used to give a new DC point of the input signal. We can control the DC point of the signal with changing the voltage value of this voltage source. Same as the first level S2D, the first circuit is used for generating two differential signals and the second circuit will amplify these two signals in order to passing them the next stage.

The block diagram for the second level S2D is same as the first level, so below does not display it.

3.2.4. Duty cycle resumer

The block diagram of duty cycle resume is shown in Figure 9. This block is added for debugging the circuit signal, and it is

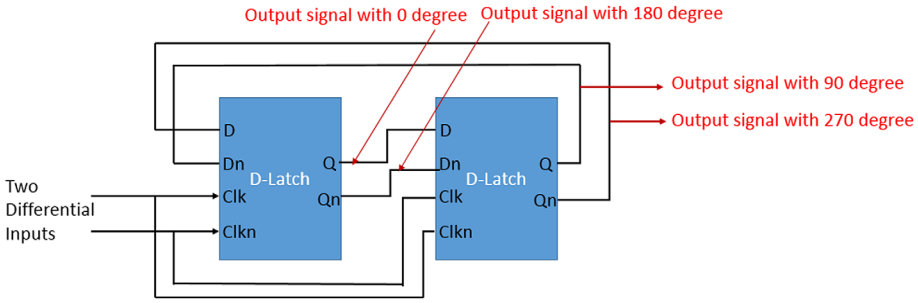

Figure 12. The inter structure of the frequency divider, is constructed by two D-latches with the same structure. Each of the two outputs of the latch are differential with each other.

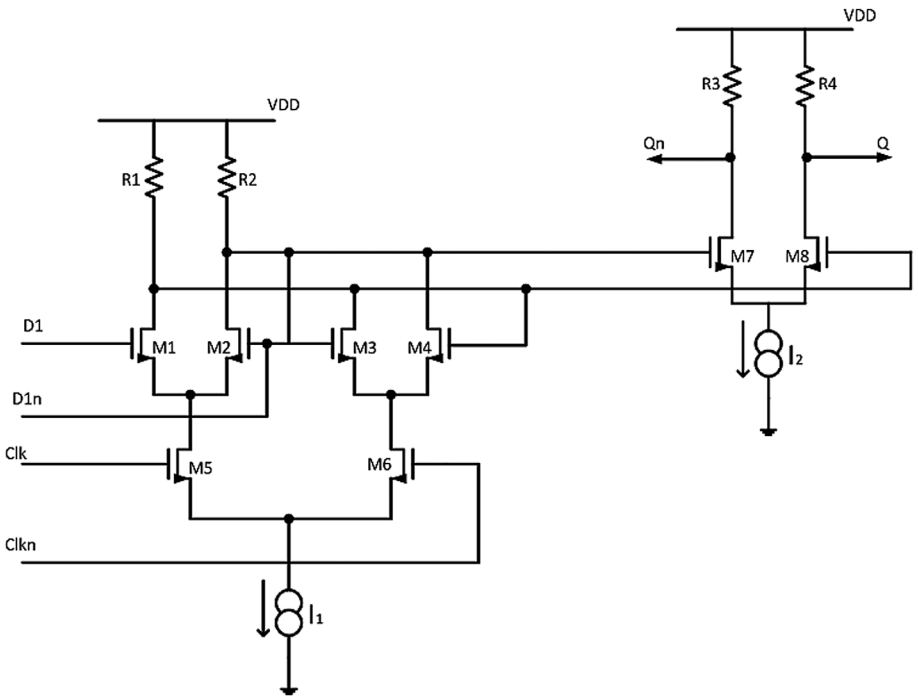

Figure 13. Schematic circuit of D-latch.

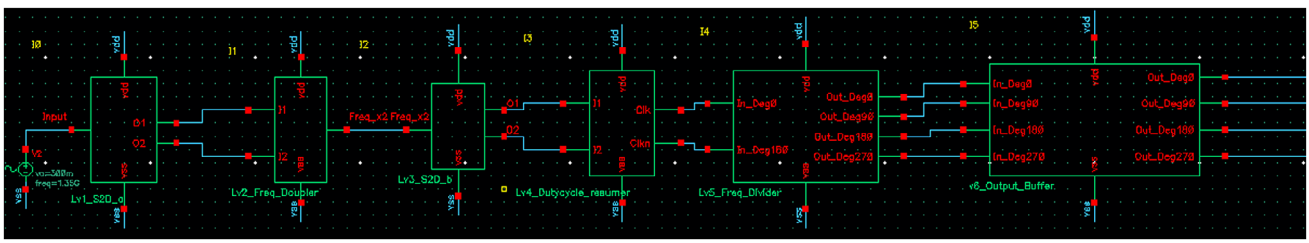

Figure 14. Final system with symbols of every block, in order to display a signal with enough amplitude, an output buffer, which is built by differential amplifier, is connected in the end of the system.

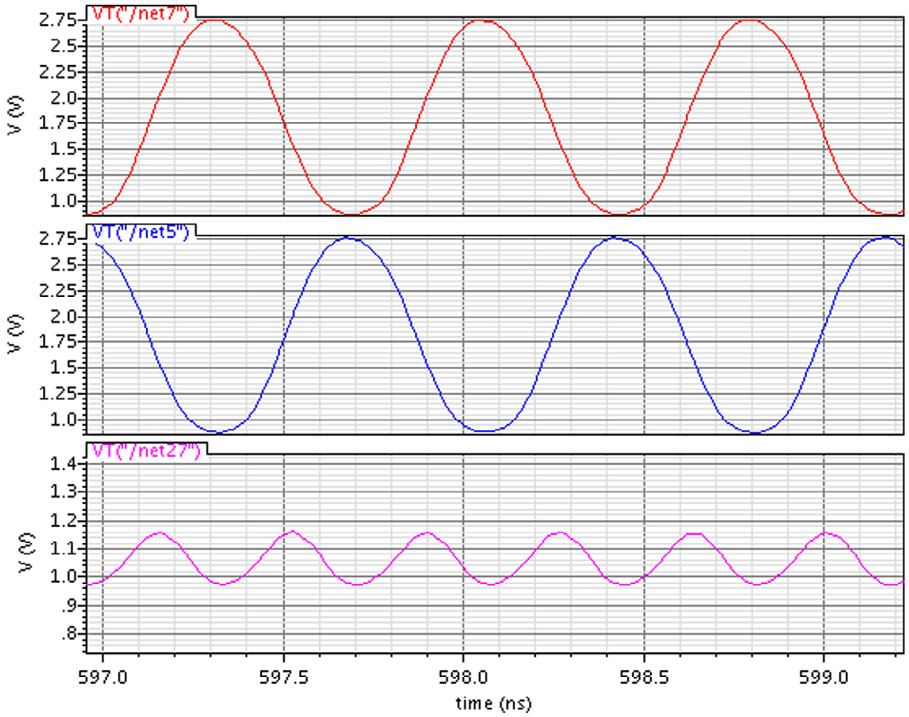

Figure 15. Simulation result for frequency doubler.

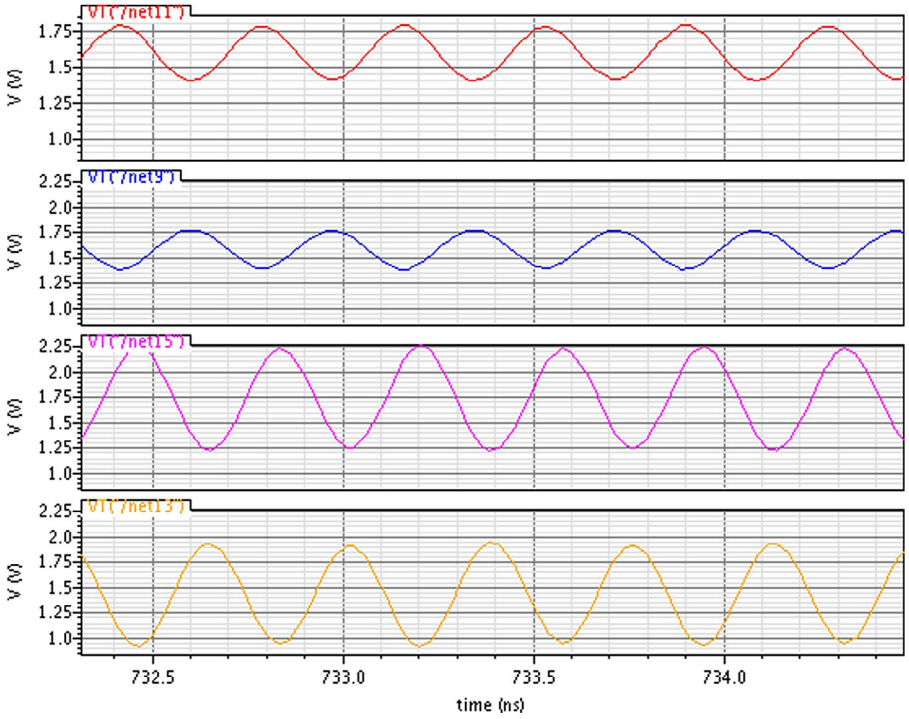

Figure 16. Simulation result for duty cycle resumer.

used to controlling duty cycle of the signals. It will not change the phase and the frequency of the signal and only adjust the duty cycle back to the correct location. During the design time, the differential outputs of the second level S2D had a very bad duty cycle when input to the frequency divider. This problem will influence the linear properties, dc point and the output frequency of the signal. So I added a circuit to resume the duty cycle. The design schematic circuit is shown in Figure 10.

3.2.5. Frequency divider

The block diagram of duty cycle resume is shown in Figure 11. This is mainly the design block of the system. It is used for dividing the frequency of the input signal in half and the phase of the differential input signal will be separated into four different phases, which are 0, 90, 180 and 270 degrees. This block is constructed by two D-latches, and the block diagram can be changed to two D-latches diagram with the same structure,

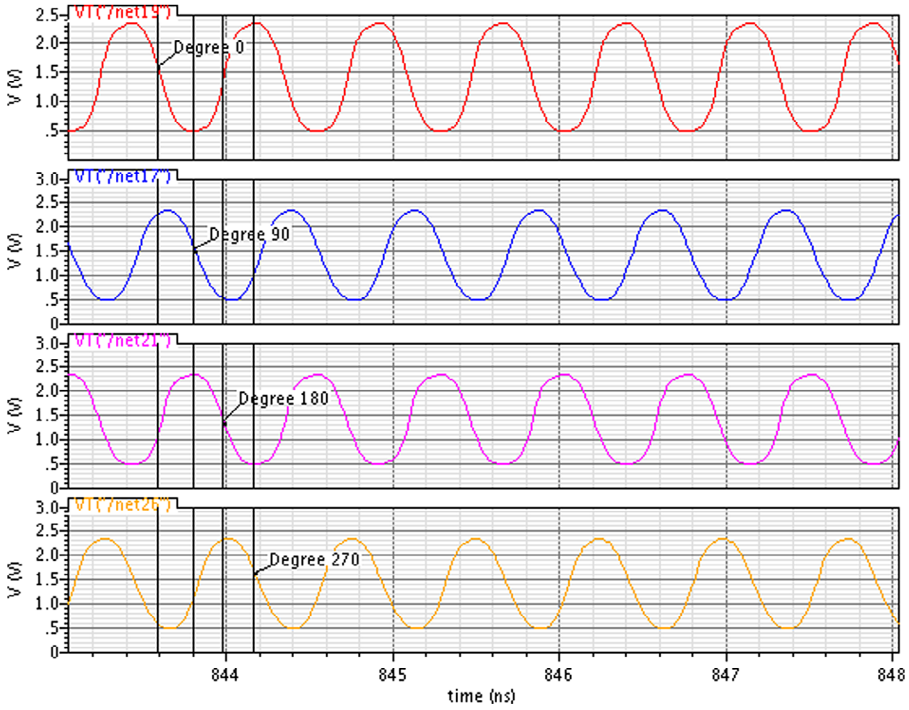

Figure 17. Simulation result for frequency divider.

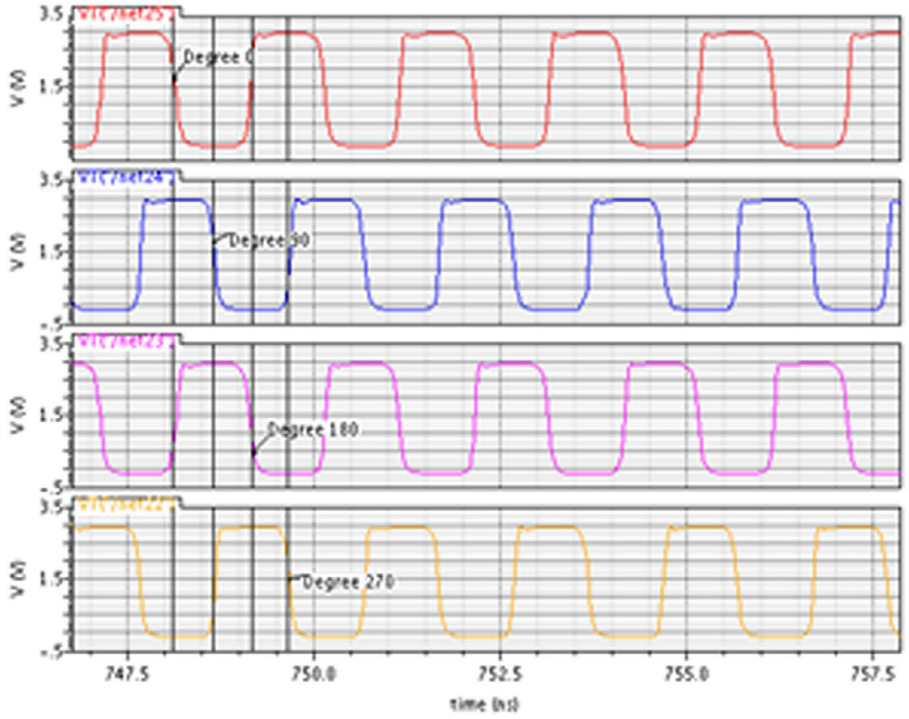

Figure 18. Simulation result for 1.35 GHz input frequency, generate four signals with 90 degree phase shift.

which is shown in Figure 12. From this block diagram, we can realize that the two differential inputs are treated as the clock signal of the D-latch, which are clock and clock'. Then the four different phase signals are outputted from each D-latch's output, which are Q and Q'. Also, the frequency of the input signal can be divided by 2 with one D-latch. Thus, four signals with 90 degrees phase shift can be generated by using this frequency divider. The schematic circuit for the frequency divider is the same as the schematic circuit of the D-latch, it is designed and shown in Figure 13.

The two D-latches have same structures with each other, so here just one is introduced. From the circuit we can see that the D-latch built with two stages, the first stage is the main structure of the D-latch, with six NMOS transistors connected with each other, it will achieve the function of signal latch and this is the basic function of DFF. The second stage is another differential amplifier. This is added to control the linear properties and the amplitude of the output signal of the D-latch. When connected these two D-latches together, the main function of frequency divider will achieved.

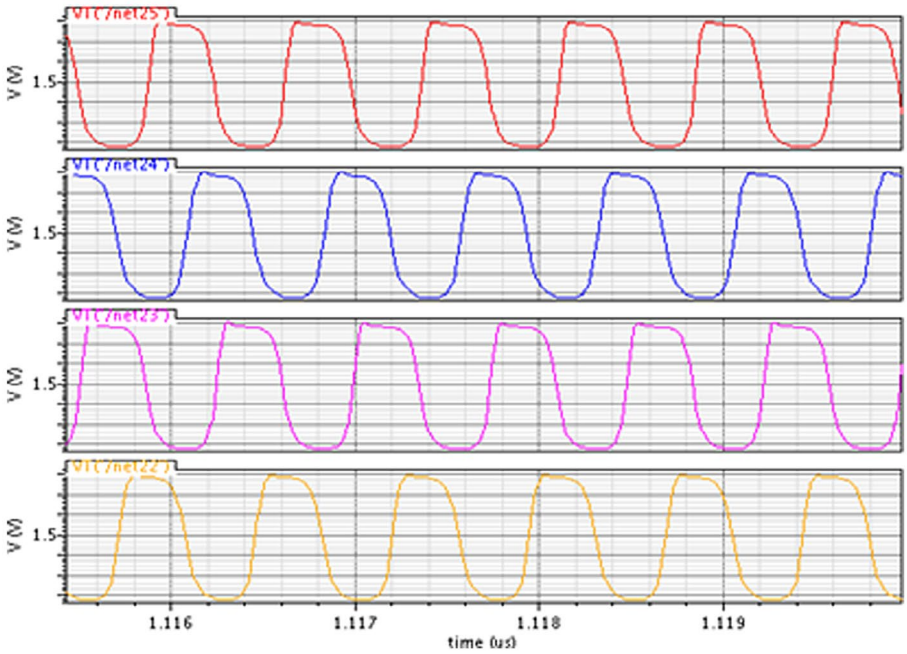

Figure 19. Simulation result for 500 MHz input frequency.

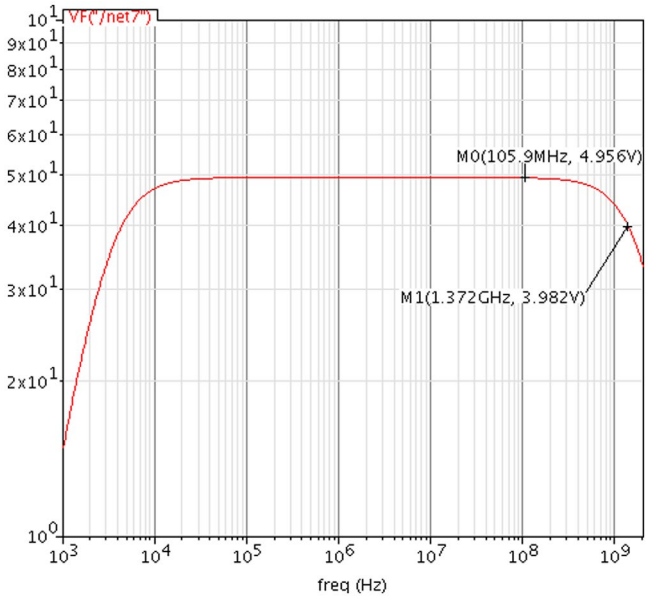

Figure 20. Simulation result of frequency response.

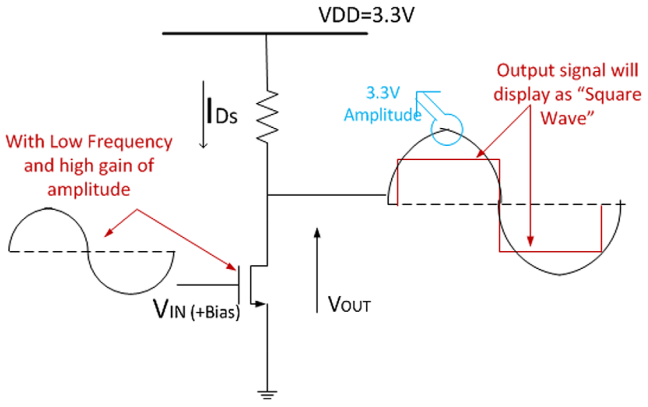

Figure 21. Output phenomenon at low frequency, this will explain why the output signals in figure 5.20 and 5.21 are displayed as a square wave, the signal amplitude is cut off at low frequencies.

Table 1. Components' value of block frequency doubler.

Name of block				
Frequency doubler	Resistors	NMOS Transistors	Current Source	Capacitors
Number Values/Width (Ohms, A, F, V)	–	M1 = M2 = 8um	I1 = 2.75 m	–

Notice: All transistors have same length, which is 350 nm.

4. Simulation results

After analyzing the basic circuit, the method used in debugging circuit has been declared. In this chapter, the simulation result will be displayed with circuit components value. All of the circuit design and simulation is in the Cadence with suitable analogue states loaded.

The final design circuit is shown in Figure 14, which is built within Cadence interface: it connects all of the blocks that introduced before. In order to display a signal with enough amplitude, an output buffer is added in the end of this system.

Because the system is designed for a high speed signal generator, which means the frequency of the output signal is between ranges of 100 kHz to 1.35 GHz, the simulation result will be showed based on the highest frequency it can be reached, 1.35 GHz, and other simulation frequencies will be displayed with the whole final system simulation.

4.1. Frequency doubler

The values for each kind of component are listed in Table 1.

The simulation result for frequency doubler is shown in Figure 17.

As the result picture shows, the first two signals are the differential signal, which outputs from the first level S2D, and the last signal is the output signal of frequency doubler. Although it has achieved the function of double the frequency, the DC point of the signal is drifting off the value

Table 2. Components' value of block duty cycle resumer.

First stage: Amplifier				
Second stage: duty cycle resumer				
Third stage: amplifier	Resistors	NMOS transistors	Current source	capacitors
Number	R1, R2	M1, M2	I1	0
	R3, R4, R5, R6	0	0	C1, C2
	R7, R8	M3, M4	I2	0
Values/Width (Ohms, A, F, V)	R1 = R2 = 450	M1 = M2 = 20um	I1 = 7.55 m	–
	R3 = R4 = R5 = R6 = 30 K	–	–	C1 = C2 = 50p
	R7 = R8 = 450	M3 = M4 = 20um	I2 = 7.55 m	–

Notice: All transistors have same length, which is 350 nm.

Table 3. Components' value of block frequency divider.

First stage: D-latch			
Second stage: amplifier	Resistors	NMOS transistors	Current source
Number	R1, R2	M1, M2, M3, M4, M5, M6	I1
	R3, R4	M7, M8	I2
Values/Width (Ohms, A, F, V)	R1 = R2 = 1.5 K	10um for all six transistors	I1 = 1.5 m
	R3 = R4 = 500	M7 = M8 = 20um	I2 = 7.55 m

Notice: All transistors have same length, which is 350 nm.

1.65v, so we should use DC point controller to fix it before goes into the next stage.

4.2. Duty cycle resumer

The values for each kind of component are listed in Table 2.

The simulation result for duty cycle resumer is:

The first two signals show in the image is the input of the duty cycle resume, and after fixed the duty cycle of the signal, the output signal is show in the image as last two signals.

4.3. Frequency divider

The frequency divider is construed by two D-Latches, the structure of them are the same and the components value are all the same too, so here I just list one D-latch's components values. The values for each kind of component are listed in Table 3.

The simulation result for frequency divider is:

From the image of the simulation result, we can see that four signals with 90 degree phase shift are generated from the frequency divider. The amplitude is not very good for both of them, so the last block is an amplifier, which called output buffer, and the structure of it is the differential amplifier, I have discussed in last section. The next step is to simulate the whole system with output buffer under different input signal frequency.

4.4. Simulation result of 1.35 GHz

Figure 18 shows the simulation result of 1.35 GHz input frequency, and it generates four signals with 90-degree phase shift.

4.5. Simulation result of 500 MHz

Figure 19 shows the simulation result of 500 MHz input frequency, and it generates four signals with 90-degree phase shift.

4.6. Simulation result of frequency response

Figure 20 shows the simulation result of the frequency response, and it gives a good explanation of the curve shape shows in Figure 18. Although the input signal is a standard sine wave form, the output signal with 500 MHz looks like a square wave. This is, because when the power supply voltage is fixed, which is 3.3 V, the lower frequency will have a higher AC magnitude, the gain of the amplifier will become larger, and the signal amplitude cannot reach the value when it is higher than the power supply voltage 3.3 V. This will cause the signal "cut" at the positive peak and negative peak, so it will display like a square wave. Figure 21 shows this phenomenon very clearly.

After analyzing the system for each block, the design of this project is finished. In this project, four phase signal generator has achieved and satisfied the requirement. For the signal this system generated, phase shift is 90 degrees for each signal, and the frequency range is between 100 MHz to 1.35 GHz, which achieved the requirement of high frequency signal design.

5. Conclusion

The main aim of this project is to design a system with four output signals whose phase have a 90 degree shift with each other and the frequency should be reached a high range, which is between 100 MHz to 1 GHz. Two systems have been researched and one of them has tried to be designed during the summer project period, which is DDS system. For achieving the requirements and to finish the project, another system was chosen to design. At last, the function of every block is achieved and the high speed system has been designed by using analogue circuit knowledge, and the design bench is Cadence analogue circuit design software. The design of each system block is not very hard, but the most challenging part is the circuit debugging, which means test the circuit with different components' value, like transistor width, resistor value and current source value. Then this system will act as a signal generator to use in the electrorotation system, and for the biological cell research area, which required a high speed electric rotation field, this system will be a good choice. But there still is some work not finished, these things will be discussed in future work.

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Disclosure statement

No potential conflict of interest was reported by the authors.

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References

Behrhorst, S. (1993, Aug). Design DDS Systems and Digitize IFs with DACs/ADCs. *Microwaves & RF,* 111–119.

Fuhr, G., Glaser, R., & Hagedorn, R. (2013). Rotation of dielectrics in a rotating high frequency field; Model experiments and theoretical explanation of the rotation effect of living cells. *Biophysical Journal, 49*, 395–402.

Holzel, R., & Lamprecht, I. (2012). Dielectric properties of yeast cells as determine by electrorotation. *Biochimica et Biophysica Acta, 1104*, 195–200.

Jones, T.B., & Washizu, M. (1996). Multipolar dielectrophoretic and electrorotational theory. *Journal of Electrostatics, 37*, 121–134.

Nicholas, H.T., Samueli, H., & Kim, B. (1998, June). The optimization of direct digital frequency synthesizer in the presence of finite 14. Word length effects performance. In *Proceedings of the 42nd Annual Frequency Control Symposium* (pp. 357–363).

Park, C.H., Kim, J.W., Lim, J.H., Jeong, S.S., Kim, M.H., & Park, T.G. (2012). Increase of generating power of cantilever type piezoelectric generators by interconnecting the generators. *Intelligent Automation & Soft Computing, 134*, 88–101.

Pohl, H.A. (1999). *Dielectrophoresis*. Cambridge, UK: Cambridge University Press.

Ponce, P., Molina, A., & MacCleery, B. (2013). Integrated intelligent control and fault system for wind generators. *Intelligent Automation & Soft Computing, 19*, 373–389.

Tierney, J., Rader, C., & Gold, B. (1991, March). A digital frequency synthesizer. *IEEE Transaction on Audio and Electroacoustics, AU-19*, 48–57.

Understanding Direct Digital Synthesis (DDS). (2013, November, 21). Retrieved from http://www.ni.com/white-paper/5516/en/