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High Linear Voltage Gain in QZNC Through Synchronizing Switching Circuits

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Abstract: The solar powered systems require high step-up converter for efficient energy transfer. For this, quasi-impedance network converter has been introduced. The quasi-impedance network converter (QZNC) is of two types: type-1 and type-2 configuration. Both the type-1 and type-2 QZNC configurations have drooping voltage gain profile due to presence of high switching noise. To overcome this, a new quasi-impedance network converter synchronizing the switching circuit with low frequency noise has been proposed. In this paper, the proposed QZNC configuration utilizes the current controlling diode to prevent the output voltage drop. Thus, the suggested topology provides linear high voltage gain profile, low load voltage ripple, and reduced impedance network stress and device stress. Therefore, the efficiency of proposed QZNC has been improved. The topology description, working principle, parameter design and comparison with traditional converters are illustrated. And finally, both simulation and practical results are presented to confirm the converter characteristics and performance. From the results, it has been found that the performance of the suggested topology is better as it achieves a higher efficiency of 81% and hence, it is suitable for high power applications.

Keywords: Quasi impedance network converter (QZNC); voltage ripple; network stress; device stress; and efficiency

1 Introduction

The renewable energy resources such as solar and wind energy are appeared as an alternate energy resource in many industrial applications. Since the industrial sectors faces the problem of shortage of conventional fossil fuel. Therefore, the alternate energy chosen should available abundantly and eco-friendly [1]. In view of this, among the renewable energy resources, the solar energy is mostly preferred as it meets the demand efficiently. Whereas the output from such solar energy resources is low, and far from the high voltage dc link. So, the demand for high step-up dc-dc converter is risen and more research on these topologies has been carried out. Most of the industrial applications such as electric vehicle power supplies, Light Emitting Diode (LED) lighting, X-ray systems, electric vehicle charging system, and grid connected systems requires high boost ratio dc-dc converters [2].

The most commercially used topology for solar energy is the boost Direct Current (DC-DC) converter [3] which achieves higher gain at high duty ratio. Due to this, the device losses increase which results in the degradation of the converter efficiency [4]. Moreover, considering the effect of parasitic elements, the duty ratio of the traditional boost converter is limited [5]. In addition to that, many topologies such as cascading two boost converters [6], coupled inductors [7] and interleaving concept [8], converter with switched capacitor [9], converter with switched inductor [10], voltage lift technique [11] have been presented. However, the size of the converter is increased making it more complex [12], and it needs to be worked at high duty ratio [13]. To overcome this, Z-source converter has been proposed in the year 2002 [14]. Whereas it has the drawback of the discontinuous source current which affects the converter performance [15]. Thus, the QZNC has gained more attraction in the power electronics sector due to its unique feature of high voltage gain at low duty ratio [16], the continuous source current [17] and higher efficiency [18]. It works in both buck and boost operation based on the load profile [19]. These types of converters are applied in photovoltaic system [20], electric vehicle charging station [21] and distributed generation [22]. This converter uses the impedance network placed between the source and load to boost the voltage. The boost factor depends on the shoot-through duty ratio. By incorporating the impedance-network configuration, the requirement of passive components is lowered. The impedance network is in X-shape with interconnection of inductors and capacitors [23].

QZNC is of two types: type-1 [24] and type-2 configuration [25]. The output inductor in the type-1 configuration has been replaced with the diode in the type-2 QZNC, hence, the voltage gain has increased [26]. But the type-2 QZNC has limited duty ratio ($D < 0.33$) [27] and has the problem of heavy voltage stress across the network, thereby the converter behavior is affected. The reason for limited duty ratio for operating the converter is due to high switching noise. In DC-DC converter, dead time exists in between turning ON and OFF of the power switch. During dead time, reverse current flows through the circuit which degrades the converter performance. To commutate this, capacitor draws high starting current from the power supply. Due to this, whenever the input voltage to output voltage ratio increases, the capacitor draws higher starting current, thereby, the output voltage drops. This results in the converter voltage gain profile to droop after certain value of duty ratio. Also, the voltage ringing occurs in the converter circuit if the negative current is not commutated properly. As the capacitor takes more time to commutate the reverse current, the high switching noise exists. Because of high switching noise and ESR present in the switching capacitor limits the converter efficiency for wide range of input voltage to output voltage ratio. Since the existing QZNC comprises of capacitors in the network, the duty ratio of the converter is limited and the voltage stress across the network as well as across the power device increases. This result in the existing type-1 and type-2 QZNC is not preferred for high power applications.

In this paper, a new type of QZNC has been proposed with low switching noise. The low switching noise is obtained using current controlling diode. But the diode should have short reverse recovery time. Because, the diode with long reverse recovery time takes more time to commutate the negative current and also, the parasitic inductance present in it increases the dI_F/dt. Due to increased dI_F/dt, the voltage stress across the network increases. Thus, the fast reverse recovery diode FR107 has been used in the proposed topology, thereby, low switching noise operation is obtained. This extends the new QZNC operation for wide range of input voltage to output voltage ratio and achieves high voltage gain compared to other topologies. Also, the voltage stress across the impedance network as well as across the power device is reduced. The reduced output voltage ripple is obtained with the proper designing of converter parasitic elements. This results in the improved converter efficiency for wide range of duty cycle. Hence, the proposed QZNC can be used for high power application. To confirm the performance, the comparative analysis has been carried out between the new modified QZNC topology with the conventional boost, ZNC and type-1 and type-2 QZNC configurations. The parameters accounted for the analysis are voltage gain, load voltage

ripple, capacitor voltage stress, diode voltage stress, device voltage stress and efficiency. The performance of the parameters has been computed for different duty ratio and compared.

The organization of the paper is as follows: The operating principle and design guideline of the proposed topology have been discussed in Section 2 and Section 3. Section 4 illustrates the simulation results and comparative analysis of the three converter topologies. Section 5 deals with the hardware results of the proposed converter. Section 6 concludes the paper.

2 Operating Principle of Proposed QZNC

The concept of QZNC attracted the power electronics engineers because of its unique feature illustrated in [28] which is imperative for the DC-DC converter. The impedance-network (LDC unit) is placed between the supply (in cascading with the supply) and load [29]. The pictorial representation of the type-1 QZNC is shown in Fig. 1. Due to the presence of output inductor (L_o), the type-1 converter performance is limited to the $D < 0.37$ which limits converter gain. Thus, the output inductor is replaced by diode (D_o) in type-2 QZNC as shown in Fig. 2. Though, high voltage gain is achieved, the duty ratio is still limited to $D < 0.33$ and the converter undergoes high stress across the device as well as the impedance network. To overcome these demerits, a new type of QZNC has been proposed, and it is depicted in Fig. 3. The proposed converter behaves better for the ranges of duty cycle (D) upto 0.49. In this section, the working principle and modes of operation of the proposed converter is explained.

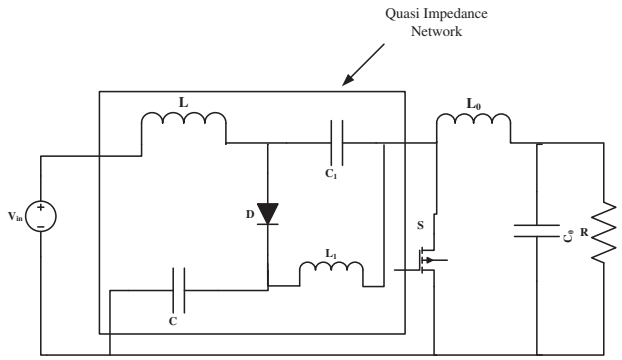


Figure 1: Type-1 QZNC

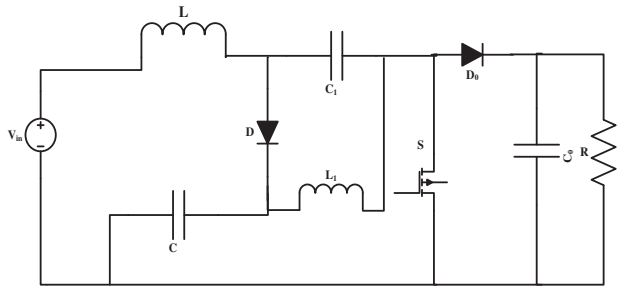


Figure 2: Type-2 QZNC

The inductors L, L_1, capacitor C, and diode D, D_1 constitute the impedance network. The operation of the proposed converter is described in two modes as presented in Figs. 4a and 4b, and it is explained below.

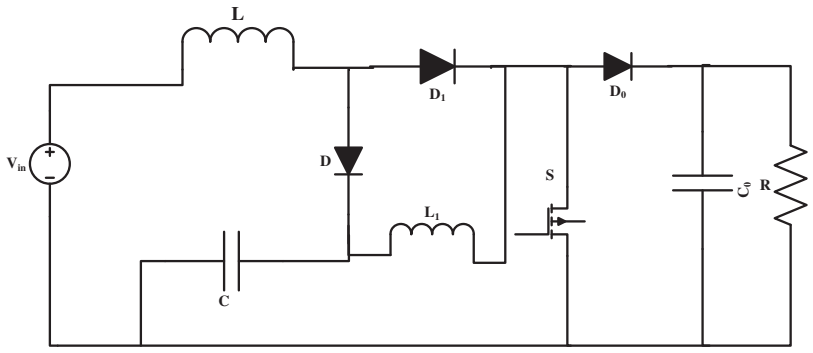
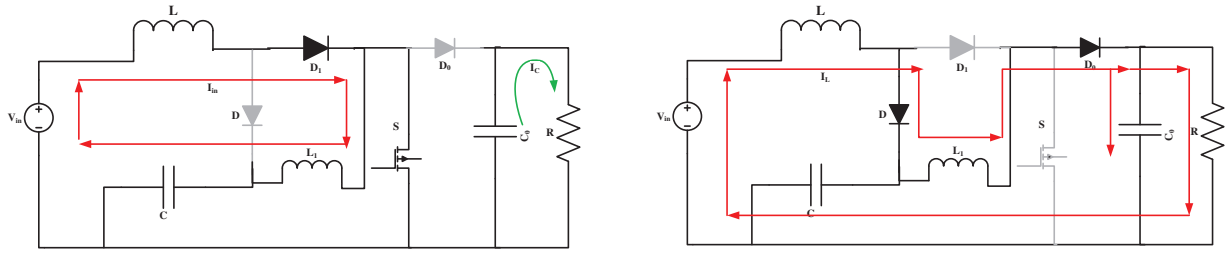


Figure 3: Proposed QZNC



(a) Mode 1 operation of QZNC

(b) Mode 2 operation of QZNC

Figure 4: (a) Mode 1 operation of QZNC (b) Mode 2 operation of QZNC

Mode 1 [0 ~ t_0]: When switch S and diode D_1 are in conduction, the pre-charged capacitor discharges the current through the inductors (L_1 and L_2), thus, reverse biases the diode D and D_0. Due to this, the current through the inductor increases linearly as shown in Fig. 5. Once the inductor current reaches the steady state value, the inductor starts to discharge ending mode-1 operation.

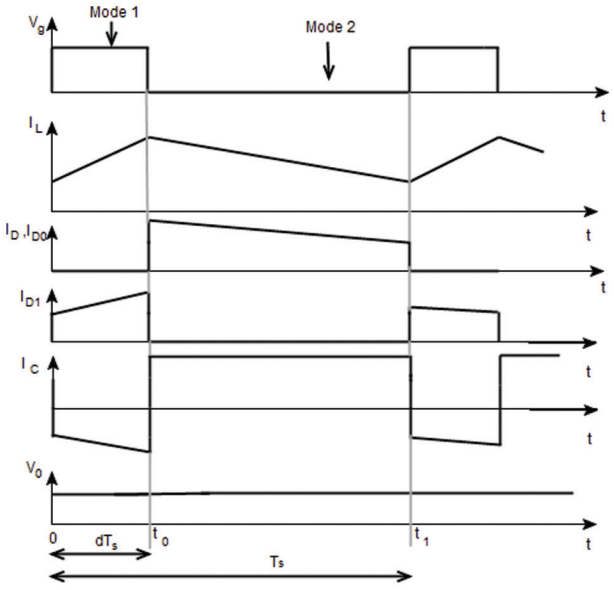


Figure 5: Waveforms of the proposed QZNC

Mode 2 [$t_0 \sim t_1$]: When switch S is in off state, the capacitor C is charged by the inductors (L_1 and L_2). This turns on the diode D and D_0, whereas the diode D_1 is in off condition. Now, the current through the inductor decreases linearly as shown in Fig. 5. The load is powered by impedance network.

3 Design Equations of QZNC

The QZNC emerges as an eye-catching topology due to its superior performance such as low output voltage ripple and reduced stress across power device. These features are attained by proper designing of the converter. Thus, the equations derived for the passive elements describe in this section. The voltage relationship of the new topology is obtained by using the voltage-second balance for the inductor [30] as in Eq. (1).

$$(V_{in} + V_c)dT_s + (-V_c)(1-d)T_s = 0 \tag{1}$$

According to mode2, the load voltage of the converter is as in Eq. (2)

$$V_0 = V_{in} + 2V_c \tag{2}$$

By manipulating Eqs. (1) and (2), the gain of the converter is as in Eq. (3)

$$G = \frac{V_0}{V_{in}} = \frac{1}{1-2d} \tag{3}$$

Assuming loss free converter, the current through inductor is found using the Eq. (4).

$$I_L = \frac{V_0^2}{V_{in}\,R} = \frac{V_{in}}{(1-2d)^2\,R} \tag{4}$$

Then, the inductor expression is as in Eq. (5),

$$L = \frac{2d\ (\ 1-2d)V_{in}}{(1-2d)\Delta I_L f_s} \tag{5}$$

where,

ΔI_L = 10% to 30% of I_L,

f_s = switching frequency,

d = duty ratio

V_c = capacitor voltage

The voltage ripple of the capacitor is expressed as the function of inductor current as it is equal to the capacitor current during mode 1. From this, the capacitor is found by the expression and stated as in Eq. (6),

$$C = \frac{I_L d}{\Delta V_c f_s} \tag{6}$$

where,

ΔV_c = 1% to 5% of V_c

4 Simulation Results

The problems associated with the existing topologies for high step-up voltage applications have been overcome by the proposed QZNC. The modifications performed in the proposed topology, and it is

operations are clearly presented in the Section 2. Also, distinctive features are achieved by proper design which has been described in Section 3. Based on the Eqs. (1)–(6), the proposed converter has been designed and simulated in MATLAB/SIMULINK. The simulations parameters are listed in Tab. 1 are identical for all the three converters. The simulation results are studies and compared with other topologies in terms of its performance. The parameters accounted for analysis are voltage gain, load voltage ripple, capacitor voltage stress, diode voltage stress, device voltage stress and efficiency [31]. The parameters are computed for different duty ratios [32].

Table 1: Simulation parameters

Parameters	Rating
Input voltage (V)	40 V
Output voltage (V)	52 V
Duty cycle (D)	0.15
Inductor (L)	147 μH
Capacitor (C)	413 μF
Load resistor (R)	25 Ω
Device frequency (f)	25 kHz

4.1 Voltage Gain

The main feature of the proposed QZNC is linearly higher voltage gain characteristics. The voltage gain characteristics of all the three QZNC for distinct values of duty ratio has been depicted in Fig. 6. From Fig. 6, it is clear that the suggested topology has increasing gain characteristics, whereas the other topologies has drooping characteristics due to its operation at limited duty ratio.

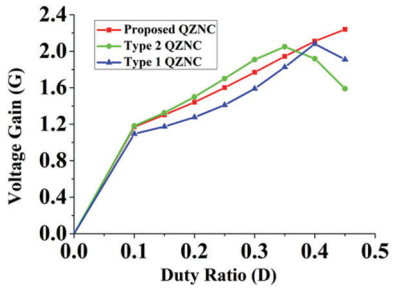


Figure 6: Voltage gain *vs.* duty ratio

As depicted in Fig. 6, the voltage gain of the type-2 converter starts to decrease when the duty ratio is increased beyond 0.33 even though it has high voltage gain than the proposed converter. Also, the type-1 converter starts to droop when the $D > 0.37$. This clearly shows that the existing topology works upto the duty ratio of 0.37 only. In contrast, the recommended converter performs well for $D \leq 0.49$.

4.2 Load Voltage Ripple

Another main feature of the proposed QZNC is reduced load voltage ripple. The behavior of load voltage ripple characteristics of all the three QZNC for different duty ratio has been studied and its pictorial representation is depicted in Fig. 7. Though type-1 configuration has lower load voltage ripple, it

has the drawback of low voltage gain than the proposed and type-2 topologies. Thus, from the Fig. 7, it has been inferred that the proposed topology is preferred as it has low load voltage ripple compared to type-2 topology.

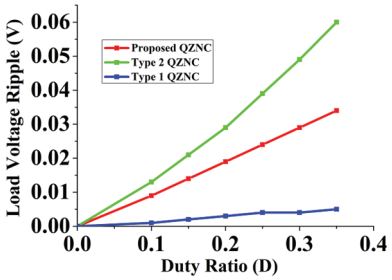


Figure 7: Load voltage ripple *vs.* duty ratio

4.3 Stress Analysis

As discussed earlier, the proposed QZNC achieves high step-up output voltage at low duty ratio. Owing to this, the voltage spike across the power device, diode and capacitor has been reduced drastically. To ensure this, the voltage stress across the switch, diode, and capacitor for different duty ratios of all the three converters has been computed and compared with each other. The voltage stress characteristics have been depicted in Figs. 8 to 9. The comparison of network diode voltage stress for various values of voltage gain is presented in Fig. 8. From 8, it could be inferred that the proposed QZNC has reduced voltage stress across the diode compared with type-1 and type-2 QZNC.

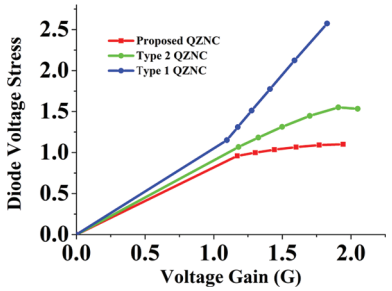
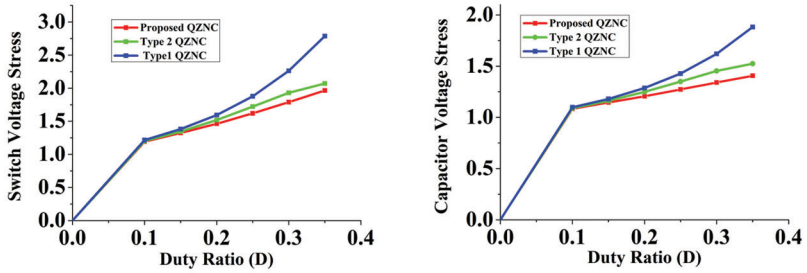


Figure 8: Diode voltage stress $\left(\frac{V_d}{V_i}\right)$ *vs.* voltage gain



(a) Voltage stress across the switch $(\frac{V_s}{V_i})$ versus duty ratio

(b) Voltage stress across network capacitor $(\frac{V_c}{V_i})$ versus duty ratio

Figure 9: (a) Voltage stress across the switch $\left(\frac{V_s}{V_i}\right)$ *vs.* duty ratio (b) Voltage stress across network capacitor $\left(\frac{V_c}{V_i}\right)$ *vs.* duty ratio

Fig. 9a shows the voltage stress across the device for all the three converters. It is implied that the proposed QZNC has lower voltage stress across the device compared with the existing configuration. Furthermore, it is inferred that for D > 0.1, there is a drastic reduction in voltage stress across the device for the proposed QZNC against the other topologies. Also, the recommended proposed QZNC has lower capacitor voltage stress compared with type-1 and type-2 QZNC as shown in Fig. 9b. From Fig. 9b, it is implied that compared with other topologies, the suggested converter has drastic reduction in the voltage stress across the device for D > 0.1.

4.4 Efficiency

The efficiency of all the three QZNC are evaluated and compared with each other. The power loss (P_{loss}) computation for all the three topologies for the specified duty ratio (D = 0.15) is presented in Tab. 2. The loss calculation is shown below [33].

Table 2: Comparison of power loss

QZNC	P_{loss} (W)	Efficiency (%)
Type-1	137.68	88.45
Type-2	169.88	87.01
Proposed	130.47	89.39

The device loss is,

Device loss, $P_s = Conduction\ loss + Switching\ loss$ as in Eq. (7)

$$P_s = \left(\frac{DI_o^2}{(1-2D)^2}\right) r_s + \frac{f_s C_o P_o R_o}{2} \tag{7}$$

The diode loss is as in Eq. (8)

$$P_D = \left(\frac{\left(2D\sqrt{1-D}\right)^2}{(1-2D)^2}\right) I_o^2 r_d + \frac{2D\,(1-D) I_o V_f}{(1-2D)} \tag{8}$$

The inductor loss is as in Eq. (9)

$$P_{rL} = \left(\frac{1}{(1-2D)^2}\right) I_o^2 r_L \tag{9}$$

The Capacitor loss is as in Eq. (10)

$$P_{rC} = \left(\frac{\left(\sqrt{D} + 2D\sqrt{1-D}\right)^2}{(1-2D)^2}\right) I_o^2 r_C \tag{10}$$

where, C_o = Output capacitance of the device,

V_f = Forward voltage drop of the diode.

Hence, the efficiency of QZNC is improved against the suggested network. The efficiency comparison for different duty ratio is depicted in Fig. 10. From Fig. 10, it could be seen that the recommended QZNC has high efficiency for all the values of duty ratio compared with the existing topologies.

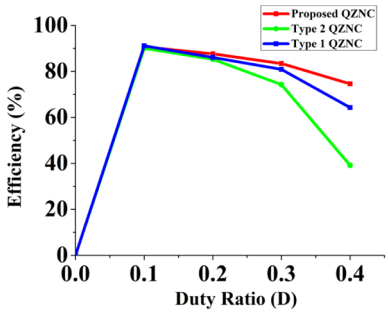


Figure 10: Efficiency *vs.* duty ratio

4.5 Number of Components

The comparison of proposed topology with other converter topologies for the specified duty ratio (D = 0.15) in terms of converter components are listed in Tab. 3. The number of diodes, inductors and capacitors are denoted as N_D, N_L and N_C.

Table 3: Comparison of converter topologies

Topology	N_D	N_L	N_C
Boost [34]	1	1	1
Interleaved boost converter [35]	2	2	1
Quadratic boost converter [36]	3	2	3
Voltage multiplier [37]	4	2	5
Z-source converter [38]	1	3	3
Type-1 QZNC [20]	1	3	3
Type-2 QZNC [21]	2	2	3
Proposed QZNC	3	2	2

4.6 Output Waveform

The simulation waveform of proposed topology is presented in this section. The supply and load waveforms of new QZNC shown in Fig. 11. The stress across the device shown in Fig. 12.

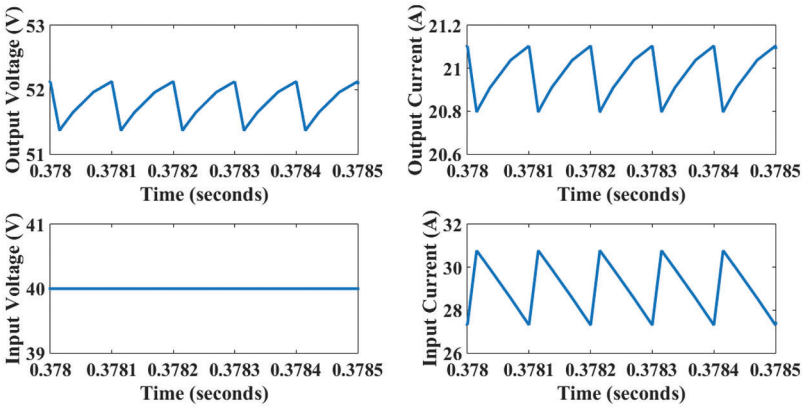


Figure 11: Supply and load voltage of proposed QZNC

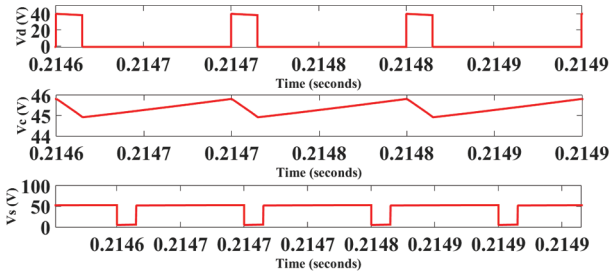


Figure 12: Stress waveform of proposed QZNC

The supply voltage of 40 V stepped to 52.12 V for D = 0.15 as shown in Fig. 11. Thus, the converter voltage gain is 1.303 based on Eq. (3). From Fig. 11, it is observed that the ripple of the load voltage is less which is 0.01 V. The pictorial representation of the voltage across the network diode (V_d), network capacitor (V_c) and across the device (V_s) is depicted in Fig. 12.

For the suggested QZNC, the voltage stress across the network diode (V_{ds}) is 0.99 $\left(\frac{V_d}{V_i} = \frac{39.98}{40}\right)$, the network capacitor voltage stress (V_{cs}) is 1.14 $\left(\frac{V_c}{V_i} = \frac{45.8}{40}\right)$ and the voltage stress across the device (V_{ss}) is 1.3 $\left(\frac{V_s}{V_i} = \frac{52.9}{40}\right)$ as depicted in Fig. 12. The diode stress is reduced to 19% and capacitor as well as switch stress is reduced to 2% compared with type-2 QZNC. Thus, the proposed topology is better, when compared to the conventional impedance network converters. The comparison of the proposed topology with existing topologies illustrated in Tab. 4. The summary of the topologies is analyzed, as in Fig. 13.

Table 4: Comparison of converter topologies

Topology	G	ΔV_o (%)	Duty ratio D = 0.1			Duty ratio D = 0.3			∩ (%)
			$V_{cs} = \left(\frac{V_c}{V_i}\right)$	$V_{ds} = \left(\frac{V_d}{V_i}\right)$	$V_{ss} = \left(\frac{V_s}{V_i}\right)$	$V_{cs} = \left(\frac{V_c}{V_i}\right)$	$V_{ds} = \left(\frac{V_d}{V_i}\right)$	$V_{ss} = \left(\frac{V_s}{V_i}\right)$	
Boost [34]	1.15	1.5	1.15	1.13	1.17	1.41	1.38	1.43	90.3
Interleaved boost converter [35]	1.16	1	1.14	1.12	1.16	1.4	1.25	1.31	85.5
Quadratic boost converter [36]	1.13	0.9	1.21	1.35	1.35	1.39	1.6	2.13	80.3
Voltage multiplier [37]	1.17	1.1	1.15	1.21	1.39	1.35	1.71	1.85	83.5
Z-source converter (ZSC) [38]	1.17	0.27	1.18	1.31	1.38	1.62	2.12	2.23	66.3
Type-1 QZNC [20]	1.17	0.23	1.18	1.31	1.38	1.62	2.12	2.23	88.45
Type-2 QZNC [21]	1.3	2.1	1.16	1.18	1.34	1.45	1.55	1.93	87.01
Proposed QZNC	1.3	1.4	1.14	0.99	1.32	1.34	1.09	1.79	89.39

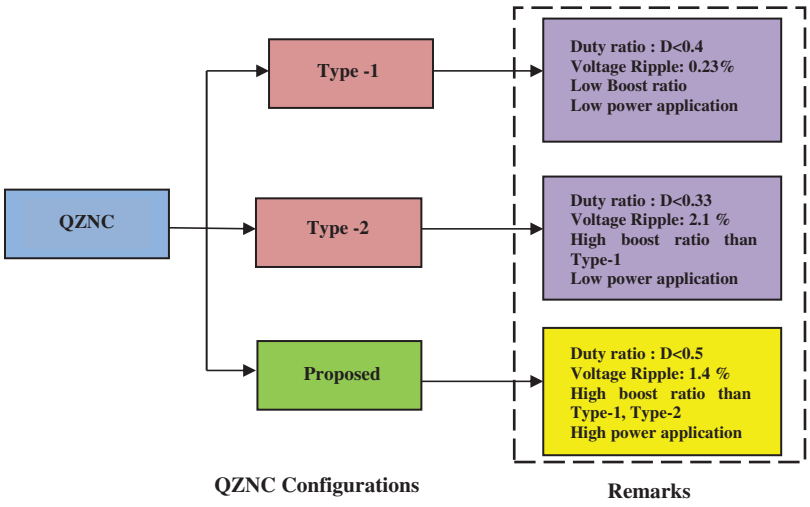


Figure 13: Summary of QZNC

Though Z-source converter has lower ripple in the load voltage as shown in Tab. 4, the stress across the network diode is higher than the boost converter, and efficiency has also reduced. The efficiency has improved with type-1 and type-2 QZNC, still the stress higher and it has limited duty ratio feature. Though the gain of the suggested topology and type-2 converter are same, the gain of the suggested topology is higher than the boost converter, ZSC and type-1 converter. The stress across the network diode has also drastically reduced with the suggested converter (19% reduced) compared with other converter topologies. The reduced load voltage ripple compared with boost converter and the efficiency has enhanced. The stress comparison for two different duty cycles for all the DC-DC converter is listed in Tab. 4. From Tab. 4, it could be implied that the network stress as well as device stress of the recommended topology has reduced even if the duty cycle has increased. Thus, it is observed that the recommended proposed QZNC has better performance as it has high gain, reduced load voltage ripple, reduced network stress and device stress, better efficiency and works well for all the value of duty ratio.

5 QZNC Test Bed Results

The simulation results also shows that the proposed converter has superior features such as linearly high voltage gain for all the values of duty ratio and reduce voltage spike across the network and device. To validate, a laboratory setup has been developed compared with type-1 and type-2 converter in this section. The setup of proposed QZNC with input of V_{in} = 40 V, I_{in} = 1.49 A is depicted in Fig. 14.

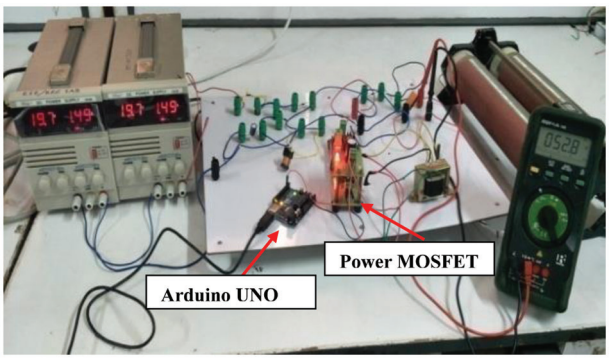


Figure 14: Proposed QZNC

The two DC voltage sources cascaded, and it provides 40 V input to the quasi network. From Fig. 14, it could be seen that the boosted voltage is 52.8 V, and the voltage gain is 1.3. The power MOSFET used in the converter is IRFP 840 and diode is FR107. The gating pattern has been generated using ARDUINO UNO. The results measured using power quality analyzer WT500. The waveforms are presented in Figs. 15–18.

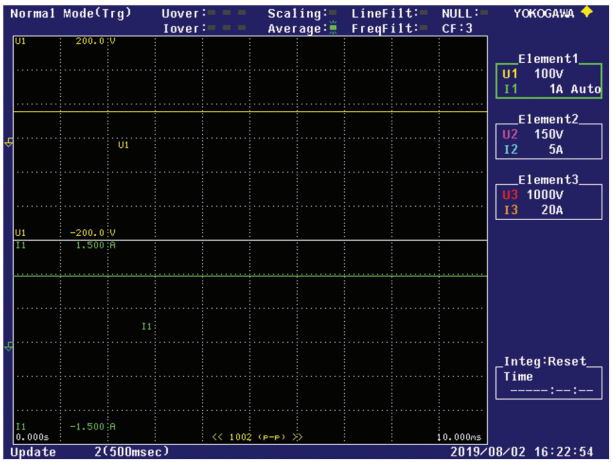


Figure 15: Load voltage and load current of proposed QZNC

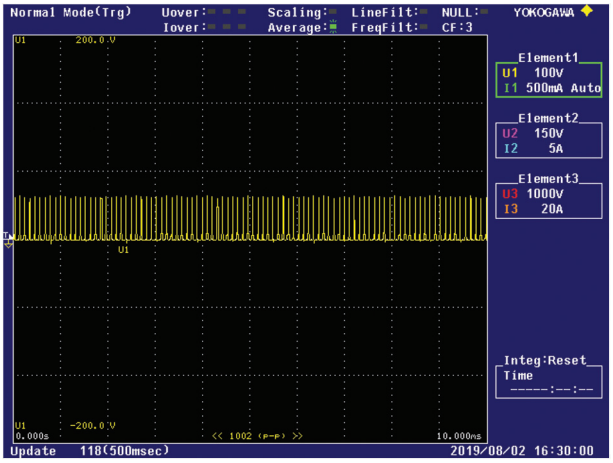


Figure 16: Network diode voltage waveform

From Figs. 15–18, the measured values are as follows: output voltage ripple is 1.04%. The network diode voltage (V_d) is 4.92 V, network capacitor voltage (V_c) is 43.61 V, device voltage (V_s) is 43.8 V. And, the network diode voltage stress (V_{ds}) is 0.1, network capacitor voltage stress (V_{cs}) is 1.09 and device voltage stress (V_{ss}) is 1.09.

The comparative analysis between all the three types of converters based on hardware results are presented in the Tab. 5. And the comparison between simulation and hardware results are illustrated in Tab. 6.

From Tab. 5, it could be inferred that though the voltage gain of proposed QZNC remains same as that of the type-2 converter, but the network and device stress has reduced and the efficiency has improved significantly. Further, it is observed that the variation in the voltage ripple is less compared with the type-2 converter. However, the ripple reduces as the duty ratio increases in the case of the proposed converter

as shown in Fig. 7. Therefore, the overall performance of the suggested converter is better than the existing topologies. The comparison between simulation and hardware result is presented in Tab. 6. From 6, it has been concluded that the simulation values are validated through practical results.

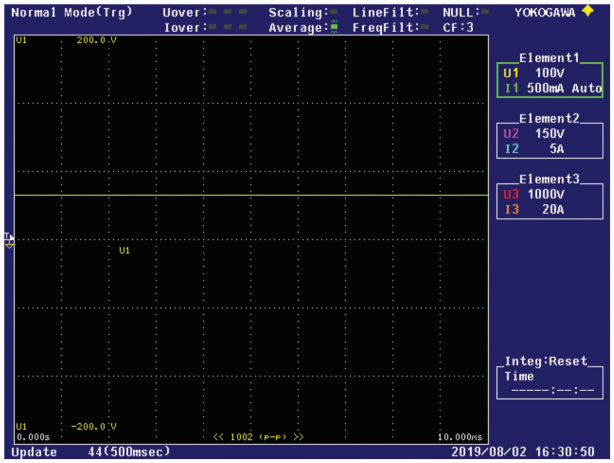


Figure 17: Waveform of the network capacitor voltage

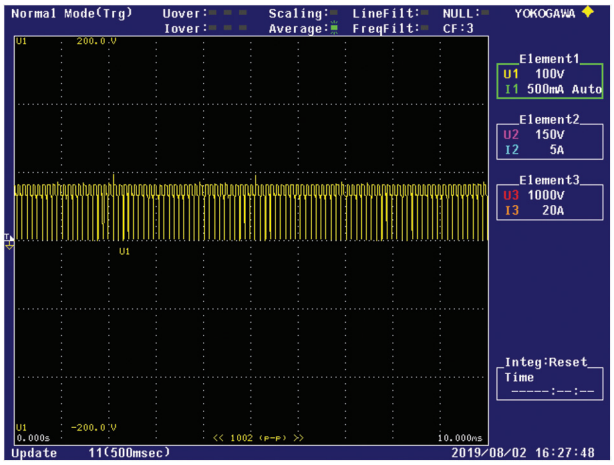


Figure 18: Waveform of the switch voltage

Table 5: Comparative analysis based on the hardware results

Topology	G	CfU1 (%)	V_{ds}	V_{cs}	V_{ss}	η (%)
Boost	1.1	1.4	0.5	1.2	1.1	73
ZSC	1.1	0.5	0.2	1.15	1.15	75
Type-1	1.2	1	0.4	1.16	1.15	79
Type-2	1.3	1.01	0.2	1.14	1.13	74
Proposed	1.3	1.04	0.1	1.09	1.09	81

Table 6: Comparison between simulation and hardware results

	Simulation values						Hardware values					
Topology	G	CfU1 (%)	V_{ds}	V_{cs}	V_{ss}	∩ (%)	G	CfU1 (%)	V_{ds}	V_{cs}	V_{ss}	∩ (%)
Type-1	1.17	0.23	1.31	1.18	1.38	88.45	1	1	1.4	1.16	1.15	79
Type-2	1.3	2.1	1.18	1.16	1.34	87.01	1.3	1.01	1.2	1.14	1.13	74
Proposed	1.3	1.4	0.99	1.14	1.32	89.39	1.3	1.04	0.1	1.09	1.09	81

6 Conclusion

In this paper, a new QZNC with low switching noise has been proposed. The problem associated with the existing type-1 and type-2 QZNC is drooping voltage gain profile and higher voltage stress across the impedance network and power device. This has been overcome in the proposed topology using current controlling diode. The working principle and design equations are clearly presented. The performance of the proposed QZNC has been evaluated and compared with the existing topologies such as boost, ZNC, type-1 QZNC and type-2 QZNC. The parameters accounted for analysis are voltage gain, load voltage ripple, capacitor voltage stress, diode voltage stress, device voltage stress, and efficiency. From the analysis, it could be inferred that the suggested converter topology has linearly high voltage gain profile, low load voltage ripple, reduced voltage stress across the network and power device, and higher efficiency. Compared with other topologies, the stress across the network as well as across the devices is reduced with the proposed topology. The laboratory model of the proposed topology has been constructed and evaluated to validate the simulation results. The practical analysis also clearly concludes that the performance of proposed converter is superior to the type-1 and type-2 converter. Hence, the proposed QZNC is suitable for high power applications such as electric vehicle charging station.

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