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Interleaved Boost Integrated Flyback Converter for Power Factor Correction in Brushless DC Motor Drive

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Abstract: The scope of this research is to manage the speed of Permanent Magnet Brushless DC Motor Drive (PMBLDCMD) for various less capacity applications. In the circuit, a 1ϕ AC power is given to Diode Rectifier and the converted DC supply is given to condenser, which leads to abnormal pulsating current. Because of this pulsating current, the power quality disturbances arise at the supply point. Hence, the PMBLDCMD requires Power Factor Correction (PFC) converter for many household and profitable applications. The rotors of PMBLDCMD are driven by 3ϕ voltage source inverter (VSI), which performs electronic commutation. The range of PFC converter for feeding PMBLDCMD has high emphasis on the power quality (PQ) norms, cost and performance of controllers. The proposed converter requires very less components, which imposes less stress, low ripple and less power loss with positive voltage polarity. The chopper is used to correct the power factor. Various chopper layouts like buck boost Converters and boost converters with single switch are used. The mostly used regulated structures for PFC converters govern the current with continuous conduction technique and to govern the potential differential tracker using discontinuous conduction method (DCM). The processes like examining, modelling and governing of PFC converters are applied for upgrading the quality of power in AC supply.

1 Introduction

The PMBLDCMD is broadly applied in less and medium power applications as it has various advantages such as broad selection of speed control, elevated power to weight ratio, high efficiency, low magnetic interference and high rigidity. Hence, it is used in various household and commercial applications like as fans, pumps, spindle, hybrid vehicle, aerospace [1–3]. The conventional motors like Synchronous motor and Induction motors are restricted for some high applications. As these motors occupy large spaces and brushes, extensive care is required, which increases the cost in a wider range. To overcome all these issues, the PMBLDCMD is utilized. This motor has some other special names like, Synchronous DC Motor and Electronically commutated motor. It resembles the synchronous machines

with 3ϕ stator coils and permanent magnet. In addition, it is fed by DC supply through an inverter [4–7]. The machine is electronically commutated by 6 switches in VSI (Voltage Source Inverter). However, the main disadvantage of BLDCM drive is its complexity. The motor is operated only when the rotor position is known. The rotor's location is captured by a sensor, which makes the system complex and it leads to an increase in economy. To overcome this, the sensorless BLDCM drive is used. The voltage source V_s, is given to the BLDCM drive through the converters and filter. By using DBR (Diode Bridge Rectifier), the dc is switched from ac with the help of a filter to curtail the ripples. Along with that, the power factor is corrected by using BIFRED (Boost Integrated Flyback Rectifier Energy Storage DC-DC) converter. The output of BIFRED converter is provided as a source to the voltage source inverter [8–12]. This voltage source inverter converts DC to AC by using six switches and the output signal is connected with the 3 terminals (ABC) of BLDCM drive. The terminal voltage from the BLDCM drive is given to the terminal voltage sensing and then the output hall signals are given to the digital signal processor (DSP).

The PFC converter functions in 2 ways like CICM (Continuous Inductor Current Mode) and DICM (Discontinuous Inductor Current Mode), in which the CICM is operated when the DC supply voltage, current in the input side and potential difference across DC link are continuous. High amount of sensing is mandatory and so it is applied in average and high power applications. In this mode, the impact on PFC converter is minimized. When the DICM is used, only DC link potential is enough for sensing the potential and so it is used in low power applications. However, the stress in PFC converter is increased.

The BLDC motor drive is fed by AC main through BIFRED, the power quality is improved. The unity power factor is achieved as the voltage ripples and THD (Total Harmonic Distortion) are reduced with help of Interleaved BIFRED converter. To achieve the expected functions, it requires a DSP with high speed and to increase the computational algorithm time, the PLL (Phase Locked Loop) observer is used. The chopper based control of VSI is used to adjust the motors mean voltage for controlling the speed [13–15]. With the help of the electronic communication of BLDC motor, the switching frequency is limited for the switching loss of VSI. The phase lead and the falls detection based on virtual hall signals are operated by using a hysteresis based technique. Here, a zero crossing detection (ZCD) is employed, which leads to increase in component.

In paper [16], the authors explains about the AC-DC converters, which are operated in solid state switching mode with the high frequency transformer. This model is acquired with the help of buck, boost or buck-boost configuration and so the THD and power factor correction is improved. Moreover, the usage of high frequency isolation transformer increases the system maintenance cost. In [16], the BLDCMD with Buck-Boost converter is operated with adjustable speed by the PFC of bridgeless buck-boost converter. The THD and PFC are improved in a wider range. In addition, the bridgeless circuit provides less cost. According to this research, the range of speed control is performed at discontinuous inductor current mode but the hall sensor in BLDCM drive makes the system complex, which leads to high cost.

The CSC (canonical switching cell) converter is used for rectifying the specified issues. The BLDCM drive is used to vary the speed by using this CSC converter. Here, this converter gives the non pulsating input current to the motor but the converter is costlier than the normal converters. The sensorless mode to find the position of rotor in BLDCM makes the system costlier [17,18]. In [19], the sensorless BLDCM in the origin crossing recognition of back electromotive force (emf) from the difference in line potential is discussed. This takes an important task in the field of BLDCM since the sensors in the BLDCM to find out the position of the rotor is costly and makes the system complex. In this paper, the back emf depends on many factors such as number of coils in the stator, angular velocity of motor, the field with magnetic force in BLDCMD rotor. The operating speed has to be high to find out the zero crossing.

In [20], the sensorless BLDCM drive with hybrid I-F starting observer based control is explained in detail. Here, the rotor position is easily found out and the motor speed is varied. However, the power quality issue arises and the THD level is increased since the power factor correction is not done. The control is limited in this system. Thus, these major disadvantages of this work are changed in the proposed system.

In [21], the sensorless control in BLDCM drive using hysteresis comparator with high starting torque is clearly explained. The low pass filter and the hysteresis comparator are used for attaining high accuracy. The control is limited when the hysteresis control is used. These drawbacks are overcome in the proposed paper. The paper [22] explains about the technique of torque ripple diminishing in PMBLDCMD with an imperfect counter electromagnetic force. Here, the motors torque is controlled by the new torque control method, which is used in various speed control method. The noise and the ripples are minimized by using this technique. This technique is only possible for the high speed operation. The unbalanced ZCP compensation for sensorless BLDC motor is utilized, which reduces the torque and current ripple in the system. The zero crossing point is found out by utilizing the back emf method. It requires voltage in dc link, terminal potential difference and the flow of current in the line. Thus, it depends upon many parameters [23].

The fault tolerance of the PMBLDC motor with torque regulation is explained. This paper mainly explains about the BLDCM torque control, which helps to reduce the torque ripples. To avoid the fault, the fault tolerance is maintained [24]. In [25], the boundary conduction mode buck PFC converter. There are various PFC converters, among which the BCM (boundary conduction mode) converter operates in the buck configuration. Thus, the buck-boost configuration is used in this proposed model.

2 Proposed Interleaved BIFRED Converter for PMBLDCMD

The proposed model of Interleaved BIFRED converter for BLDCMD is indicated with respective to Fig. 1. The 1ϕ AC source is driven to DBR by an interleaved BIFRED converter with PFC. The Interleaved BIFRED converter is modelled to work at triple DICM. The VSI gets the input from PFC converter, in which the result signals of the VSI are given to the PMBLDCM drive. The aim of the intended setup is to attain the broad span of speed regulation. To accomplish the speed governing, the DC bus potential difference of VSI is varied. To minimize the switching losses in VSI for better electronic commutation, basic switching rate is performed. These three terminals of the drive are powered by the VSI and the output from the BLDCM is given to the sensorless unit or virtual hall signal generation unit. Moreover, this proposed model of sensorless setup contains circuit with voltage sensor, hysteresis comparator, an isolation circuit, phase-lead compensator and the negative clipper circuit. Thus, the design of the sensorless unit, which produces virtual hall signals to calculate the position of the rotor is visualized at Fig. 2.

The components in the circuit design of virtual hall signal generation unit are described below. A resistive potentiometer gets the terminal voltage from the PMBLDCMD and it is used to step down the terminal voltage of BLDCM for keeping the similarity with the analogue Integrated Circuit. This step down potential is drawn to the phase lead compensator. Because of the hysteresis comparator and sensing circuit, the phase lag is eliminated in the virtual hall signal approximation. Then, the output of the lead phase is driven to the hysteresis comparator, in which the zero crossing detection (ZCD) is done to remove the commutation ripple. To neglect the error switching conditions, the range of hysteresis comparator is preferred as less phase change is achieved in allowed range. The negative half cycle is clipped from negative clipper, which is driven by output from comparator. It is connected to the opto-isolator, in which the isolation is optically done within the DSP and power signal condition circuit. Fig. 3 shows the graphs of the counter emf's, with definite (HA-H$_C$) hall signals and necessary hall signals.
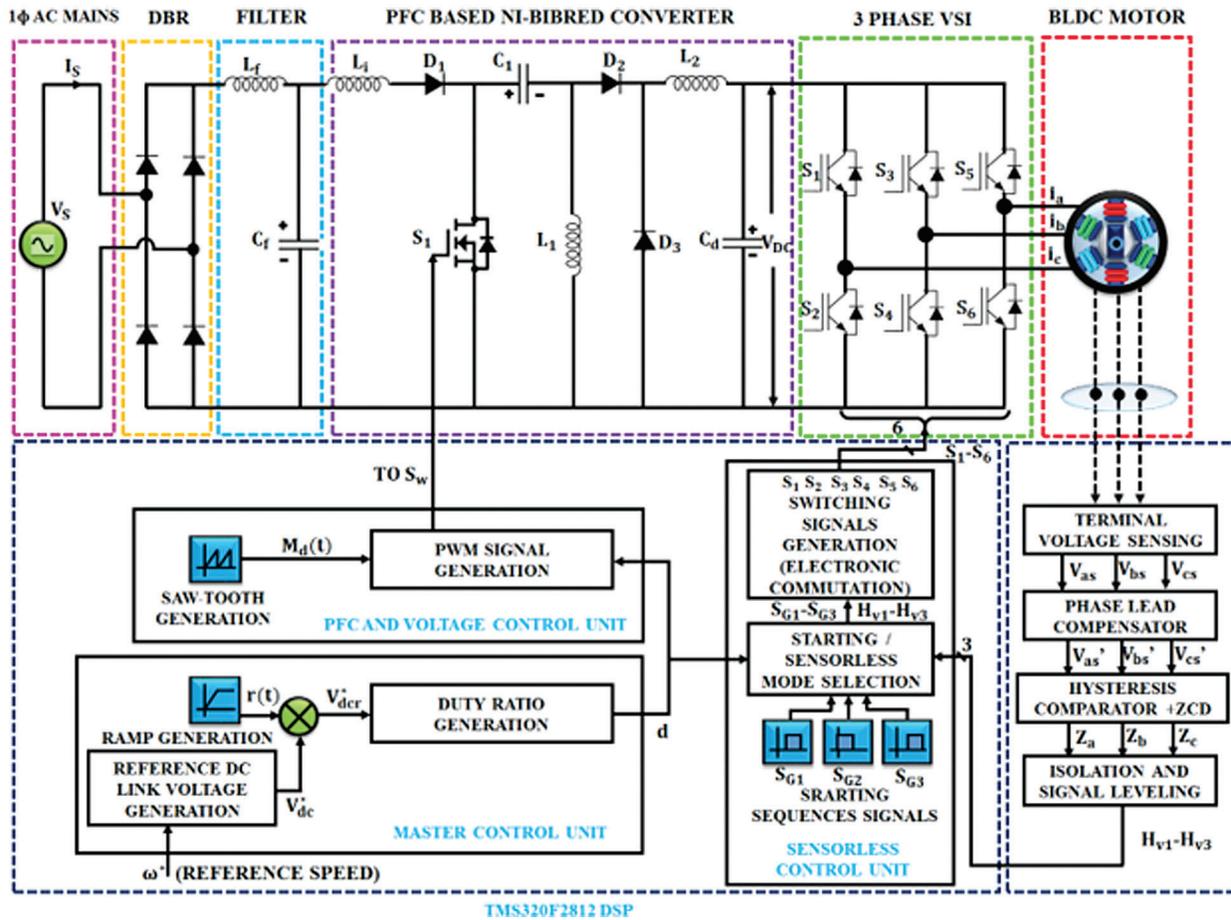
Figure 1: Circuit design of interleaved BIFRED converter for BLDCM drive

3 Design of BLDCM Drive

The BLDC motor is expressed by the 3Φ motor equations, which are written below as,

$$V_a = i_a R_a + L_a \frac{dia}{dt} + M_{ab} \frac{dib}{dt} + M_{ac} \frac{dic}{dt} + e_a \tag{1}$$

$$V_b = I_b R_a + L_b \frac{dib}{dt} + M_{bc} \frac{dia}{dt} + M_{bc} \frac{dic}{dt} + e_b \tag{2}$$

$$V_c = i_c R_c + L_c \frac{dic}{dt} + M_{cb} \frac{dib}{dt} + M_{ca} \frac{dia}{dt} + e_c \tag{3}$$

where, the resistance in the stator per phase is indicated by R which is implicit to be similar for all phases, the inductance in stator per phase is represented by L and the mutual inductance in between phases is denoted by M.

It is assumed that the self inductance of stator is non-aligned to the spot of the rotor. Thus,

$$L = L_a = L_b = L_c \tag{4}$$
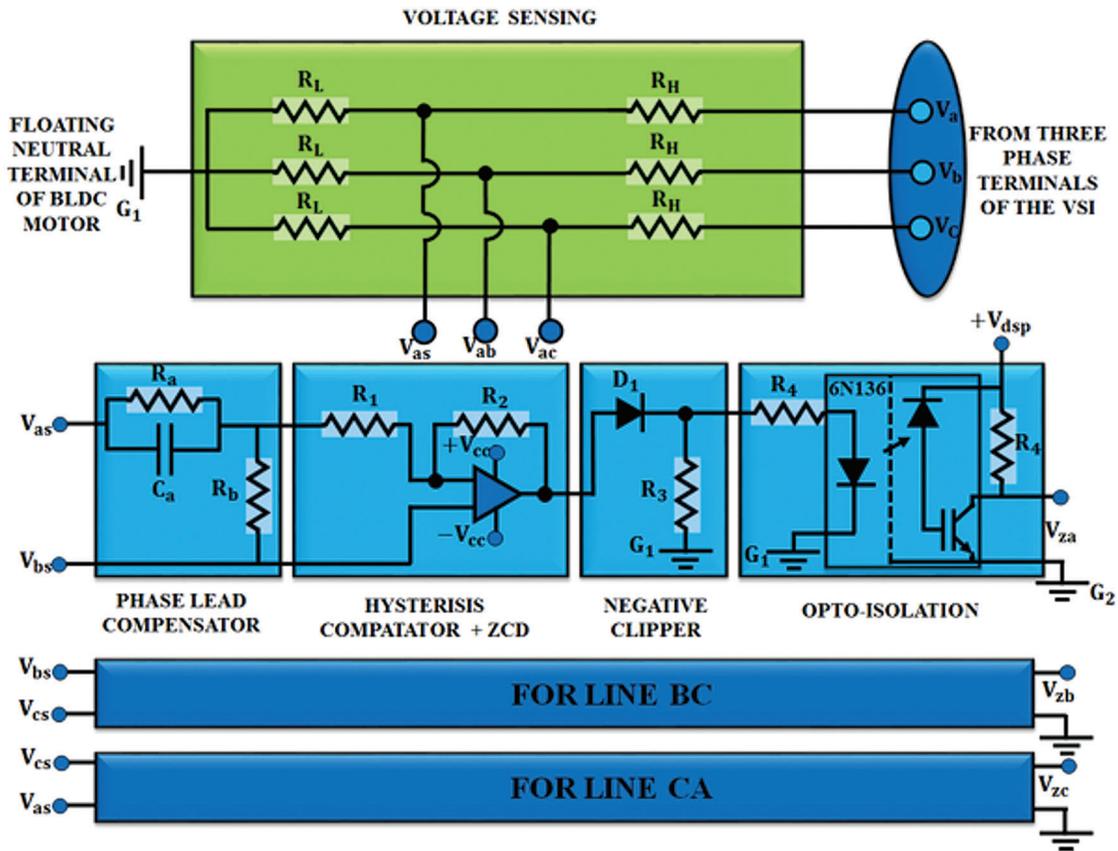
Figure 2: Generation of virtual hall signal circuit diagram
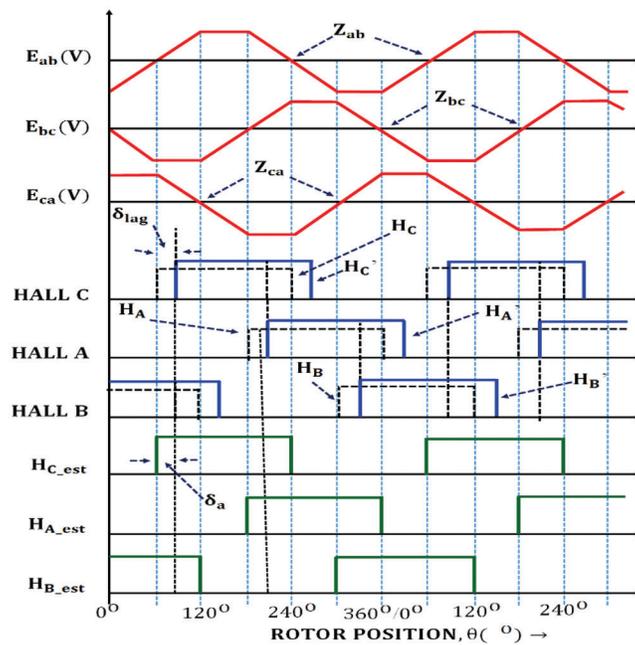
Figure 3: Output with compensation of line counter emf *vs.* actual and estimated hall signals

The mutual inductances is represented as,

$$M = M_{ab} = M_{ac} = M_{ba} = M_{bc} = M_{ca} = M_{cb} \tag{5}$$

The phase resistances are considered to be same since the system is considered as phase balanced system. Therefore,

$$R = R_a = R_b = R_c \tag{6}$$

The formulae (4)–(6) indicate the mutual inductance. If it is neglected, the motor equations are rewritten as,

$$V_a = i_a R + L\frac{dia}{dt} + e_a \tag{7}$$

$$V_b = I_b R + L\frac{dib}{dt} + e_b \tag{8}$$

$$V_c = i_c R + L\frac{dic}{dt} + e_c \tag{9}$$

4 Design of Interleaved BIFRED Converter

The interleaved BIFRED converter works under triple discontinuous current period. Due to the switch, the current becomes discontinuous by the inductors. Five different processes are briefly explained in in the subsequent part.

Mode 1: At this stage, turn on the switch S_1 and so the current passes from the source towards the inductor L_i. The inductor L_1 charges from the capacitor C_1, since the capacitor C_1 is discharged. The C_d gives the necessary energy to BLDCM drive. The inductor L_2, diodes D_2 and D_3 are not conducting.

Mode 2: In this stage, turn off the switch so that current begins to decrease in inductor L_i and L_1. Because of this decrease, there is charging in the capacitor C_1, inductor L_2 and dc link condenser C_d. The voltages of capacitors and inductor get increased.

Mode 3: The inductor current is in discontinuous current mode because the inductor L_2 becomes zero. The inductors L_i and L_2 keep on discharging whereas the capacitors C_1 and C_d continues to charge. This happens in mode 3.

Mode 4: At this time, the middle capacitor C_1 is still charging and the inductor L_2 current become zero and comes to DICM again. Therefore, the BLDCM drive is powered by dc link condenser C_d. This operation is done in mode 4.

Mode 5: Here, the inductors L_i, L_1, L2 are fully drained and so the only source of BLDCM drive is dc link capacitor, which provides energy to the motor. Because of this, the voltage falls within dc link capacitor and it persists to decrease.

These are the five modes of operation on DICM of interleaved BIFRED converter. The inductors and capacitors are designed to make the BIFRED converter to operate in DCIM mode as PFC converter. Thus, for a 310 V 1HP PMBLDCM drive, the interleaved PFC based BIFRED converter is modified by using the following equations,

The supply voltage is derived from the equation shown below,

$$V_s = V_m * \sin(2 * \pi * f_L * t) \tag{10}$$

here,

V_m stands for peak input potential difference.

f_L stands for Line frequency

V_{in} is said to be input average voltage

D represents the duty ratio

f_s represents switching frequency, I_{in} represents average input current.

$$V_{in} = 2 \frac{V_m}{\pi} \tag{11}$$

For the buck-boost converter specification, the potential difference in dc link is given by,

$$V_{dc} = \left[\frac{D}{(1-D)} \right] V_{in} \tag{12}$$

The input inductance Li and output inductance's L_{oc} critical value is given by,

$$Li = \frac{VinDdes}{2Iinfs} \tag{13}$$

$$Loc = \frac{Vdes(1-Ddes)}{2Iofs} \tag{14}$$

The intermediate and the dc link capacitance are found out by using the following formulae,

$$C_1 = \frac{VoDdes}{RLfs\Delta Vc1} \tag{15}$$

where R_L is known as equivalent emulated resistance.

$$C_d = \frac{Iomin}{2\omega L \Delta Vdcmin} \tag{16}$$

The $\Delta Vdcmin$ has to be taken as 2.5%, which is known as tolerated rise and fall in the potential difference at dc link. The ceiling value of capacitor is found out by using the higher value of current, peak input voltage, displacement angle and the angular velocity of the rotor.

Finally, the filter inductance calculated by using the expression,

$$L_f = \frac{1}{4\pi^{2}fc^{2}Cf} \tag{17}$$

5 Phase Lead Compensator Model

The delay in the phase or the balanced phase is minimized by the use of phase lead compensator before the operation of hysteresis comparator. Thus, measuring of phase delay in zero crossing between line counter emf and waves from hall sensor is done. Regarding the estimation, the phase-lead compensator is modeled as,

$$G_c(s) = a \left(\frac{s + \omega c1}{s + \omega c2} \right) = a \left(\frac{s + 1/aT}{s + 1/T} \right) \tag{18}$$

Two corner frequencies are represented by $\omega c1$ and $\omega c2$. There are two time constants a and T. These constants are found out by using the formulae, which needs angle at phase lead and rate of phase lead angle at

maximum point.

$$a = \frac{1 + \sin{(\varphi m)}}{1 - \sin(\varphi m)}; \quad T = \frac{1}{\omega m \sqrt{a}} \tag{19}$$

The transfer function of the compensator with realized RC network is given by the following equation,

$$G_c(s) = \frac{s + (1/RaCa)}{s + \left(\frac{1}{RaCa} + 1/RbCa\right)} \tag{20}$$

The bode plot has been plotted to get the desired frequency by using the required phase delay in the phase-lead compensator. By using this, the designed compensator has an error less than 0.5%. The phase lead compensator is calculated and the governing of projected motor drive is described in the subsequent part.

The major functions of BLDCM drive are to correct the power factor and to reduce the THD by eliminating voltage ripples by using the sensorless control.

The rotor's velocity in BLDCM is related directly to the dc link potential difference. By knowing the velocity, the reference voltage has been generated. The generated reference potential difference in dc link side is expressed as,

$$V*_{dc} = K_v \omega* \tag{21}$$

where, K_v represents the voltage constant of BLDCM drive. From the above equation, the potential difference in dc link is calculated. The generated duty ratio is specified into the PFC control, sensorless control and voltage control to gain the sensorless work. The ramp signal is multiplied with the potential difference in dc link, which steadily increases the reference potential difference. When the motor starts to rotate, it gives enough time for the position of rotor alignment.

The switch in the PFC converter is triggered and the wave with PWM (Pulse Width Modulation) is set to the PFC converter to continue the chosen potential difference with DC bus side. From the master control, the preferred duty ratio is attained. By this, the power factor correction is done on the main supply without the alteration in current sensing equipment or voltage sensing equipment.

The pulses from the switching signals are given to the VSI to operate the BLDCM and to identify the rotor position. The virtual hall signals are found out by using these sensorless signals. This mode is used by various selection modes such as synchronization, sensorless mode and sensorless starting. By holding the current state, the switching state gets varied. The commutation failure is overcome by synchronizing the pulses with the other blocks. Three types are explained in the following part. At first, the position of the rotor alignment, turning on the two switches at VSI are assessed. The pulse is given to the motor to initially assign the rotor position. This is done to verify the position of the rotor to operate in sensorless mode. The six switch pulses in VSI are given sequentially with low frequency, which ranges from 10–15 Hz since the voltage at dc link side is directly related. The current in the stator side is produced when the dc link potential difference is high. To overcome this criteria, the machine begins with less speed and low frequency range in the initial stage. Later, the speed is increased. Finally, the desirable counter electromotive force is produced by the calculation of virtual hall waves. By using the above signal from the counter electromotive force detection circuitry, the motor is electronically commutated.

6 Simulation and Hardware Results

The interleaved BIFRED converter for BLDCM drive is analyzed and the simulation result of BLDCM drive with interleaved BIFRED converter is discussed in the subsequent section. Here, the power factor

correction is done. The voltage ripples and harmonics are reduced, which leads to the reduction in the THD value.

The source current and voltage are found to be sinusoidal in nature as these are not affected by the motor drive load. The amplitude of input potential is 220 V and current amplitude is 1.5 A.

The proposed converter is designed to meet the power factor specification as mentioned in the description. Fig. 4 indicates the input ac source current with the power factor correction converter. It is a single phase sinusoidal waveform with 1.5 A current. Fig. 5 describes the AC source voltage with 210 V. Its corresponding hardware results are depicted in Fig. 6.
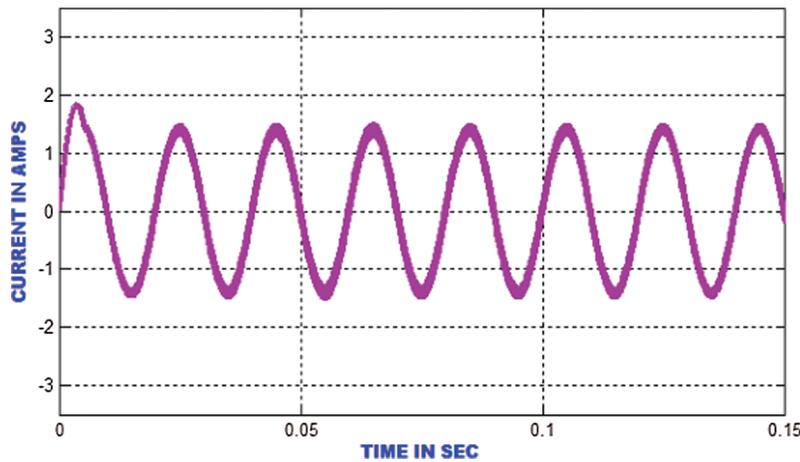
Figure 4: Input AC source current waveform with AC-DC PFC converter
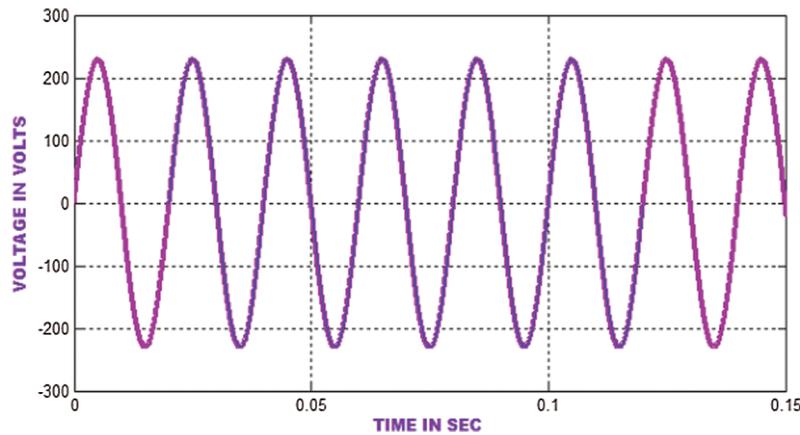
Figure 5: Waveform of input AC source voltage
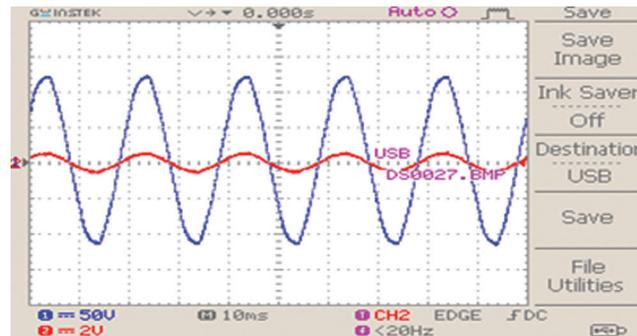
Figure 6: Hardware results of input voltage and current waveform

The BLDCM current for the described model is 3 A and the current settles at 0.1 s, which is graphed in Fig. 7.
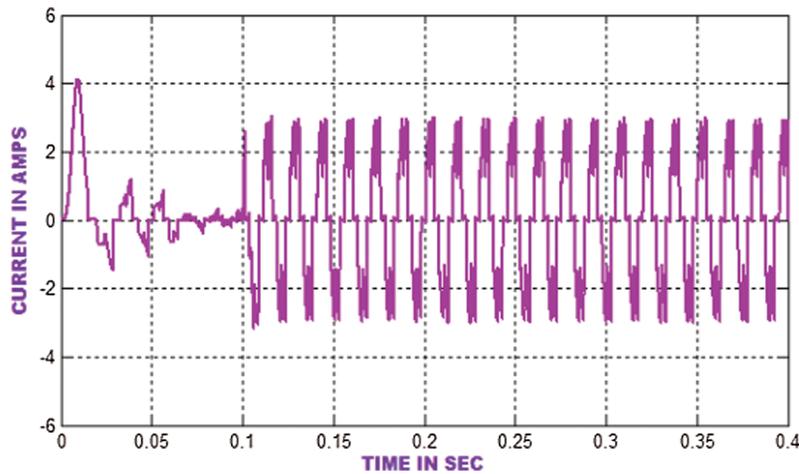
Figure 7: BLDC motor current output

The PMBLDCMD current waveform is plotted in Fig. 8 whereas the torque waveform is depicted in Fig. 9 and the torque waveform settles at 0.1s. The hardware outcomes of the PMBLDCMD torque waveform is represented in Fig. 10.
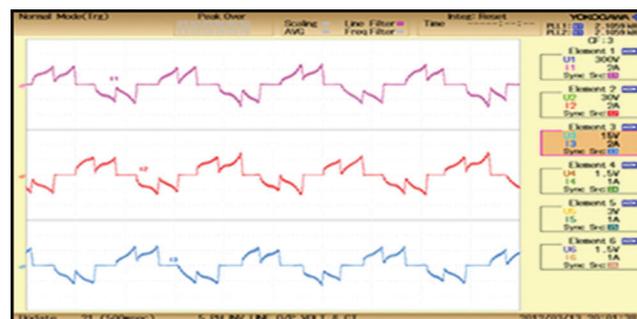
Figure 8: Hardware results of BLDC motor current waveform
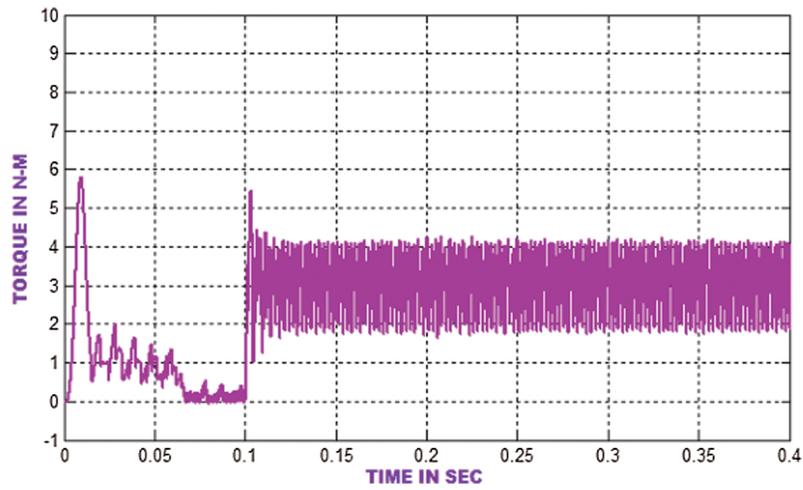
Figure 9: BLDC motor torque waveform
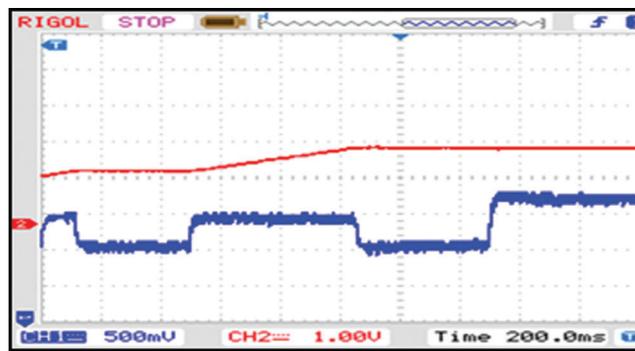
Figure 10: Hardware results of Brushless DC motor torque waveform

The output potential difference graph of the motor with PI controller is plotted in Fig. 11. Here, the accuracy is high and the peak is less than 0.01 s. The waveform settles with 200 V at 0.04 s.
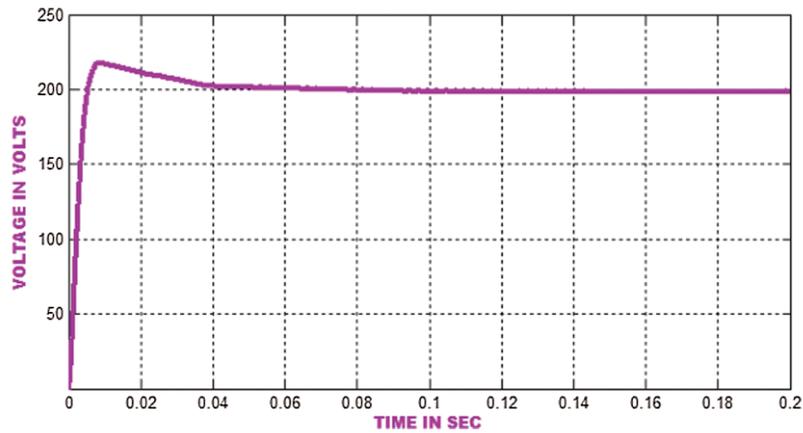
Figure 11: AC-DC PFC converter output voltage waveform with PI controller (Ref. Voltage = 200 V)

Fig. 12 signifies the hardware outcomes of AC-DC PFC Converter output voltage waveform using PI controller.
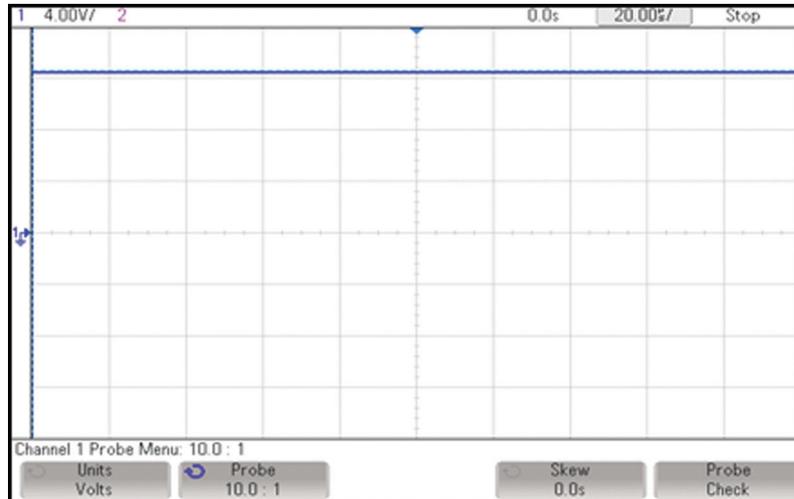
Figure 12: Hardware results of AC-DC PFC converter output voltage waveform with PI controller (Ref. Voltage = 200 V)

The Brushless DC motor speed is plotted in Fig. 13. The preferred speed is set as 1000 rpm. The rotor speed settles at 0.1 s. Here, the PI controller is employed to regulate the motor speed. The hardware outcomes of Speed in BLDCM using PI controller is highlighted in Fig. 14.
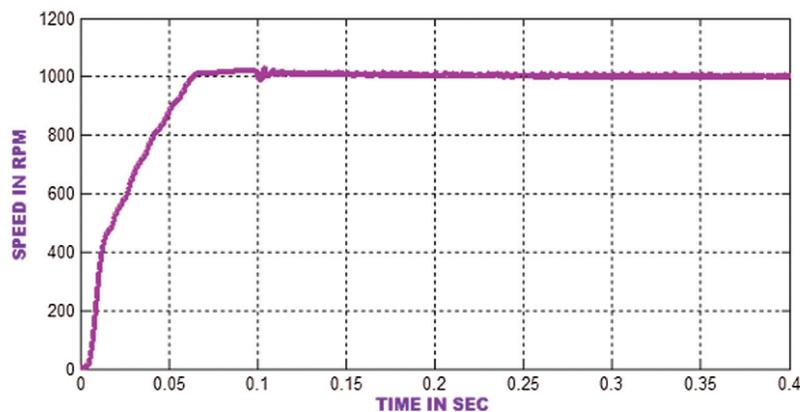
Figure 13: Speed waveform using PI controller in BLDCM (Ref. Speed = 1000 rpm)

The device's THD level is less than 2% and the PF is maintained as 1. The THD level is represented in Fig. 15.

The comparison of the proposed converter in consideration with the factors like number of components, current ripples, voltage polarity and drive complexity is shown in Tab. 1. It indicates that the suggested converter outperforms the existing converters.

The amount of power loss for different converter with different operations such as PFC, VSI and BLDC is given in Tab. 2.

Figure 14: Hardware results of speed waveform using PI controller in BLDCM (Ref. Speed = 1000 rpm)
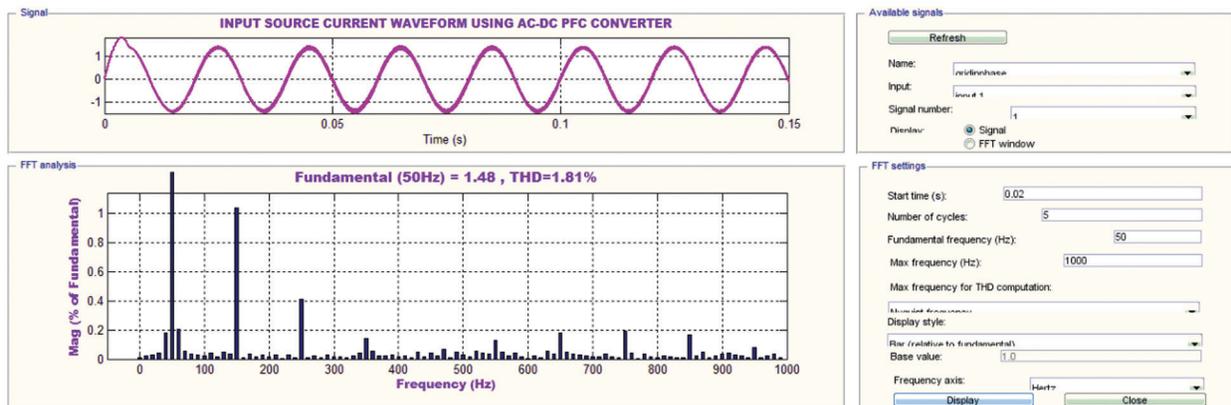
Figure 15: Harmonic spectra of Input source current waveform using AC-DC PFC converter

Table 1: Comparison for various layouts of PFC converter

Layout	Number of devices					Current ripple (output)	Current ripple (input)	Voltage polarity (output)	Complexity of drive
	S_w	D	L	C	Tot				
BL Buck-Boost [10]	2	4	2	1	9	High	High	Negative	High
BL Cuk [12]	2	4	4	3	13	High	Low	Negative	Low
BL SEPIC [13]	2	4	4	3	13	High	Low	Positive	Low
BL Zeta [14]	2	4	4	3	13	High	High	Negative	Low
BL Luo [15]	2	4	4	3	13	High	High	Negative	High
BL CSC [17]	2	4	2	3	11	High	High	Negative	High
Landsman	2	4	4	3	13	Low	High	Negative	High
Proposed BIFRED	1	3	3	2	9	Low	Low	Positive	Low

Table 2: Study of power losses at different stages and comparison with various layout of PFC converter

Layout	Power loss percentage (%)					
	CSC		Landsman		BIFRED	
	200 V	60 V	200 V	60 V	200 V	60 V
PFC	6.00	13.25	5.40	9.25	5.25	8.75
VSI	7.25	9.25	7.25	8.75	7.10	8.50
BLDCM	8.00	9.00	8.00	9.00	7.85	8.25
Total	21.75	32	21.1	27.50	20.85	18.80

The entire work is experimentally investigated as illustrated in Fig. 16. The comparison of peak-to-peak voltage and current stresses is given in Tab. 3, which depicts that the proposed converter has less stress than other converters.

Figure 16: Experimental setup for proposed system

Table 3: Study of switch stress and comparison for different layout of PFC converters

Layout	Voltage stress (peak to peak voltage)	Current stress (peak to peak current)
CSC	500 V	28 A
Landsman	490 V	27 A
BIFRED	475 V	26 A

7 Conclusion

The interleaved BIFRED converter for BLDCMD with PFC is designed and analyzed in this study. This is done with Simulink assistance and the simulation outcomes are discussed with prior validations. Here, the PFC converter is used to maintain the unity power factor. The voltage ripples and harmonics are eliminated to

decrease the THD level. The usage of sensorless BLDCM drive makes the cost of hardware system effective. In addition, the maintenance and complexity of the motor are reduced with the assistance of virtual hall signal production. In future, the PFC converter is possibly done with DTC (Direct Torque Control) sensorless mode for high power usages.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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