

Image Denoising Using a Nonlinear Pixel-Likeness Weighted-Frame Technique

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Abstract: Recent advances in the development of image denoising applications for eliminating the various sources of noise in digital images have employed hardware platforms based on field programmable gate arrays for attaining speed and efficiency, which are essential factors in real-time applications. However, image denoising providing for maximum denoising performance, speed, and efficiency on these platforms is subject to constant innovation. To this end, the present work proposes a high-throughput fixed-point adaptive edge noise filter architecture to denoise digital images with additive white Gaussian noise in realtime using a nonlinear modified pixel-likeness weighted-frame technique. The proposed architecture works in two stages. The first stage involves normal and conditional sorting. The second stage is a decision-oriented output selection unit. Decision-oriented adaptive windowing is included for better impulse noise suppression and edge preservation. The denoising performance of the proposed denoising scheme is demonstrated to be superior to those currently available state-of-the-art approaches. Moreover, the power consumption is reduced by 25.01% compared to conventional algorithms.

Keywords: Adaptive edge noise; additive white Gaussian noise; image denoising; PLWF; peak signal-to-noise ratio

1 Introduction

The Discrete Wavelet Transform (DWT) of a noisy image includes a substantial number of factors with low SNRs, and shrinking the wavelet coefficients associated with these DWT factors with low Signal to Noise Ratio (SNRs) was demonstrated to be a useful procedure for denoising images, particularly those with additive white noise. In addition to digital images, the good performance of DWT-based denoising strategies has made these strategies useful for speech signals, electrocardiograms (ECGs), and encephalograms [1–4]. Like many recent implementations of image processing, DWT-based image denoising is executed on Field Programmable Gate Array (FPGA) platforms owing to their good computational performance and low resource consumption. In addition, these developments have focused mainly on the convolution method. The denoising method utilizing DWT consists of three stages: forward DWT (FDWT), adaptive thresholding, and inverse DWT (IDWT). While recent advances in the



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development of DWT-based image denoising employing hardware platforms based on FPGAs have attained high computational speed and efficiency [5–7].

To this end, the present work proposes continuous use of the forward/backward pixel likeness weighted frame (PLWF) technique for image denoising. The proposed method is planned and executed on an FPGA platform utilizing the Xilinx System Generator (XSG), MATLAB 2017a, and the XUP Vertex-II Pro improvement board. The Pixel Likeness Weighted Frame (PLWF) is employed in conjunction with a modified Adaptive Edge Noise (AEN) filter to minimize noise such as salt-and-pepper and Gaussian noise [8]. The algorithm employs two stages: separating the filtering windows into four orthogonal edge direction patterns and the identification of the ideal directions of the edges, which are those with highly indistinguishable pixels. Knowledge regarding the ideal directions of the edges enables the identification of more edge pixels, which helps to reduce edge degradation during the denoising process. To this end, the present work adopts the average deviation from the mean (i.e., the standard deviation) because it yields better outcomes than the difference or change in other methods for estimating the noise levels of pixels [9–13].

2 Materials and Methods

A block diagram of the proposed PLWF image denoising algorithm is presented in Fig. 1. Its architecture consists of five principal blocks, which include odd and even line buffers, register bank, threshold determination, and an AEN filter. These are presented in detail as follows.

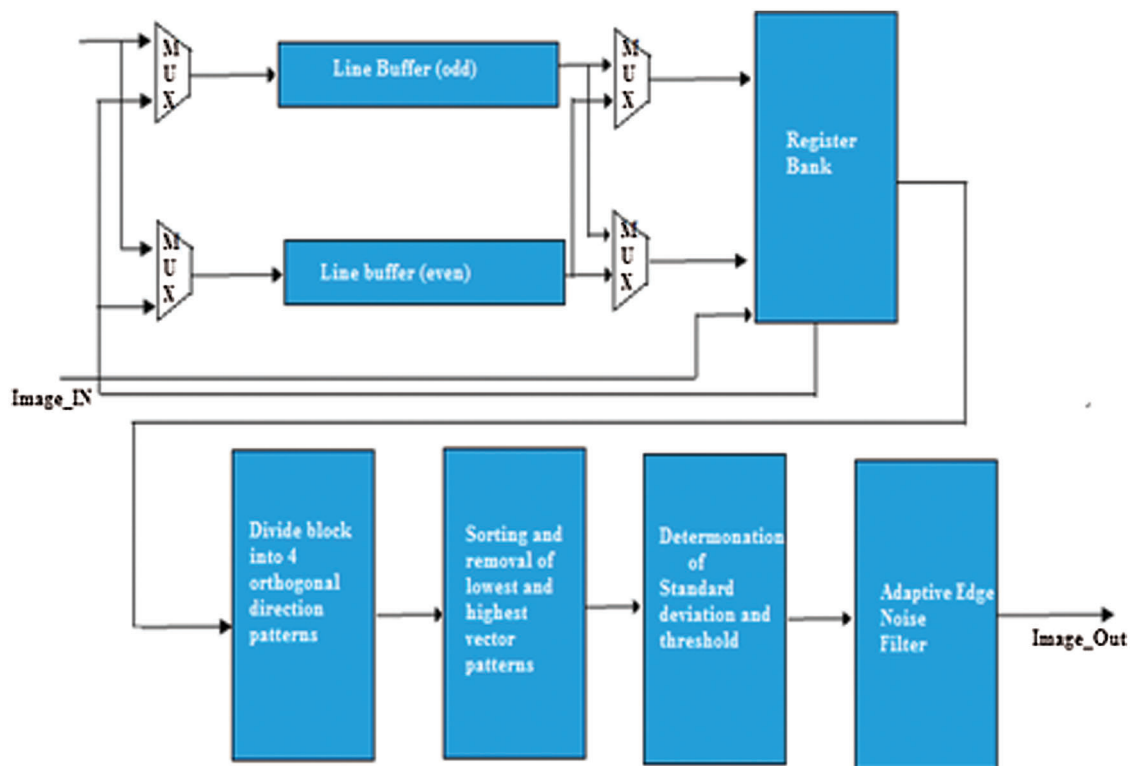


Figure 1: Block diagram of the PLWF image denoising scheme

A. Line buffers

The proposed algorithm employs a 3×3 convolution mask. Therefore, the computation is facilitated by four hybrid multiplexers and two line buffers, where the odd and even line buffers store pixels at odd and even column positions, respectively. The cost and power consumption of the implementation are reduced by adopting a double-port SRAM in the line buffers to conduct the computational activity [14–16].

B. Register bank

The register bank consists of 12 registers, Reg0 to Reg11, that accumulate the 3×3 pixel estimates of the present convolution masks. The architecture of the line buffers and register bank are illustrated in Fig. 2, where every three registers are associated sequentially to obtain evaluations of the three-pixel rows a mask [17–21].

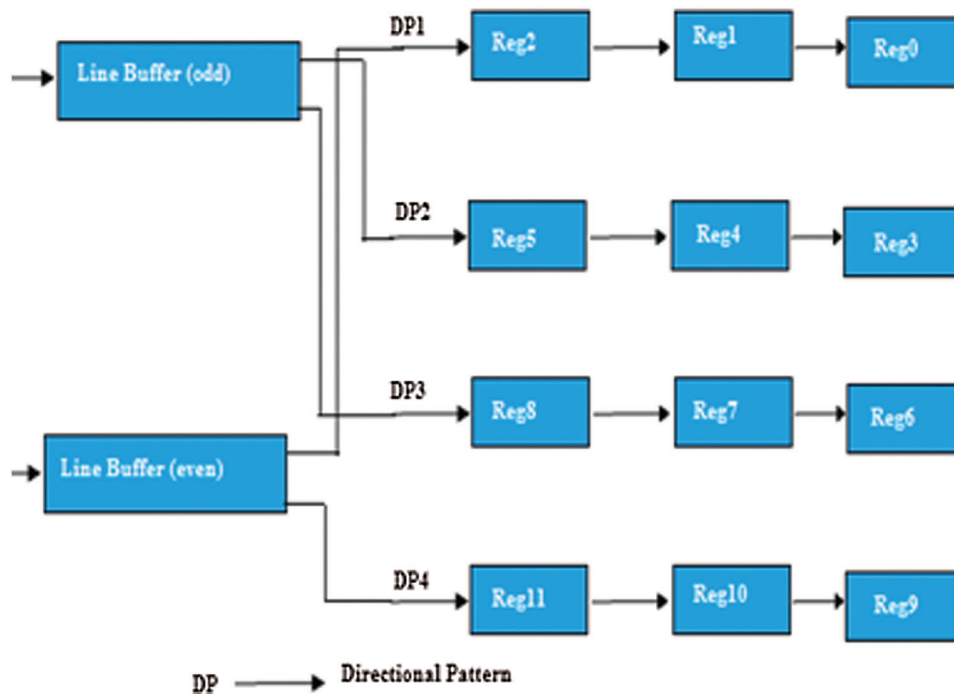


Figure 2: Architecture of the line buffers and register bank

C. Threshold block

The threshold block design is illustrated in Fig. 3. The evaluation of whether the input value is greater or lower than the threshold limit (T_s) is more important than the T_s itself. Accordingly, one clock cycle is enough for the line buffer, but two clock cycles are needed for the AEN filter during the noise removal process [22–24].

D. Adaptive edge noise filter

The two-stage pipeline design of the AEN filter is illustrated in Fig. 4. Here, the adder (ADD) unit locates the two input sources and transfers the added value to the multiplexer. The ADD modules help in locating the four orthogonal edge direction patterns composed of highly indistinguishable pixels [25–28]. The directional contrasts for the four edge directions are determined by the ADD units. At this point, the smallest distinction is chosen by the DIV/9 unit. The final block provides the mean of the two-pixel values, i.e., the output after filtering [19–31].

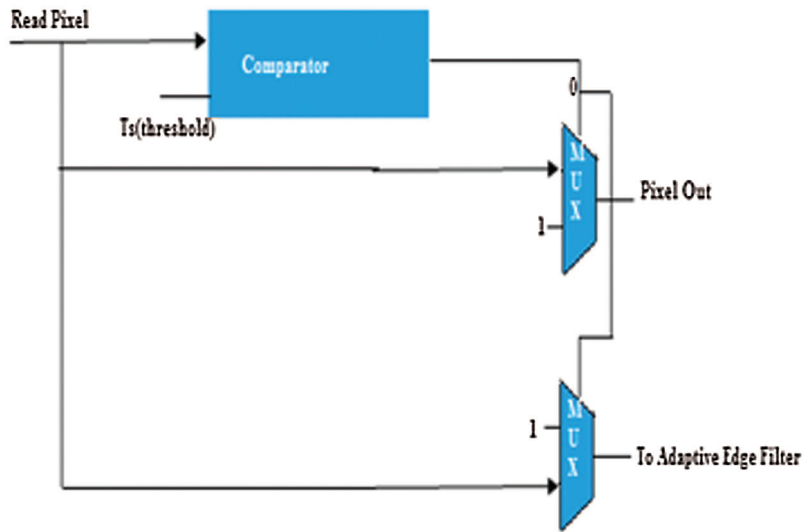


Figure 3: Architecture of the threshold block

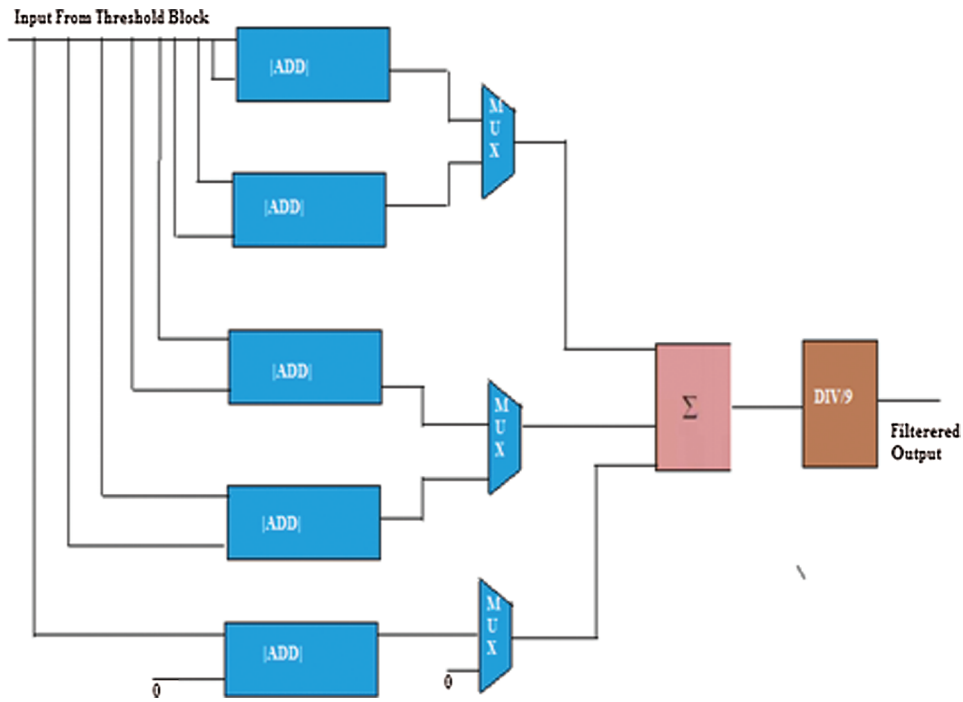


Figure 4: Architecture of the adaptive noise filter

3 Pixel Likeness Weighted Frame Algorithm

A flowchart of the proposed PLWF algorithm is presented in Fig. 5. These stages are presented in detail as follows.

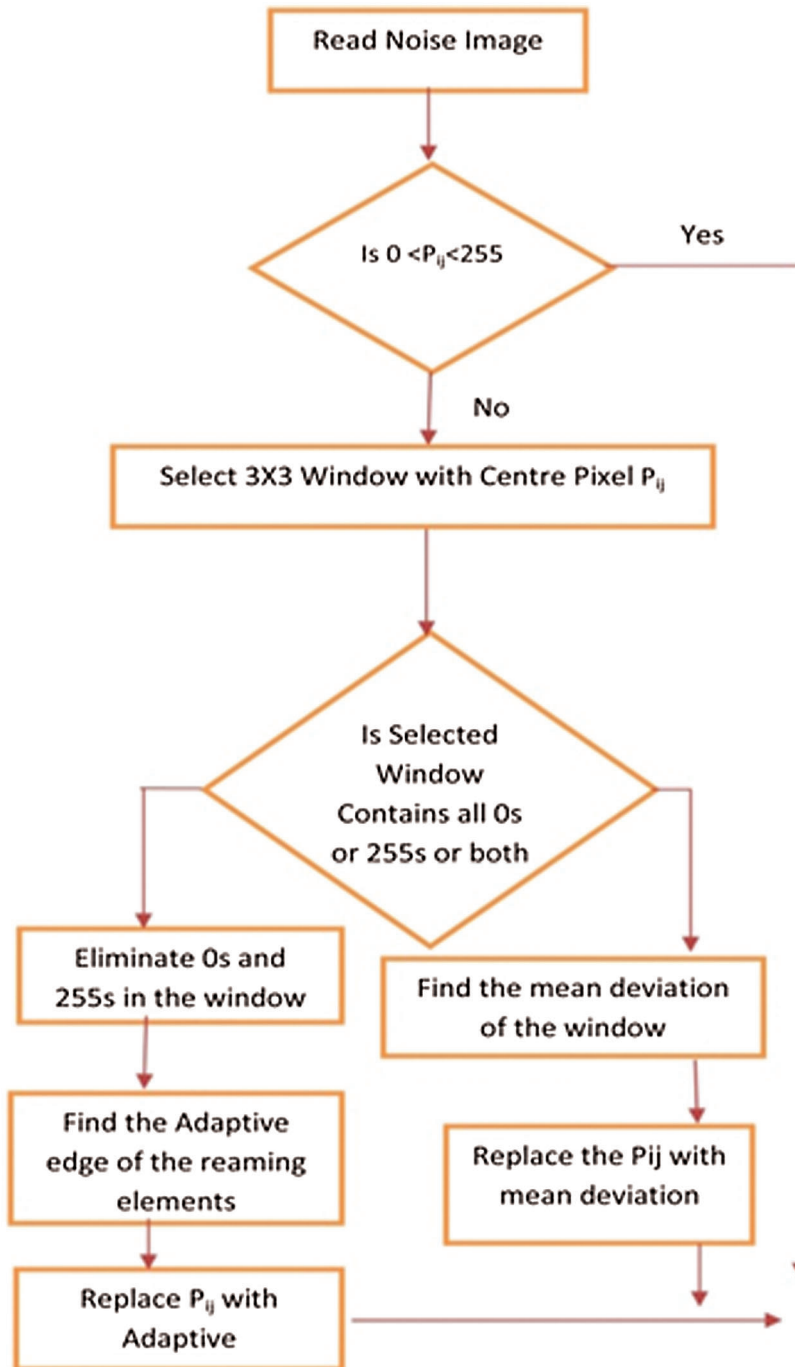


Figure 5: Flow chart of the proposed PLWF algorithm

Stage 1: Apply a two-dimensional (2D) window of size 3×3 to a center pixel with an 8-bit grayscale value denoted as P_{ij} .

Stage 2: If $0 < P_{ij} < 255$, the center pixel is considered to be uncorrupted; thus, no procedure is required and its value is left unaltered.

Stage 3: If $P_{ij} = \text{zero or } 255$, then the center pixel is corrupted by salt-and-pepper noise. This yields two possible cases.

Case I: The window includes pixels with values that are not exclusively 0 or 255. Then, find the adaptive edge of the remaining pixels and replace P_{ij} with its adaptive value.

Case II: The window includes pixels with values that are only 0, 255, or both. Then, the center pixel may be either zero or 255; again this is a small issue. Then, replace P_{ij} with the mean deviation (Fig. 5).

Stage 4: Apply stages 1–3 to every pixel in the image.

4 Results and Discussion

The performance and operational characteristics of the proposed PLWF algorithm were compared to those of various other state-of-the-art noise-removal algorithms, including iterative pixel compression (IPC), and those based on the discrete cosine transform (DCT) and the DWT. To this end, the algorithms were applied to standard Lena and Cameraman8-bit grayscale images composed of 512×512 pixels. Salt and pepper noise having pixel values of 0 and 255 with equal probability was deliberately added to all images in proportions of 10% to 90% using MATLAB. For this, a window size of 9×9 was uniformly applied.

Tab. 1 shows the evaluation parameters used in the proposed system.

Table 1: Evaluation parameters

Parameter	Specification
Dataset	Natural and raw images
Tools used	Matlab and XSG
Number of images	100
Languages	System C and HDL
Device	Vertex-2 Pro FPGA

The results of applying the proposed PLWF algorithm to the Lena and cameraman images in MATLAB are presented in Figs. 6 and 7, respectively.

The noise-reduction performances of the algorithms compared were evaluated according to the peak signal-to-noise ratio (PSNR) and mean square error (MSE), which are defined as follows [5,19]:

$$MSE = \frac{\sum_{M,N} [I_1(m,n) - I_2(m,n)]^2}{M*N}, \quad (1)$$

$$PSNR = 10 \log_{10} \left(\frac{R^2}{MSE} \right), \quad (2)$$

where M and N are the respective numbers of rows and columns in the image, m and n are the indices of the rows and columns, respectively, I_1 and I_2 represent the ground truth noise-free image and the denoised image, respectively, and R is the maximum possible pixel value in the input image (i.e., 255). Here, the noise reduction performance of an algorithm increases with decreasing MSE and with increasing Peak Signal to Noise Ratio (PSNR).

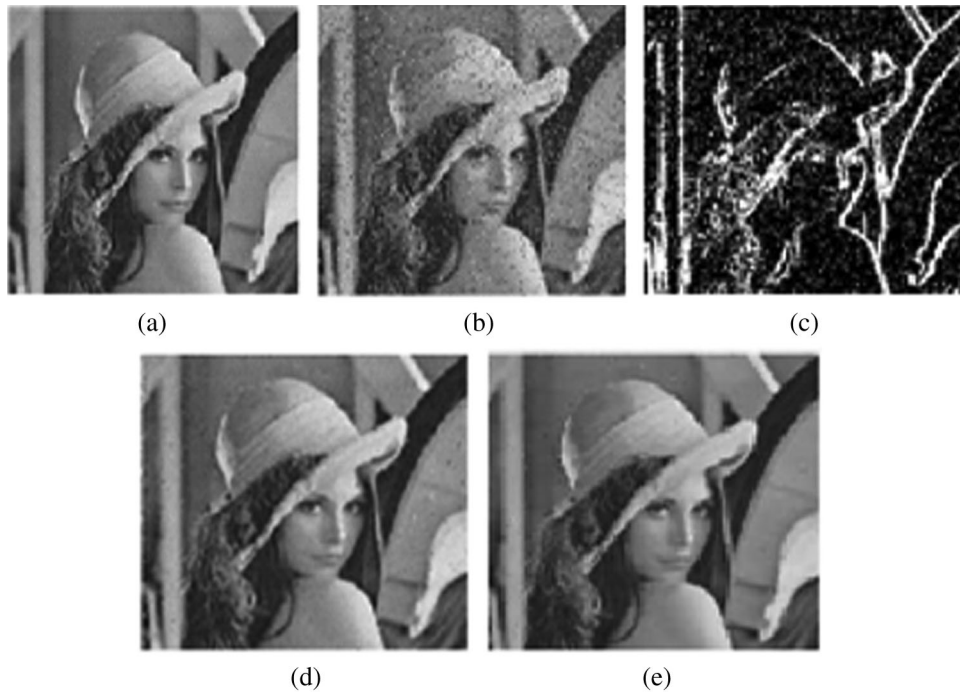


Figure 6: Results of applying the proposed PLWF algorithm to the Lena image. (a) Input image (b) Noisy image (c) Noise pixels detected (d) Denoised image (first level) (d) Denoised image (second level)

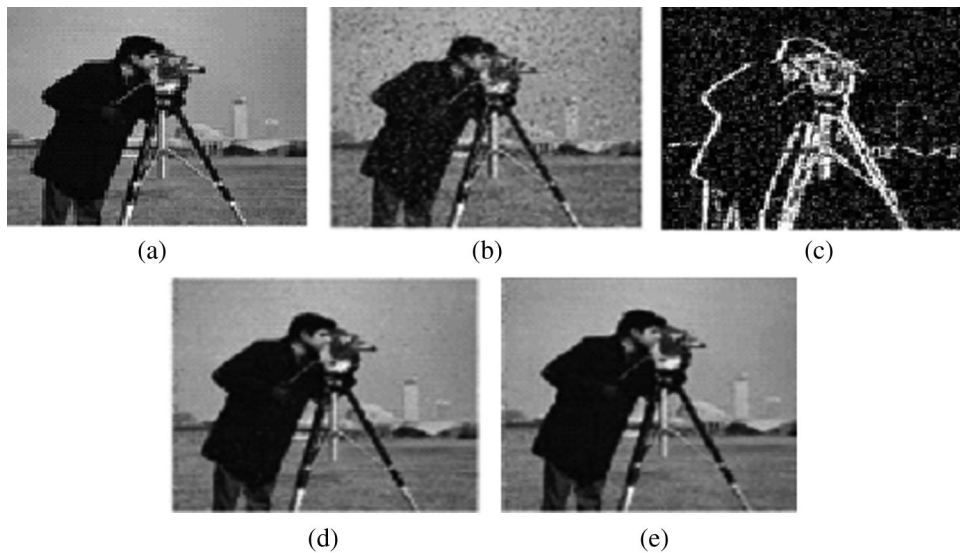
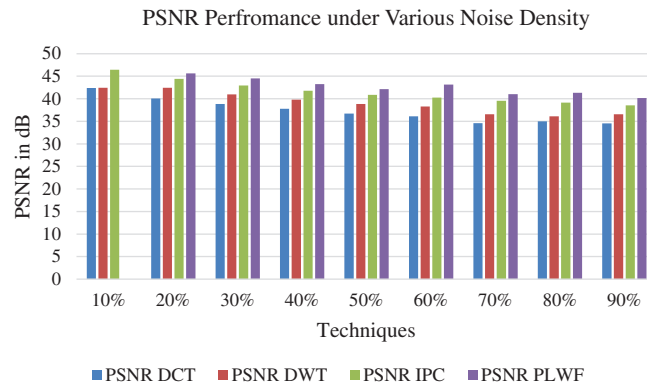


Figure 7: Results of applying the proposed PLWF algorithm to the cameraman image. (a) Input image (b) Noisy image (c) Noise pixels detected (d) Denoised image first level (d) Denoised image second level

The PSNR and MSE values obtained by the various noise reduction algorithms for the Lena and cameraman images under different salt and pepper noise levels are listed in [Tab. 2](#). In addition, we plot the PSNR values listed here in [Fig. 8](#) for a more intuitive comparison. These results indicate that the proposed PLWF algorithm provides better visual quality than the other methods considered.

Table 2: Comparison of PSNR and MSE values obtained by various noise reduction algorithms for the Lena and cameraman images under different salt and pepper noise levels

Noise level	PSNR				MSE			
	DCT	DWT	IPC	PLWF	DCT	DWT	IPC	PLWF
10%	42.39	42.46	46.46	48.62	0.02	0.02	0.02	0.02
20%	40.08	42.42	44.42	45.63	0.04	0.03	0.03	0.03
30%	38.84	40.96	42.96	44.51	0.05	0.05	0.05	0.04
40%	37.77	39.78	41.78	43.23	0.06	0.06	0.06	0.05
50%	36.70	38.86	40.86	42.15	0.08	0.08	0.08	0.07
60%	36.08	38.27	40.27	43.12	0.09	0.09	0.09	0.09
70%	34.57	36.54	39.54	41.02	0.11	0.11	0.11	0.10
80%	34.97	36.12	39.12	41.3	0.12	0.12	0.12	0.10
90%	34.55	36.55	38.55	40.15	0.14	0.14	0.14	0.14

**Figure 8:** Comparison of PSNR performances obtained under different salt and pepper noise levels

Other factors, such as the complexity of the hardware implementation and the power consumption of denoising algorithms, are equally important as the denoising performance. Therefore, we compare the percentages of the total area employed to implement the denoising algorithm and the percentage of total power consumed by that implementation in Fig. 9. These results demonstrate that the proposed PLWF algorithm provides minimum area complexity and power consumption compared to the other methods considered. In addition, the complexity of logic utilization and the computational times required by the different algorithms are listed in Tab. 3. These results further demonstrate the superiority of the hardware implementation of the proposed PLWF algorithm.

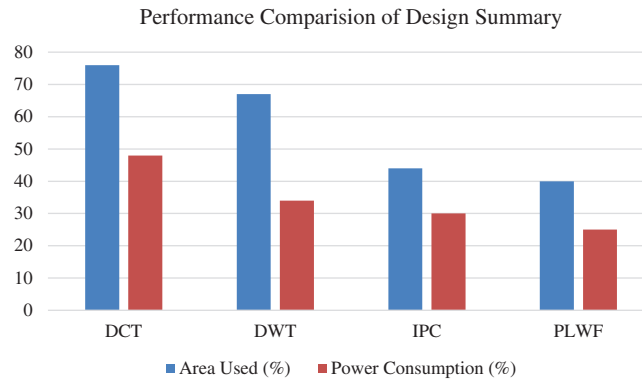


Figure 9: Comparison of area and power consumption

Table 3: Comparison of logic utilization and computational times

Logic utilization	DCT	DWT	IPC	PLWF
Number of I/O	131	131	130	130
Number of bonded IOBs	117 out of 190	116 out of 190	111 out of 190	105 out of 190
Minimum period (ns)	20.650	15.520	10.120	9.012
Minimum input arrival time (ns)	21.750	17.510	11.821	10.25
Maximum output required time (ns)	4.880	4.283	3.982	3.92
Maximum combinational path delay (ns)	15.153	15.113	15.101	14.95

5 Conclusion

The present work addressed the need for developing image denoising algorithms with maximum denoising performance, speed, and efficiency on FPGA platforms by proposing a high-throughput fixed-point AEN filter architecture to denoise digital images in real time using a nonlinear modified PLWF technique. The denoising performance of the proposed denoising scheme was demonstrated to be superior to the denoising performances of IPC and those algorithms based on the DCT and DWT. Moreover, the hardware implementation of the proposed PLWF algorithm required less area and less power consumption than the other implementations considered, and the logic utilization and computational speed were both improved.

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