Energy Engineering

Tech Science Press

DOI: 10.32604/ee.2022.017556

ARTICLE

Research on Phase-Shifted Full-Bridge Circuit Based on Frequency and Phase-Shift Synthesis Modulation Strategy

Mingda Jiang[1], Yanbo Che[1], Hongfeng Li[1,*], Muhammad Ishaq[1] and Chao Xing[1,2]

[1]Key Laboratory of Smart Grid of Education Ministry, Tianjin University, Tianjin, China
[2]Electric Power Research Institute of Yunnan Power Grid Co., Ltd., Kunming, China

*Corresponding Author: Hongfeng Li. Email: lab538@163.com

Received: 20 May 2021 Accepted: 23 July 2021

ABSTRACT

The full-bridge converters usually use transformer leakage inductance and parallel resonant capacitors to achieve smooth current commutation and soft switching functions, which can easily cause problems such as energy leakage and significant duty cycle loss. This paper designs a novel full-bridge zero-current (FB-ZCS) converter with series resonant capacitors and proposes a frequency and phase-shift synthesis modulation (FPSSM) control strategy based on this topology. Compared with the traditional parallel resonant capacitor circuit, the passive components used are significantly reduced, the structure is simple, and there is only a slight energy loss. By controlling the charging time of the capacitor, it can be achieved without additional switches or auxiliary circuits. The automatic control of capacitor energy based on input current addresses the low efficiency of the traditional control strategies. This paper introduces its principle in detail and verifies it through simulation. Finally, an experimental prototype was built further to demonstrate the feasibility of the theory through experiments. The module can be applied to a photovoltaic DC collection system using input parallel output series (IPOS) cascade to provide a new topology for large-scale, long-distance DC transmission.

KEYWORDS

Full-bridge converter; frequency and phase-shift synthesis modulation (FPSSM); photovoltaic DC collection system; control strategy

1 Introduction

With the increasing energy crisis and environmental pollution, photovoltaic power generation has been vigorously promoted. Photovoltaic grid-connected inverter converts the DC power output by photovoltaic modules into AC power that meets the requirements of the grid and then inputs it to the grid. It is the core of grid-connected photovoltaic system energy conversion and control, and it is currently the most widely used full-bridge DC-DC converter. With the increasing requirements for the volume and efficiency of power conversion modules, the switching frequency of phase-shifted full-bridge DC-DC converters is getting higher and higher. However, existing full-bridge converters usually use transformer leakage inductance and parallel resonant capacitors to realize smooth current commutation and soft switching functions [1], as shown in Fig. 1.

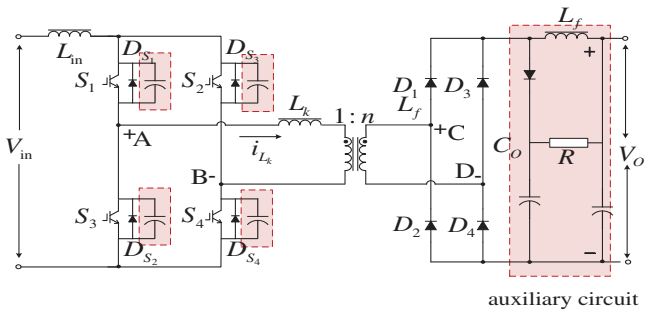


Figure 1: Existing DC boost converter topology

Parallel resonance capacitors have the following disadvantages:

1) The energy stored in the capacitor is fixed. When the load is reduced, it will cause excess energy, which will affect the adjustment range and reduce the operating efficiency of the system;
2) The parallel resonant capacitor needs a dedicated capacitor charging interval during each switching cycle, which will cause the duty cycle loss;
3) With the decrease of the load, the duty cycle loss will increase significantly, and the input current will decrease, and the capacitor charging time will be longer [2];
4) The parallel resonant capacitor will form an energy leakage channel through the transformer winding. The energy stored in the capacitor must exceed the rated value to compensate for the energy loss, but too much energy will further aggravate the energy leakage.

Input parallel output series (IPOS) to increase the output voltage level and power level while reducing the voltage and current stress of the switch tube in the circuit. It is suitable for high-power applications requiring high voltage gain and has gained popularity in recent years. More benefits of IPOS structure include reduced input current and output voltage of each module, module shedding capability, reduced ripple content due to interleaving, intrinsic balancing, and scalable control method. Li et al. [3] proposed a modular isolated soft-switching DC–DC converter that can offer two levels of fault tolerance. The converter consists of an IPOS connected modules to boost voltage levels for High-Power High-Voltage Applications. Likewise, Ye et al. [4] present a novel double-coupled inductor and voltage multiplier boost converter with input parallel output series modules, inheriting the advantages of interleaved series output capacitors with high voltage gain and low output voltage ripple for photovoltaic and fuel cell energy systems, high-intensity discharge lamps (HID), DC backup energy systems, and electric vehicles.

The above shortcomings will affect the maximum power point tracking (MPPT) range and conversion efficiency of the photovoltaic system and significantly impact the adjustment and operating range of the converter. Edwin et al. [5] propose a coupled inductance soft-switching high-gain DC-DC converter. By adding active clamps on the input side to alleviate the switching tube voltage spike problem caused by leakage inductance, it can also realize that the main and auxiliary switches work in soft-switching mode. However, the current ripple on the input side is significant. Similarly, The voltage doubling function of the switched capacitor to obtain a very high voltage transmission ratio is used in [6]. However, the isolated converter still has the disadvantages of considerable input current pulse, insufficient output voltage stabilizing ability, and low

load adjustment rate. Furthermore, Shi et al. [7,8] proposed a DC-DC converter with a source soft-switching auxiliary circuit on the secondary side based on the parallel resonant circuit, which solved voltage stabilization, realized high-frequency soft switching, and improved the working efficiency. However, the control method becomes more complicated due to the increase in the number of switch tubes.

Frequency and phase-shift synthesis modulation technology (FPSSM) is widely used in aviation, wireless communication, and other fields. Azim et al. [9] utilize FPSSM technology for energy-efficient optical wireless systems with direct current (DC) offset hybrid frequency and phase shift keying (DC-FPSK) modulation for Internet-of-Things based on optical wireless systems resulting in higher modulation rates and greater flexibility. An FPSSM signal optical generation technique is proposed in [10], which uses a polarization-preserving fiber Bragg grating with different responses to different input polarization states to convert the baseband information loaded into the signal polarization state to that of the output wavelength, and achieves frequency modulation by interpolation of the beat frequency at the receiver side. It solves the problem that the traditional dual-source beat frequency introduces large phase noise and improves the communication quality of the edge nodes of the cellular communication system. However, in power electronics, this technology has been studied by a few people. Hu et al. [11] apply the phase-shifting frequency conversion technique to a dual active bridge converter to ensure zero-voltage switching over a wide power range with minimal circulating current but does not discuss the use of phase drift compensation in the zero-sequence modulation scheme and the option of combining variable-frequency modulation (VFM) with conventional zero-sequence modulation. A novel variable frequency dual-phase shift synthesis modulation method is designed in [12] and applied in a full-bridge three-level LLC resonant converter. It is demonstrated that the proposed modulation method can achieve soft switching of all switching tubes in the whole load range, but the efficiency and reliability of its operation are not further discussed. This paper applies this technique to a full-bridge zero-current (FB-ZCS) converter, and a prototype is built to discuss its reliability.

This paper designs a full-bridge boost converter with series resonant capacitors, which controls the charging time of the capacitor through frequency and phase-shift synthesis modulation, and automatic control of capacitor energy based on input current can be achieved without the need for additional switches or auxiliary circuits. Compared with the traditional parallel resonant capacitor circuit, the passive components used are significantly reduced, the structure is simple, and have a small energy loss. At the same time, the series capacitor solves the problem of energy leakage in the transformer winding during circulating current, which improves the equipment efficiency.

2 FB-ZCS Converter

2.1 Topology Structure

The proposed full-bridge zero-current switching (FB-ZCS) converter is shown in Fig. 2. The primary side is composed of four reverse blocking switches S_1–S_4 to form a full-bridge circuit. The reverse blocking switch is realized by a package module in which IGBTs and diodes are connected in parallel. It is used to remove the discharge path of the resonant capacitor in a high-frequency circuit. The converter input inductance L_{in} is high, which can be regarded as a constant current source to provide energy for the full-bridge circuit [13–16]. This relieves the problem of transformer flux imbalance to a certain extent, and because the value of L_{in} is high, it is related to the switching frequency. In comparison, the entire LC resonance frequency is very small. A

pair of clamping diodes are attached to the secondary side to feedback the energy generated by the parasitic oscillation of the secondary side to the primary side, which can not only suppress the oscillation and voltage spike but also has a convenient and straightforward structure. A high-frequency transformer with a turns-ratio n isolates the input and output circuits, and its leakage inductance is denoted by L_f. The resonant AC capacitance C_f and the transformer leakage inductance L_f are connected in series to form an LC resonant circuit, which helps the smooth commutation of the current during the switching process and realizes the soft switching function of S_1–S_4.

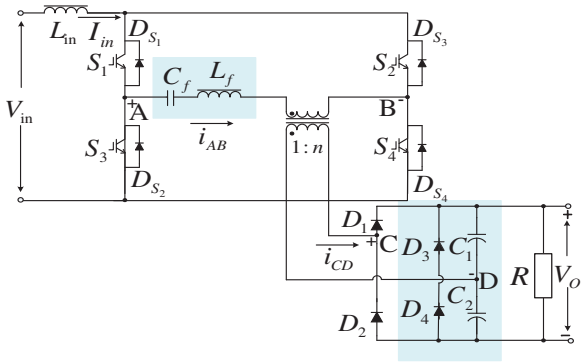


Figure 2: The proposed DC boost converter topology

The secondary circuit is composed of a voltage doubler rectifier, which is composed of a group of diodes D_1 & D_2 and a group of capacitors C_1 & C_2. Compared with the traditional full-bridge rectifier, the voltage doubler rectifier reduces the voltage on the primary side of the transformer from V_0/n to $V_0/2n$, which causes the voltage stress of the transformer winding, switching tube, and input inductor to be reduced by about 50%. The parallel capacitor on the output side mainly plays the role of filtering.

The advantages of this topology are as follows:

1) There is an inductance on the low-voltage input side to minimize voltage stress and insulation requirements. At the same time, the input inductance as a constant current source can alleviate the problem of transformer flux balance and saturation;
2) The leakage inductance of the transformer replaces the additional clamp circuit so that the circuit can smoothly commutate current without voltage spikes.
3) During the entire working cycle, the zero-current switching (ZCS) of the primary side switches and the zero-voltage switching (ZVS) or ZCS of the secondary side diode reduces the switching loss, thereby improving the system efficiency.
4) The passive components used are reduced, the secondary side does not need auxiliary components, the overall structure is simple, and the loss is reduced.

2.2 Working Principle

The working sequence of the converter is shown in Fig. 3. The switching tubes S_1–S_4 are the corresponding states of the four switches. In the working process, each switching cycle T_s is divided into eight working modes, among which the working modes of the first half cycle and the second half cycle are similar. The gate signals of the top switches S_1 and S_2 are complementary

and have a minimal overlap in time to facilitate the realization of current commutation and soft switching functions. The bottom switches S_3 and S_4 also work similarly.

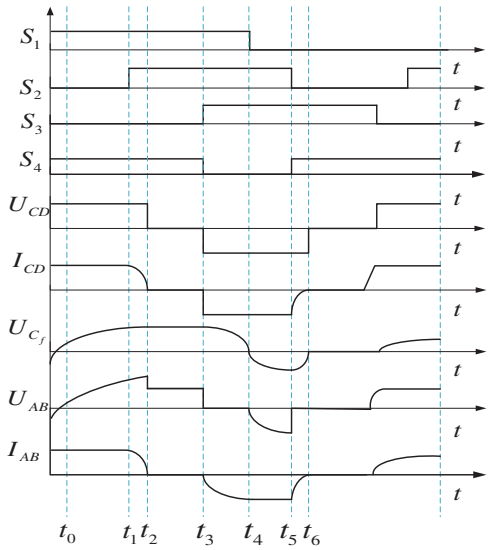


Figure 3: The timing diagram of the converter

To facilitate steady-state analysis, the following assumptions are made:

1) All components in the circuit are ideal;
2) The input inductance L_{in} is large enough to be regarded as a constant current source; the output capacitors C_1 and C_2 are large enough to keep each capacitor at a constant voltage of $V_0/2$;
3) The transformer magnetizing inductance is large.

$$\omega_0 = \frac{1}{\sqrt{L_f C_f}} \tag{1}$$

$$Z_0 = \sqrt{\frac{L_f}{C_f}} \tag{2}$$

Eq. (1) denotes the resonance frequency (ω_0) and (2) represents the characteristic impedance (Z_0); L_f is the leakage inductance of the transformer in henry (H); C_f is the resonant capacitance in Farads (F).

The steady-state operation of the circuit in a complete cycle is divided into twelve modes. The first four modes are described in detail according to the working timing waveforms, as shown in Fig. 3. Fig. 4 lists the first six modes of operation, and the following six modes can be discussed similarly for periodic symmetry.

(1) Mode-I ($T_1 = t_1 - t_0$)

When the current I_{in} is completely transferred from S_2 to S_1, the Mode I start at t_0. S_1 and S_4 are turned on in this mode, and the current I_{in} flows through S_1, capacitor C_f, transformer leakage inductance L_f and transformer primary side, and form a loop through S_4

while transmitting energy to the output side and charging capacitor C_f. The secondary side diode D_1 is turned on, forming a loop through C_1 and the secondary side of the transformer, and charging C_1 at the same time, the C_1 and C_2 supply power to the load. At this time, C_f does not need a separate charging interval, and compared with existing converters, it significantly reduces the duty cycle loss. When S_3 is turned on, this mode ends at t_1. In this mode, the primary current, capacitor voltage, and primary voltage can be expressed via (3)–(5), respectively.

$$i_p(t) = I_{in} \tag{3}$$

$$U_{C_f}(t) = \frac{\int_{t_0}^{t} i_{AB} dt}{C_f} \tag{4}$$

$$U_{AB}(t) = V_{in} - L\frac{dI_{in}}{dt} \tag{5}$$

where $t \leq t_1$, I_{in} is the current flowing through the input inductor L_{in}, i_{AB} is the primary side current flowing through C_f and L_f, U_{C_f} is the voltage across C_f, U_{AB} is the primary side voltage of C_f and L_f, and V_0 is the output voltage.

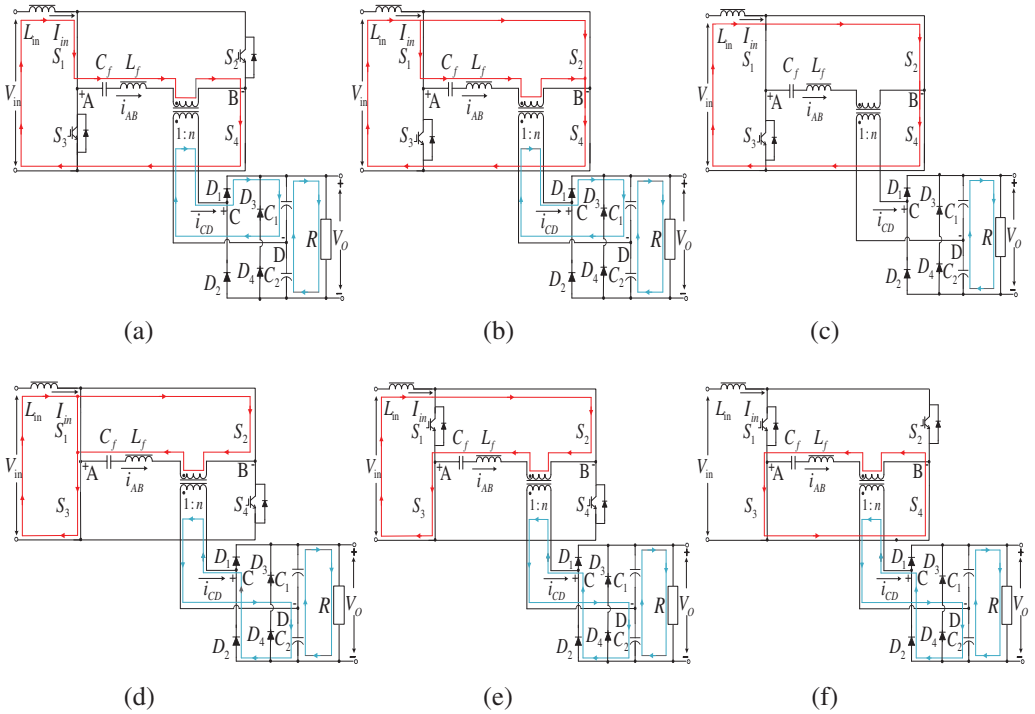


Figure 4: The first six working modes (a) working mode I (b) working mode II (c) working mode III (d) working mode IV (e) working mode V (f) working mode VI

(2) Mode II ($T_2 = t_2 - t_1$)

After S_2 is turned on, i_p will gradually decrease, and the current I_{in} will gradually change from S_4 to S_2. At this time, the primary voltage U_{AB} is clamped to 0, and i_{AB} also decreases

and gradually drops to 0 at t_2, thus achieving ZCS shutdown. At the end of Mode I, the peak voltage C_f of the resonant capacitor C_f reaches the maximum value, and the primary-current i_p continues to decrease to zero during Mode II ($T2 \ll T1$). The secondary transformer forms a loop through D_1 and C_1, and the capacitors C_2 and C_1 are discharged to supply power to the load. T_2, primary current, and capacitor voltage can be expressed using (6) and (7):

$$i_{AB}(t) = I_{in} - \left(U_{C_f-peak} + \frac{V_0}{2n} \right) \frac{t}{L_f} \tag{6}$$

$$U_{C_f}(t) = \frac{\int_{t_1}^{t} i_{AB} dt}{C_f} \tag{7}$$

where $U_{C_f-peak} = \frac{\int_{t_1}^{t_2} i_{AB} dt}{C_f}$ is the maximum voltage value of the capacitor C_f, $t \le t_2$, V_0 is the output voltage, V; n is the turn ratio of the transformer.

(3) Mode III ($T_3 = t_3 - t_2$)

At this time, the current of S_1 completely turns to S_2 and forms a loop with L_{in}. The input voltage V_{in} charges the inductance L_{in}. At this time, the primary current i_{AB} is 0, there is no energy transfer between the primary and secondary sides of the transformer [17,18], and the load capacitor-discharge provides the load energy. In this mode, the capacitor voltage and primary side voltage can be expressed by (8) and (9):

$$U_{C_f}(t) = U_{C_f-peak} \tag{8}$$

$$U_{AB}(t) = U_{C_f}(t) - \frac{V_0}{2n} \tag{9}$$

(4) Mode IV ($T_4 = t_4 - t_3$)

In this mode, S_3 is on, and S_4 is off. The part of loop current is formed by Mode III, and it will flow through S_2 and form a resonant charging circuit with C_f, L_f, and S_3 to transfer energy to the transformer. The other part of I_{in} forms a charging circuit with S_3. At this time, the current charges the inductor and capacitor in reverse, and the primary side current i_{AB} increases from zero in reverse, but its value cannot meet the current value required by the secondary-side load. At this time, the secondary side transformer forms a loop through C_2 and D_2 while the discharge of capacitors C_1 and C_2 powers the load. Due to the effect of inductance, the current flowing through S_2 cannot increase all at once but gradually increases. The current flowing through S_1 reaches zero at the beginning of the next moment to realize the ZCS turn-on. In this mode, the primary voltage and current and the energy storage capacitor voltage can be expressed via (10)–(12), respectively:

$$U_{AB} = 0 \tag{10}$$

$$i_{AB}(t) = -\frac{U_{C_f-peak} - \frac{V_0}{2n}}{Z_0} \sin(\omega_0 t) \tag{11}$$

$$U_{C_f}(t) = U_{C_f-peak} \cos(\omega_0 t) \tag{12}$$

(5) Mode V ($T_5 = t_5 - t_4$)

In this mode, S_1 is closed, the current I_{in} passes through S_2 and forms a resonant circuit with C_f, L_f, and S_3 to transfer the energy to the transformer. The primary side current i_{AB} reaches the maximum negative direction at t_5, the secondary side transformer continues to form a loop through C_2 and D_2, and the capacitors C_1 and C_2 discharge to supply power to the load.

(6) Mode VI ($T_6 = t_6 - t_5$)

In this mode, S_2 is also closed; the current I_{in} can no longer form a resonant circuit with S_2, C_f, L_f, and S_3. At this time, the resonant capacitor and inductor discharge maintain that the current of the primary circuit does not immediately decrease to 0, and the primary voltage and circuit gradually decrease. The secondary side transformer still forms a loop through C_2 and D_2, and capacitors C_1 and C_2 discharge to supply power to the load.

3 Application in the Control of Photovoltaic Power Generation

As shown in Fig. 5, in practical applications, the FB-ZCS topology adopts the form of sub-module input parallel output series (IPOS) to increase the output voltage level and power level [19–21] and reduce the voltage and current stress of the switch tube in the circuit.

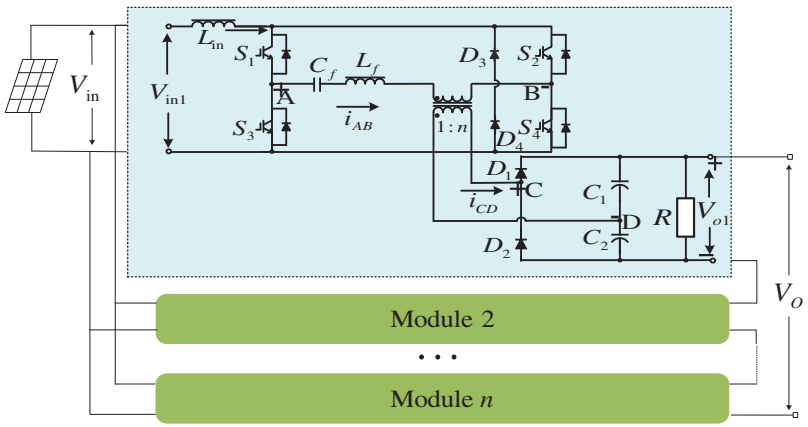


Figure 5: IPOS cascaded DC–DC converter topology

3.1 Frequency and Phase-Shift Synthesis Modulation (FPSSM) Control Strategy

In this paper, the control strategy is shown in Fig. 6, and the conductance increment method is used to achieve maximum power tracking (MPPT). The PI controller modulates the difference between the reference voltage V_{ref} generated by the MPPT algorithm and the actual photovoltaic side output voltage Vpv to generate the value of the photovoltaic side output reference current I_{in}^*. The error signal is obtained after comparing the actual input current value I_{in} and the reference current I_{in}^*, which is processed by the PI module. The signal generated by phase shift modulation adjustment and the signal generated after frequency adjustment is processed in the gate signal generator to obtain the corresponding switch tube trigger signal [22].

During the normal operation of the circuit, the load reduction will cause the input current I_{in} to decrease so that the energy stored in the capacitor C_f is also reduced. Nevertheless, when the load is gradually reduced to a certain level, the input current I_{in} is not enough to charge the capacitor to the level required for its voltage level to meet the resonance condition. In this case,

the frequency f_s gradually decreases from a fixed value, thereby increasing the capacitor charging time and compensating for the decreased input current I_{in}.

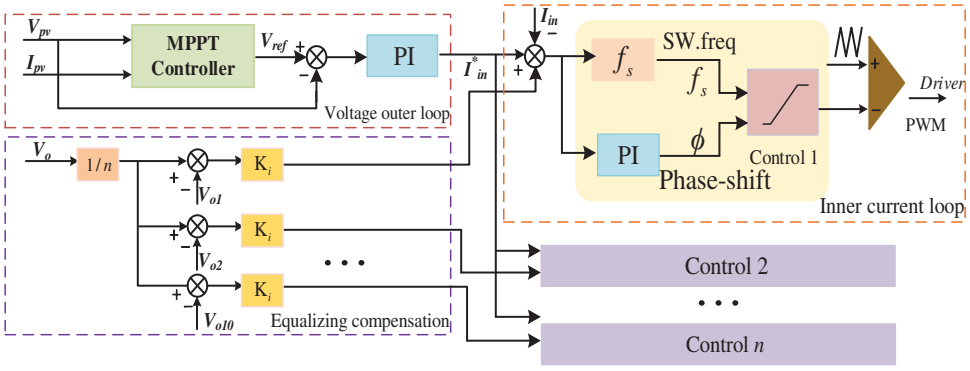


Figure 6: FB-ZCS input current control

Analyzing the working mode, the research concluded that energy is transferred from the input side to the output side during Mode I while charging the capacitor C_f. During Mode III, there is no energy transmission on the primary and secondary sides of the transformer, and the output capacitor powers the load. These modes are similar to the discharging and charging modes in a simple Boost converter, so the ideal voltage gain is expressed by (13):

$$\frac{V_0}{V_{in}}|_{ideal} = \frac{2n}{1-D} \tag{13}$$

Since the duty cycle D is relatively consistent with the conventional duty cycle, the f_s have little effect on the model's input and output voltage gains. Therefore, phase shift and frequency modulation can be independently applied to current regulation and capacitor C_f energy control. This method is called Frequency and phase-shift synthesis modulation. In recent years, it has been successfully used to improve the converter's performance. This research article is trying to apply this technology to the FB-ZCS converter. The flowchart is shown in Fig. 7.

If I_{in} is larger than the setting value I_{set}, it means that the energy of the capacitor C_f can meet the resonance condition. At this time, there is no need to adjust the frequency; just charge the capacitor through the PI controller. When I_{in} is smaller than the set value I_{set}, it is not enough to charge the capacitor C_f to the level required to make its voltage level meet the resonance conditions. At this time, the frequency is adjusted, and f_s is gradually reduced from fixed value, thereby increasing the time for capacitor charging and compensating for the decreased input Current I_{in}.

3.2 Soft Switching Analysis

From the analysis in Section 2.2, to achieve smooth current commutation and soft switching, the energy stored in the C_f must be greater than the energy stored in the resonant inductance as expressed by (14):

$$C_f\left(U_{C_f-peak} + \frac{V_0}{2n}\right)^2 > L_f I_{in}^2 \tag{14}$$

The energy stored in C_f is determined by I_{in}. When I_{in} is reduced to a specific value, the charging energy of C_f cannot reach the required voltage level. At this time, frequency regulation is used to reduce f_s to increase the charging duration to compensate for the reduced current. The relationships among $U_{C_f}-peak$, I_{in}, and f_s were defined by (15):

$$U_{C_f-peak} = U_{C_{f0}} + \frac{I_{in}}{C_f}\frac{(1-D)}{f_s} > \frac{V_0}{2n} + I_{in}Z_0 \tag{15}$$

where $U_{C_{f0}}$ is the initial capacitor voltage of Mode I. The voltage peak $U_{C_f}-peak$ is obtained by controlling the charging time T_2.

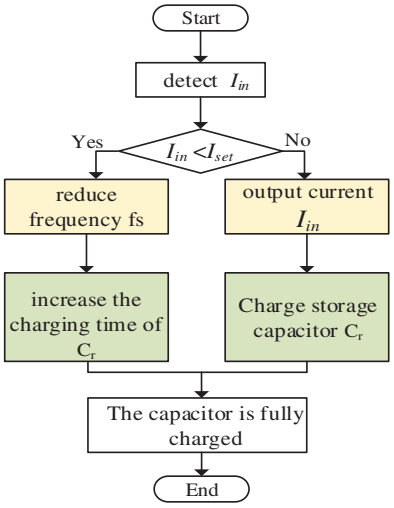


Figure 7: Mode switching flowchart

Table 1 shows the comparison of the proposed topology with other literature topologies [23–25], where converters require longer charging time to full load rating, which is an unnecessarily light load. These structures have the following advantages: the existence of a low-voltage input side inductor minimizes the voltage stress and insulation requirements; the input inductor can also be used as a constant current source to alleviate the flow balance and saturation problems of the transformer.

Table 1: Comparison of several converter structures

Type	Converter [23]	Converter [24]	Converter [25]	Proposed
Primary switch count	4	8	6	4
Secondary diode count	13	4	4	4
Output capacitor rating	Vo/2	Vo/2	Vo	Vo/2
Resonant capacitor leakage	Yes	Yes	Yes	No
Duty-cycle loss	52%	58%	43%	9.5%

As a result, the duty cycle loss of existing converters is more than 50% of the switching time period, which severely limits the operating range of the converter. In contrast, the topology in this paper uses series capacitors and FPSSM control to reduce unnecessary charging intervals and duty cycle losses to 10%. Through comparison, it can be concluded that the proposed structure is more compact and has better performance.

4 Simulation and Experiment

The proposed control strategies were verified separately, and 10 IPOS cascaded FB-ZCS DC boost converter models were built in MATLAB, and their parameter settings are shown in Table 2.

Table 2: FB-ZCS DC–DC simulation parameters

Type of parameter		Value
Photovoltaic cells	Short circuit voltage	1.05 KV
	Short circuit current	0.5 KA
	MPP voltage (25°C, 1 kW/m^2)	0.82 KV
	Maximum power	0.5 MW
	Rated power	0.5 MW
DC-DC boost converter	Rated voltage of primary side	0.85 KV
	Rated voltage of secondary side	6 KV × 10
	Transformer ratio	3.3

Next, the verification process of the topology and control strategy is proposed.

4.1 Stability Analysis of Output Voltage and Current

Due to a pair of clamping diodes that are attached to the secondary side, the energy generated by the parasitic oscillation of the secondary side is fed back to the primary side, and the oscillation and voltage spikes are suppressed so that high-frequency oscillation and voltage overshoot of the secondary stage of the transformer is effectively suppressed. Fig. 8 shows the voltage waveforms of the primary side of the transformer of the traditional DC boost converter and the proposed DC boost converter, respectively. Through comparison, it can be observed that the high-frequency oscillation of the transformer secondary side is restrained, and voltage overshoot is prevented in the process of switching on and off.

The input and output voltage and current of a single FB-ZCS sub-module are shown in Fig. 9. The analysis shows that the voltage and current enter a stable operating state after a short period of fluctuation. After stabilization, the output voltage ripple coefficient is 0.091%, and the output current value is 0.13%. Compared with the full-bridge boost converter in [26], voltage and current stability have significantly improved.

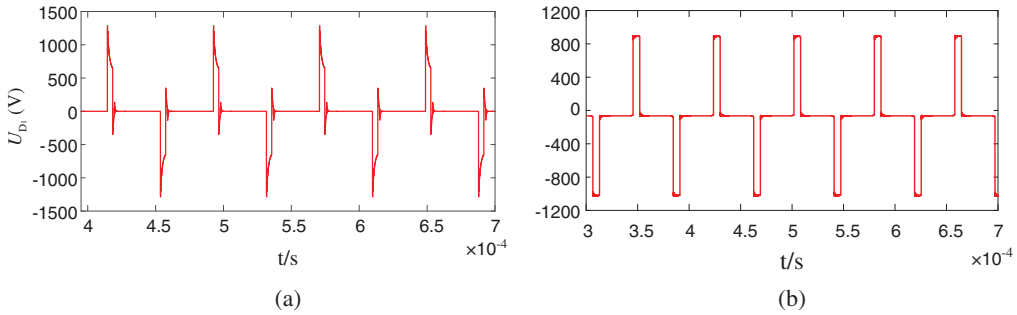


Figure 8: Voltage waveform of the secondary side. (a) Traditional DC boost converter; (b) The proposed DC boost converter

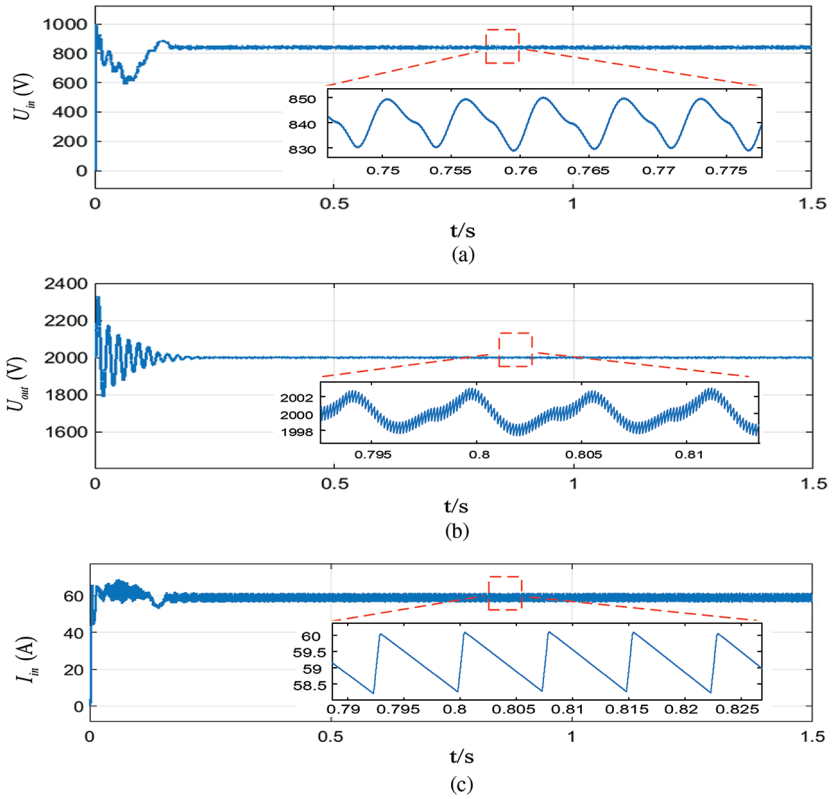


Figure 9: (Continued)

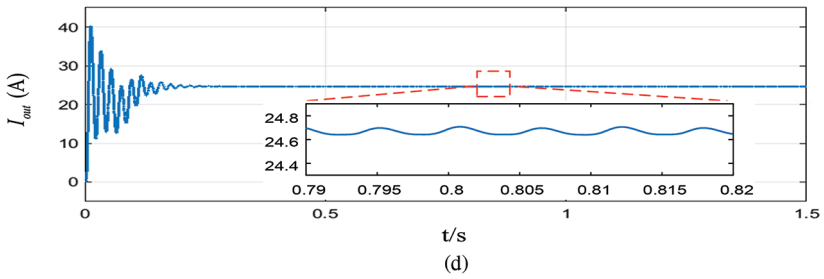


Figure 9: Single FB-ZCS input and output voltage and current waveform diagram and partially enlarged view. (a) Input voltage waveform and partial enlarged view; (b) Output voltage waveform and partial enlarged view; (c) Input current waveform and partial enlarged view; (d) Output current waveform and partial enlarged view

4.2 Frequency and Phase-Shift Synthesis Control

Fig. 10 shows the input and output waveforms of I_{in}, i_{AB}, U_{AB}, and U_{C_f} and their partial amplification. The photocurrent tends to stabilize at 0.026 s, and the entire LC resonance frequency of the series capacitor is minimal in one cycle. The C_f and L_f are connected in series to form an LC resonant circuit. During the whole process, the charging and discharging of the C_f changes according to current commutation and frequency changes.

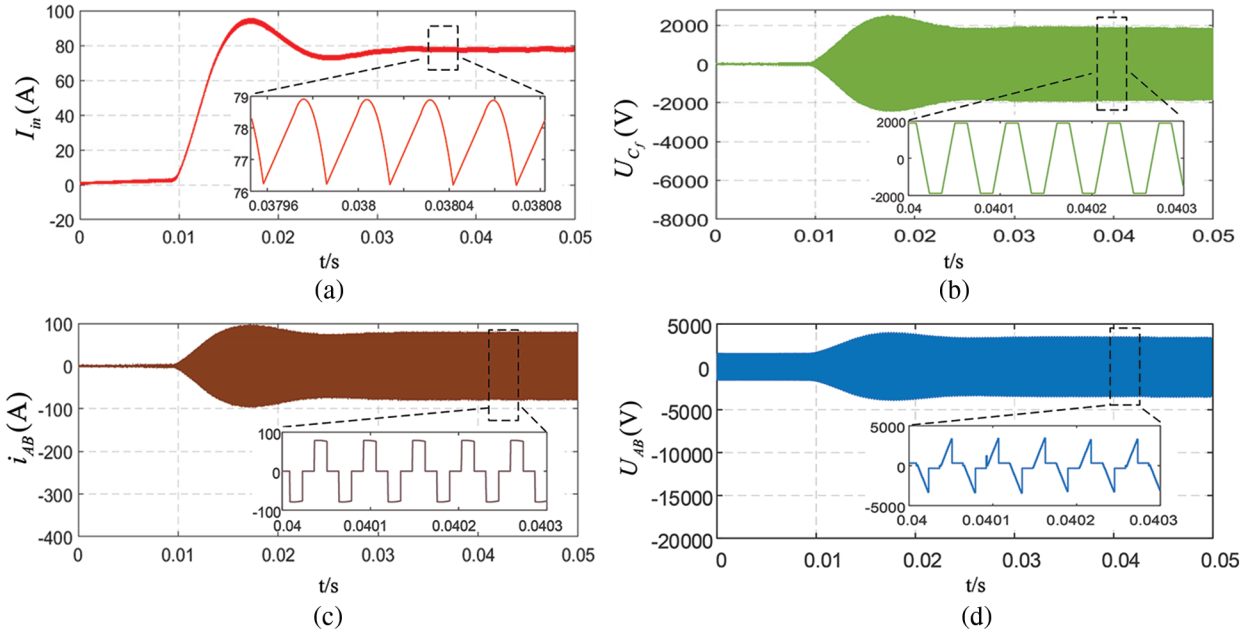


Figure 10: Input and output waveform and partially enlarged diagram. (a) I_{in} waveform and partial enlarged view; (b) U_{cf} waveform and partial enlarged view; (c) i_{AB} waveform and partial enlarged view; (d) U_{AB} waveform and partial enlarged view

According to the radiation characteristics of photovoltaic cells, as the light irradiance decreases, the voltage and current output by photovoltaic modules gradually decrease. Set the initial light irradiance of the photovoltaic module to 1000 W/m^2 in the simulation model, perform

simulation and give the corresponding primary-side current, voltage value, and the waveform of the energy storage capacitor voltage as shown in Fig. 11, and its partial enlargement is shown in Fig. 12. According to the calculation of resonance conditions, when the light irradiance is less than 600 W/m^2, the photovoltaic module output current I_{in} is not enough to charge C_f to the required voltage value. Therefore, in order to ensure the regular operation of the system, the frequency f_s is stepwise-decreased below the base value to increase the charging time of the capacitor C_f to reach the required level.

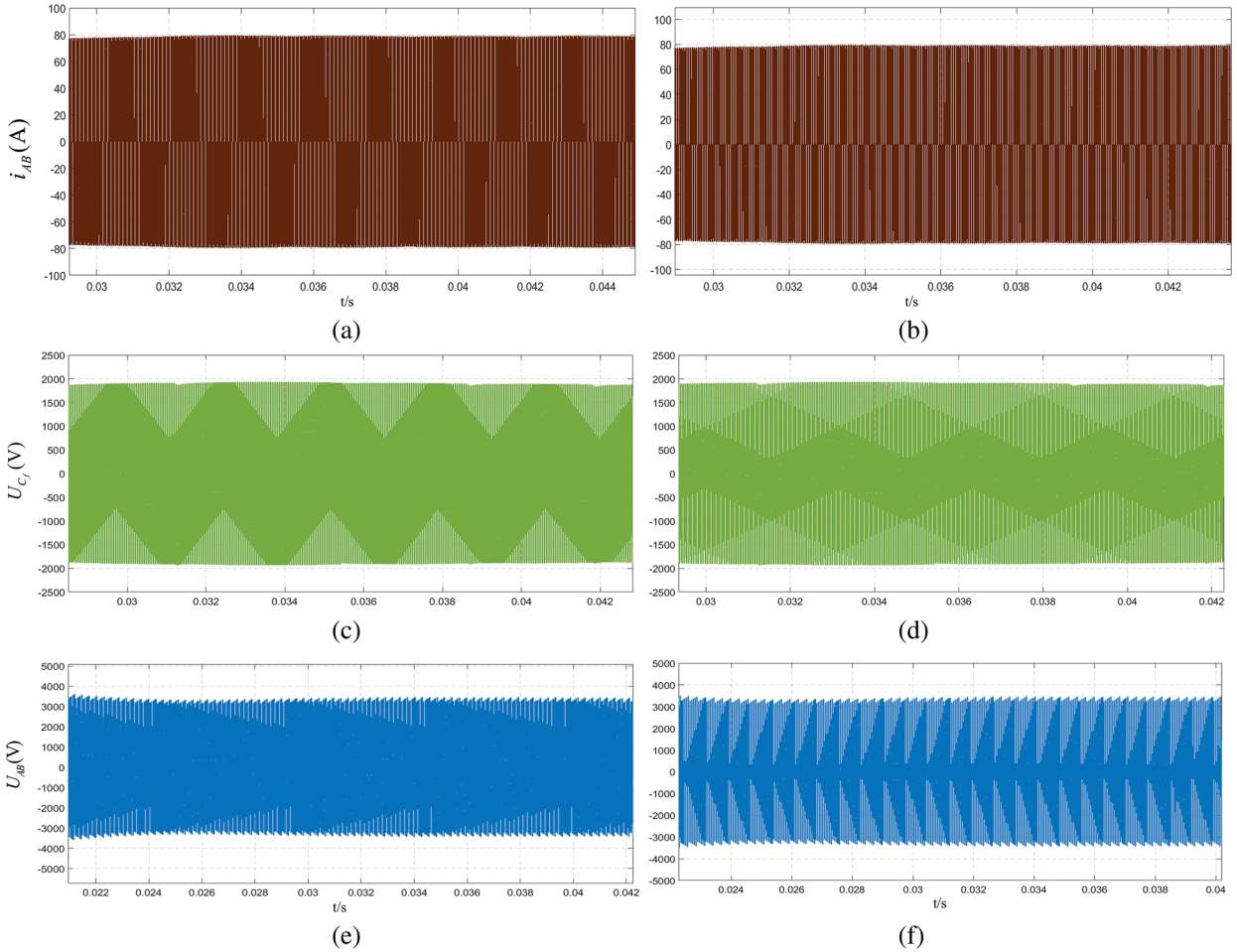
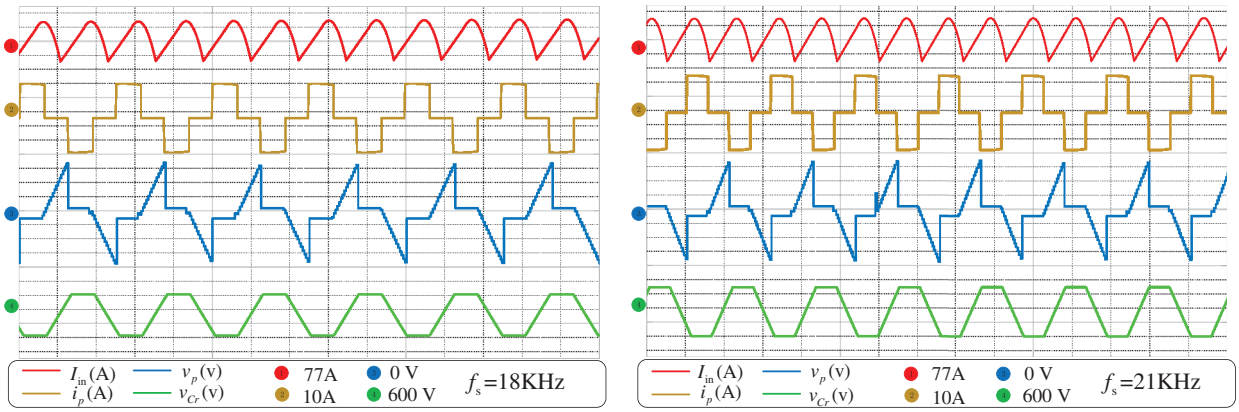


Figure 11: Waveform diagram of the primary voltage and capacitor voltage. (a) Light irradiance 550 W/m^2 f_s = 18 KHZ; (b) Light irradiance 1000 W/m^2 f_s = 21 KHZ; (c) Light irradiance 550 W/m^2 f_s = 18 KHZ; (d) Light irradiance 1000 W/m^2 f_s = 21 KHZ; (e) Light irradiance 550 W/m^2 f_s = 18 KHZ; (f) Light irradiance 1000 W/m^2 f_s = 21 KHZ



(a) (b)

Figure 12: Partially enlarged simulation waveform. (a) Light irradiance 550 W/m^2; (b) Light irradiance 1000 W/m^2

When the light irradiance is within 600 and 1000 W/m^2, the FB-ZCS model can use the input current adjustment method to adjust energy adaptively. At this time, there is no need to turn on the frequency adjustment mode, as shown in the right column of Fig. 11. A partially enlarged view is shown in Fig. 12b. When the light irradiance is less than 600 W/m^2, the photocurrent reduction of the system is not enough to support the resonant condition of the resonant capacitor, and it switches to the frequency adjustment mode, as shown in the left column of Fig. 11, and its partially enlarged view is shown in Fig. 12a.

The light irradiance of the photovoltaic module is reduced to 550 W/m^2 for the mode switching effect test. It can be seen from the figure that the switching frequency has been automatically switched to 18 KHz. The primary current, voltage, and energy storage capacitor voltage waveforms are shown in the left column of Fig. 11. The corresponding partial enlargement is shown in Fig. 12a. It can be seen that when the light irradiance drops below the reference value, the input current is detected to be less than the set minimum input current value. The mode switching command is sent to make the FB-ZCS circuit automatically switch from the current control mode to the frequency control mode, the frequency drops. The charging time of the energy storage capacitor increases to compensate for the insufficient energy of the energy storage capacitor caused by the drop in the input current [20]. A special charging interval is not required, so it can safely be concluded that the effect of frequency and phase-shift synthesis control is good.

4.3 Soft Switching

Taking the ZCS turn-on process of S_1 in Mode IV as an example for analysis. Fig. 13 shows the simulation waveform of the switching S_1. The blue dashed line and red solid waveforms represent the gate signal and current waveform of the switching S_1, respectively. It can be seen from the figure that in the turn-off process, the current flowing through S_1 is gradually transmitted to S_2 and then gradually drops to zero. Due to resonant capacitance and inductance, the current rises slowly, thus realizing soft ZCS.

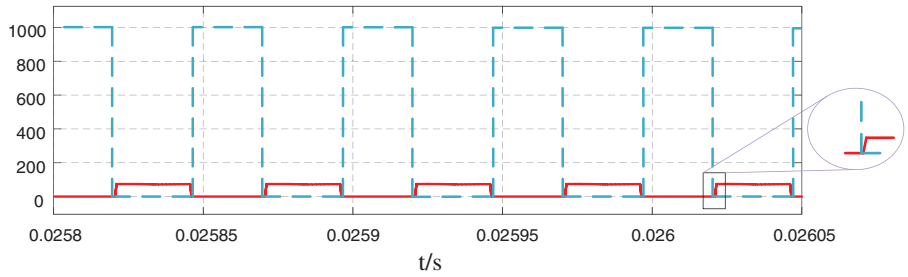


Figure 13: The soft switching function of switching S_1

4.4 Experiment and Results

We have conducted experiments for further verification. In this paper, a hardware prototype is built, integrating the control circuit and the phase-shifted full-bridge module and the drive signal, as shown in Fig. 14. The relevant parameters are listed in Table 3, and the input magnitude is changed by adjusting the amplitude with a DC input instead of a PV power input.

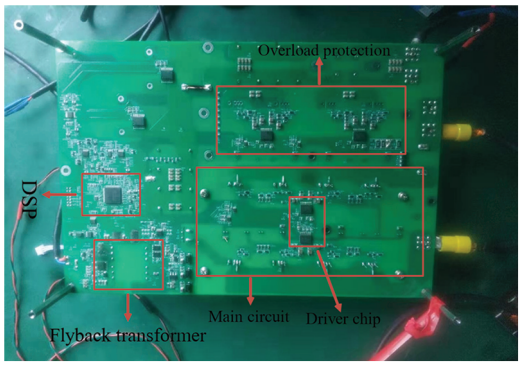


Figure 14: Experimental hardware platform

Table 3: Types and parameters of experimental devices

Type	Device selection and parameters
Primary switch	IRGP4055DPbF
Secondary diode	STTH15L06D
Power rating	3 kW
Resonant capacitor	140 nF
Output capacitor	120 uF
Input inductor	2 mH
Switching frequency	23 kHz
Turns-ratio	1:3

(Continued)

Table 3: Continued

Type	Device selection and parameters
Gate driver	Si8233BB-DS
Controller	DSPIC33CK64MC105T-I/PT

Fig. 15 shows the waveforms of i_{AB}, U_{Cf}, U_{AB} and U_{out} at 23 KHz, from top to bottom, the yellow, green, red and blue lines represent i_{AB}, U_{Cf}, U_{AB} and U_{out}, respectively. Fig. 16 shows the amplified waveforms of i_{AB}, U_{Cf}, U_{AB} and U_{out} at 23 and 17 KHz. As illustrated in the figures, the voltage across AB varies when the frequency changes, but soon stabilizes.

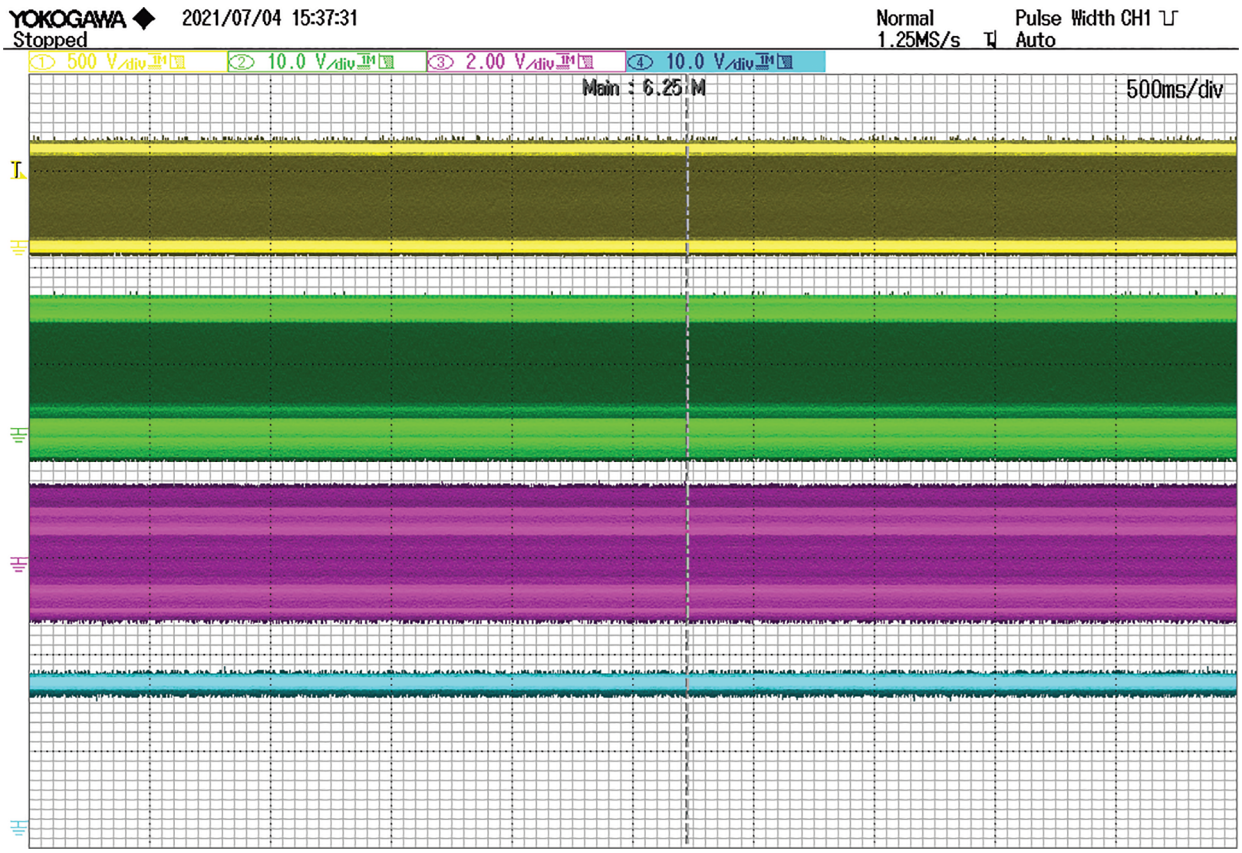


Figure 15: Experimental waveforms of i_{AB}, U_{Cf}, U_{AB} and U_{out} with $f_s = 23$ KHz

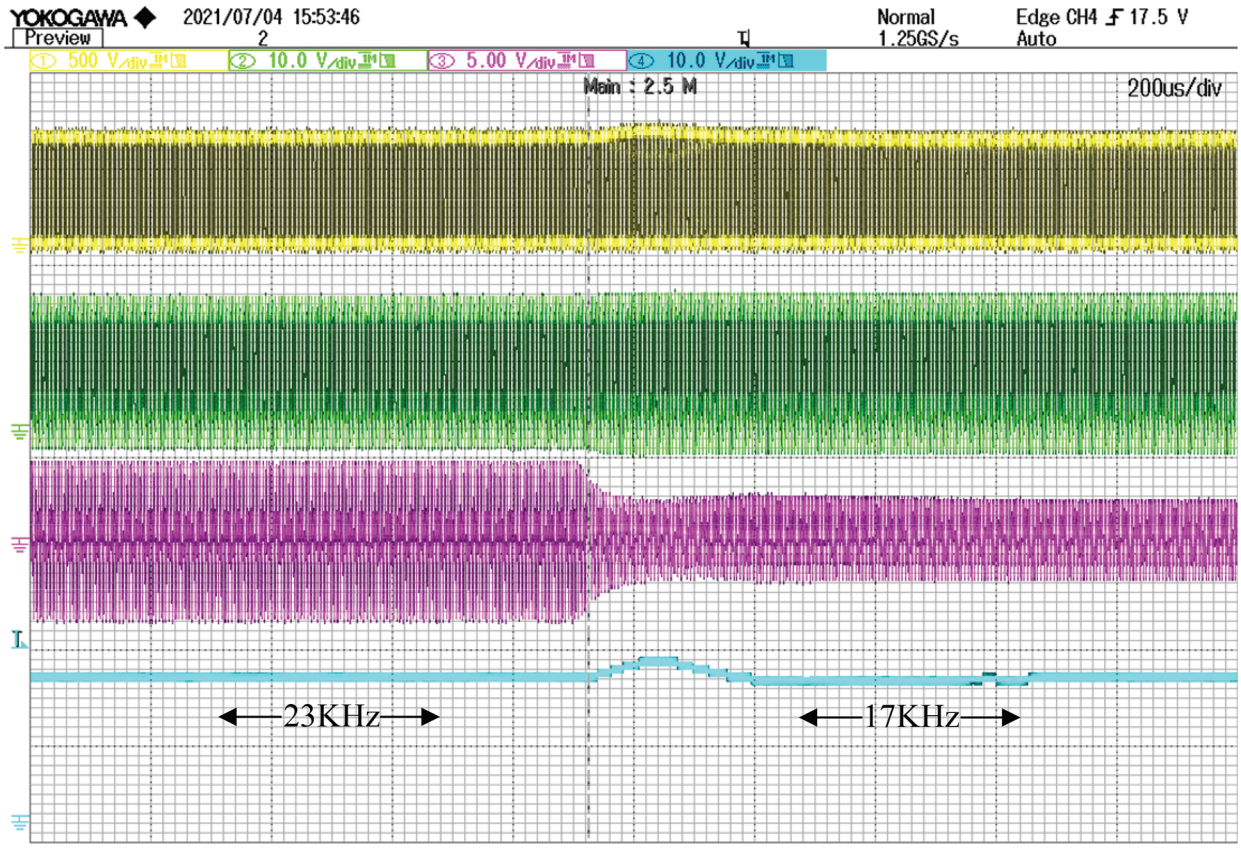


Figure 16: Experimental amplified waveforms of i_{AB}, U_{Cf}, U_{AB} and U_{out} with $f_s = 23$ KHz, $f_s = 17$ KHz

The waveforms of i_{AB}, U_{Cf}, U_{AB} and their amplification after increasing the output voltage are given in Fig. 17. By connecting C_r in series, the energy is transferred to the output while charging it in Mode I, thus significantly reducing the duty cycle loss, and variation of solar light can be changed by adjusting the input voltage magnitude. The light intensity is increased to 1000 W/m^2 corresponding to an input current of 5A, and the peak value of v_{Cr} increases as the irradiation increases, at which point the capacitor is filled with energy to meet the load requirements.

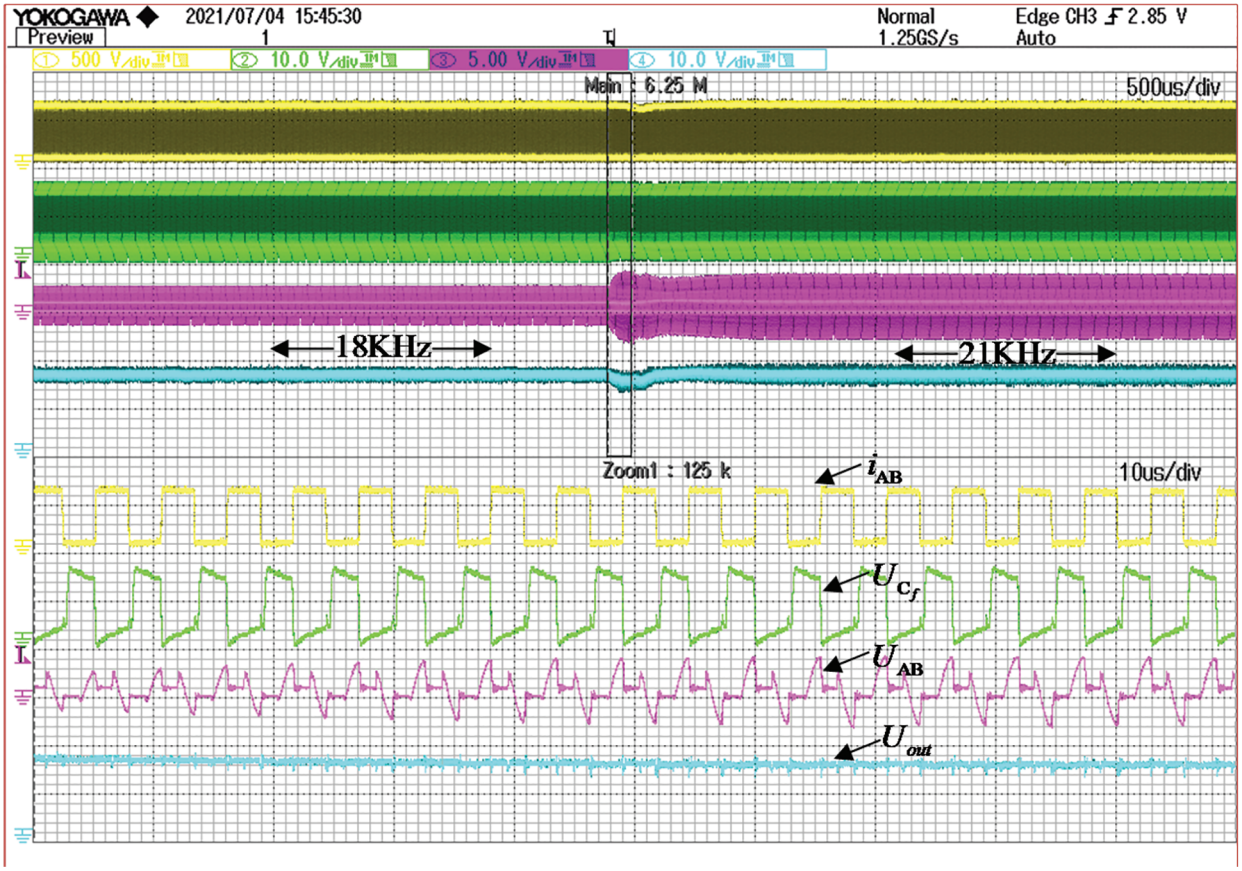


Figure 17: Experimental waveforms of $f_s = 18\,\text{KHz}$, $f_s = 21\,\text{KHz}$, i_{AB}, U_{Cf}, U_{AB}, U_{out} and amplified waveforms

Fig. 18 shows the waveforms of i_{AB}, U_{Cf} and U_{AB} corresponding to the light irradiance downward adjustment and their enlarged waveforms. The light intensity is reduced from 1200 to $520\,\text{W/m}^2$, and the corresponding input current is reduced from reaching 6.5 to 3.8A. The light irradiance is less than the reference value, the photocurrent of the system is reduced and is not enough to support the resonance condition of the resonant capacitor, and it is switched to frequency regulation mode and the v_{Cr} value decreases, thus adaptively reducing the resonance energy without storing the full-load rated energy.

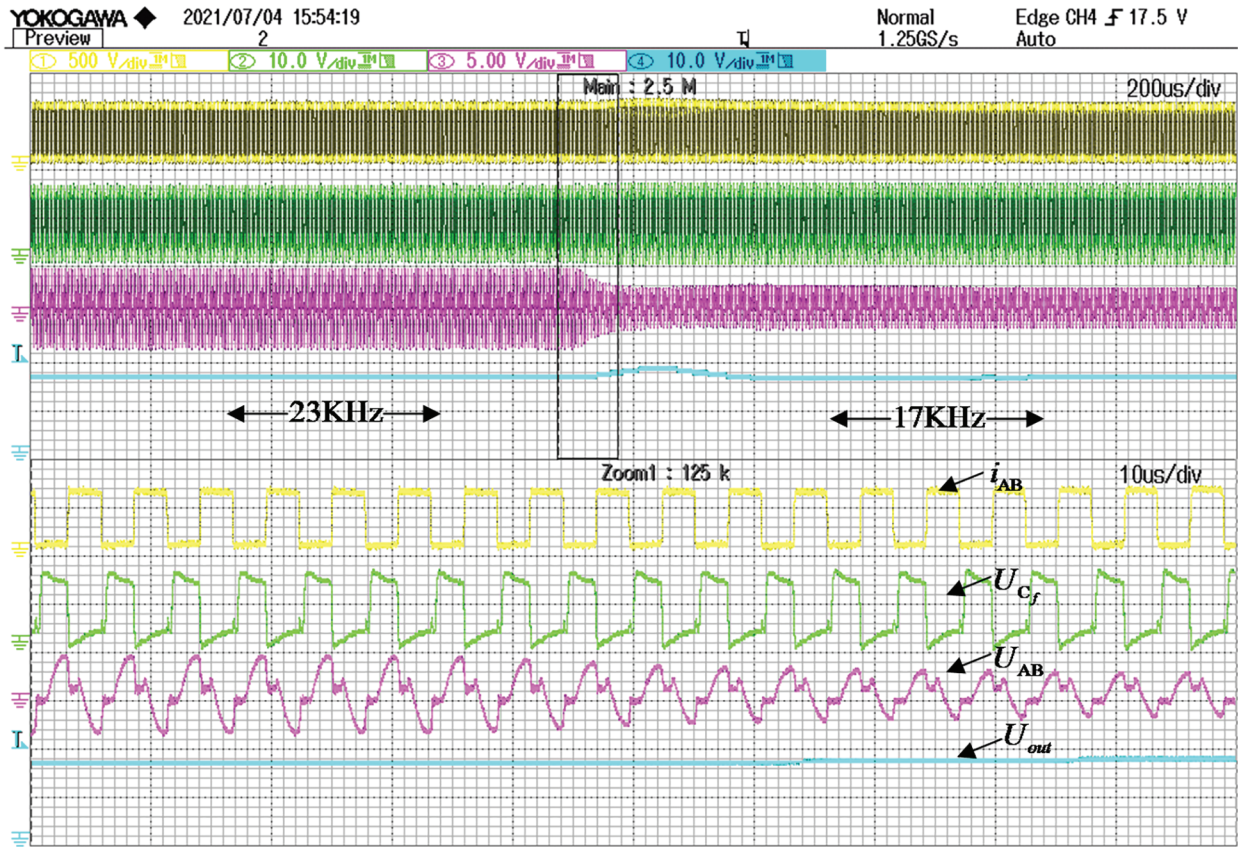


Figure 18: Experimental waveforms of $f_s = 23\,\text{KHz}$, $f_s = 17\,\text{KHz}$, i_{AB}, U_{Cf}, U_{AB}, U_{out} and amplified waveforms

Fig. 19 shows the voltage and current through switch S_1 during S_1 startup. The yellow line represents the voltage, and the green line represents the current. It can be seen from the figure that during startup, when the voltage drops, the current rises very slowly, as it is facilitated by the resonant commutation between L_f and C_f as described in operating Mode IV, which leads to zero-current conduction of switch S_1, verifying what is illustrated by the theory.

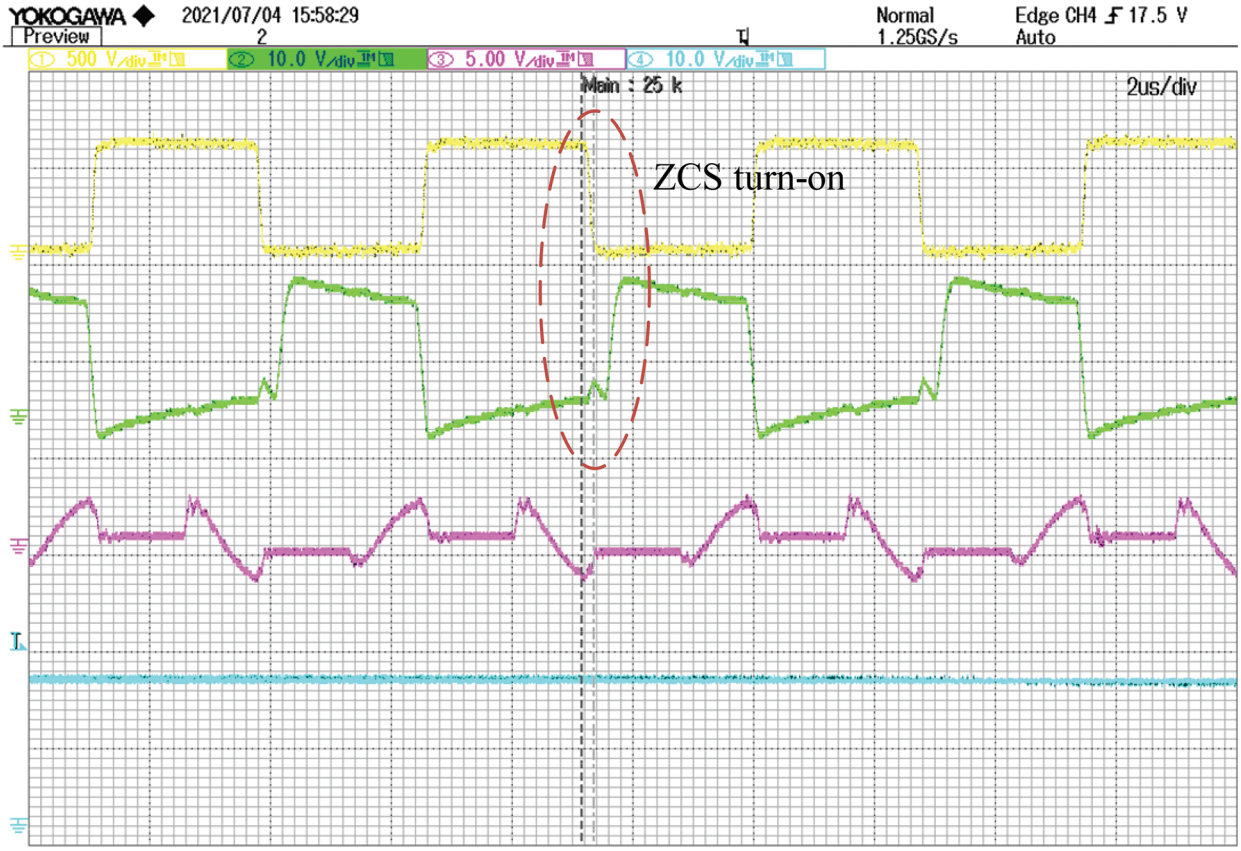


Figure 19: Experimental waveform of voltage and current of S_1

5 Conclusion

A novel full-bridge zero-current converter (FB-ZCS) is designed, and a frequency and phase-shift synthesis modulation (FPSSM) control strategy is proposed. Automatic control of capacitor energy based on input current can be achieved without additional switches or auxiliary circuits by controlling the charging time of the capacitor. The control approach solves the problems of low efficiency and high duty cycle loss in the current commutation and soft-switching functions of existing full-bridge converters, which usually use transformer leakage inductance and parallel resonant capacitance. Finally, the theoretical analysis is first verified by simulation, and then an experimental hardware platform is built and further verified by experimentation. The conclusion shows that the novel converter designed by the FPSSM modulation technique has an excellent boosting effect and high reliability. The study shows that the method is simple in structure and has a good control effect. The module can be cascaded with IPOS and used in photo-voltaic DC collection systems, providing a new topology scheme for large-scale, long-distance DC transmission.

Acknowledgement: The authors thank the support of the Tianjin University and Electric Power Research Institute of Yunnan Power Grid Co., Ltd.

Funding Statement: This work was supported by the Key R&D Program of Tianjin (No. 20YFYSGX00060).

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

References

1. Ajami, A., Ardi, H., Farakhor, A. (2015). A novel high step-up DC-DC converter based on integrating coupled inductor and switched-capacitor techniques for renewable energy applications. *IEEE Transactions on Power Electronics, 30,* 4255–4263. DOI 10.1109/TPEL.2014.2360495.
2. Tran, D., Vu, H., Choi Woojin (2016). A novel quasi-resonant ZVZCS phase shift full bridge converter with an active clamp in the secondary. *IEEE 8th International Power Electronics and Motion Control Conference*, pp. 492–495. Hefei, China.
3. Li, Z., Wu, T., Zhang, G., Yang, R. (2018). Hybrid modulation method combining variable frequency and double phase-shift for a 10 kW LLC resonant converter. *IET Power Electronics, 11,* 2161–2169. DOI 10.1049/iet-pel.2018.5304.
4. Ye, J., Yan, L., Pan, W., Luo, B., Zou, X. (2018). Generation of hybrid frequency and phase shift keying signal for radio over fiber system. *Guangxue Xuebao/Acta Optica Sinica, 38*, 80–84. DOI 10.3788/AOS201838.0206002.
5. Edwin, F., Xiao, W., Khadkikar, V. (2014). Dynamic modeling and control of interleaved flyback module-integrated converter for PV power applications. *IEEE Transactions on Industrial Electronics, 61,* 1377–1388. DOI 10.1109/TIE.41.
6. Sathyan, S., Suryawanshi, H. M., Ballal, M. S., Shitole, A. B. (2015). Soft-switching DC–DC converter for distributed energy sources with high step-up voltage capability. *IEEE Transactions on Industrial Electronics, 62,* 7039–7050. DOI 10.1109/TIE.2015.2448515.
7. Shi, K., Zhang, D., Zhou, Z., Zhang, M., Zhang, D. et al. (2016). A novel phase-shift dual full-bridge converter with full soft-switching range and wide conversion range. *IEEE Transactions on Power Electronics, 31,* 7747–7760. DOI 10.1109/TPEL.2015.2512848.
8. Zhao, L., Xu C, L., Zheng, X. (2018). A dual half-bridge phase-shifted converter with wide ZVZCS switching range. *IEEE Transactions on Power Electronics, 33,* 2976–2985. DOI 10.1109/TPEL.63.
9. Azim, A. W., Le, Y., Ros, L. (2020). Hybrid frequency and phase-shift keying modulation for energy efficient optical wireless systems. *IEEE Wireless Communications Letters, 9,* 429–432. DOI 10.1109/LWC.5962382.
10. Hiltunen, J., Vaisanen, V., Juntunen, R., Silventoinen, P. (2015). Variable-frequency phase shift modulation of a dual active bridge converter. *IEEE Transactions on Power Electronics, 30,* 7138–7148. DOI 10.1109/TPEL.2015.2390913.
11. Hu, X., Gong, C. (2015). A high gain input-parallel output-series DC-DC converter with dual coupled inductors. *IEEE Transactions on Power Electronics, 30,* 1306–1317. DOI 10.1109/TPEL.2014.2315613.
12. Li, T., Parsa, L. (2018). Design, control, and analysis of a fault-tolerant soft-switching DC–DC converter for high-power high-voltage applications. *IEEE Transactions on Power Electronics, 33,* 1094–1104. DOI 10.1109/TPEL.2017.2684832.
13. N, G. Yadav, B., Narasamma N, L. (2014). An active soft switched phase-shifted full-bridge DC–DC converter: Analysis, modeling, design, and implementation. *IEEE Transactions on Power Electronics, 29,* 4538–4550. DOI 10.1109/TPEL.2013.2284780.
14. U, P. K, R. Rathore, A. (2013). Extended range ZVS active-clamped current-fed full-bridge isolated DC-DC converter for fuel cell applications: Analysis, design, and experimental results. *IEEE Transactions on Industrial Electronics, 60,* 2661–2672. DOI 10.1109/TIE.2012.2194977.
15. Sathyan, S., Suryawanshi, H., Shitole, A. (2014). Soft switched coupled inductor based high step up converter for distributed energy resources. *40th Annual Conference of the IEEE Industrial Electronics Society*, pp. 1799–1805. Dallas, Texas, USA.

16. Pahlevaninezhad, M., Das, P., Drobnik, J., Jain, P., Bakhshai, A. (2012). A novel ZVZCS full-bridge DC-DC converter used for electric vehicles. *IEEE Transactions on Power Electronics, 27,* 2752–2769. DOI 10.1109/TPEL.2011.2178103.
17. Fardoun, A., Ismail E, H. (2010). Ultra step-up DC–DC converter with reduced switch stress. *IEEE Transactions on Industry Applications, 46,* 2025–2034. DOI 10.1109/TIA.2010.2058833.
18. Kim, E., Kwon, B. (2010). Zero-voltage-and zero-current-switching full-bridge converter with secondary resonance. *IEEE Transactions on Industrial Electronics, 57,* 1017–1025. DOI 10.1109/TIE.2009.2029581.
19. Mousavi, A., Moschopoulos, G. (2014). A new ZCS-PWM full-bridge DC–DC converter with simple auxiliary circuits. *IEEE Transactions on Power Electronics, 29,* 1321–1330. DOI 10.1109/TPEL.2013.2259847.
20. Xiao, H., Xie, S. (2008). A ZVS bidirectional DC–DC converter with phase-shift plus PWM control scheme. *IEEE Transactions on Power Electronics, 23,* 813–823. DOI 10.1109/TPEL.2007.915188.
21. Yu, W., Lai, J., Lai, W., Wan, H. (2012). Hybrid resonant and PWM converter with high efficiency and full soft-switching range. *IEEE Transactions on Power Electronics, 27,* 4925–4933. DOI 10.1109/TPEL.2012.2192293.
22. Mousavi, A., Das, P., Moschopoulos, G. (2012). A comparative study of a new ZCS DC–DC full-bridge boost converter with a ZVS active-clamp converter. *IEEE Transactions on Power Electronics, 27,* 1347–1358. DOI 10.1109/TPEL.2011.2118233.
23. Zhou, S. L., Tian, Y. T., Bi, J. B. (2019). Research on phase-shifted full-bridge DC-DC converter based on FB-ZVZCS. *Power Electronics, 53,* 16–19. DOI CNKI:SUN:DLDZ.0.2019.12.005.
24. Li, W., Jiang, Q., Mei, Y., Li, C., Deng, Y. et al. (2015). Modular multilevel DC-DC converters with phase-shift control scheme for high-voltage DC-based systems. *IEEE Transactions on Power Electronics, 30,* 99–107. DOI 10.1109/TPEL.2014.2301722.
25. Wang, H., Sun, Q., Chung, H., Tapuchi, S., Ioinovici, A. (2009). A ZCS current-fed full-bridge PWM converter with self-adaptable soft-switching snubber energy. *IEEE Transactions on Power Electronics, 24,* 1977–1991. DOI 10.1109/TPEL.2009.2018559.
26. Kumar, M., Ashirvad, M., Babu, Y. N. (2017). *An integrated Boost-Sepic-Ćuk DC–DC converter with high voltage ratio and reduced input current ripple,* pp. 984–990. Chennai, Tamil Nadu, India: Elsevier, Ltd.