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ARTICLE

A Fault Current Limiting Hybrid DC Circuit Breaker

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ABSTRACT

Due to the low impedance characteristic of the high voltage direct current (HVDC) grid, the fault current rises extremely fast after a DC-side fault occurs, and this phenomenon seriously endangers the safety of the HVDC grid. In order to suppress the rising speed of the fault current and reduce the current interruption requirements of the main breaker (MB), a fault current limiting hybrid DC circuit breaker (FCL-HCB) has been proposed in this paper, and it has the capability of bidirectional fault current limiting and fault current interruption. After the occurrence of the overcurrent in the HVDC grid, the current limiting circuit (CLC) of FCL-HCB is put into operation immediately, and whether the protected line is cut off or resumed to normal operation is decided according to the fault detection result. Compared with the traditional hybrid DC circuit breaker (HCB), the required number of semiconductor switches and the peak value of fault current after fault occurs are greatly reduced by adopting the proposed device. Extensive simulations also verify the effectiveness of the proposed FCL-HCB.

KEYWORDS

Fault current limiting hybrid DC circuit breaker (FCL-HCB); high voltage direct current (HVDC) grid; fault current limiting; fault current interruption; DC circuit breaker

1 Introduction

Compared with the traditional line commutated converter (LCC)-based high-voltage DC (HVDC) transmission systems, HVDC grids based on modular multilevel converter (MMC) have more advantages, such as independent control of active and reactive power, easiness to form a multi-terminal network, power supply for passive networks, etc. [1]. These characteristics of the MMC-HVDC grid have solved the problem of large-scale renewable energy integration [2], therefore it has become a research hotspot in recent years.

One of the important factors restricting the development of the HVDC grid is the fault isolation technology [3]. At present, there are two main fault isolation schemes for HVDC grids [4,5]: one is a combination scheme based on converters with fault-blocking capability, such as full-bridge (FB)-MMC, and disconnectors; the other is based on converters without fault-blocking capability, such as half-bridge (HB)-MMC, and DC circuit breakers (DCCBs). The former scheme relies on the FB-submodule (SMs) in the converter to generate a reverse voltage to clear the fault

current after the occurrence of the fault, and then uses disconnectors to isolate the fault line. Because this scheme requires that the number of FB-SMs in the converter accounts for more than 50% of the total number of SMs, it will cause additional investment costs and operation power losses [1]. In addition, the scheme will cause short-term outage of the HVDC grid, which is not conducive to the safe and stable operation of the HVDC grid [2]. Like the alternative current (AC) grid, the latter scheme adopts DCCBs to isolate the fault line directly without causing additional problems. Therefore, this scheme is an ideal solution for HVDC grid fault isolation.

Currently, the proposed DCCBs can be divided into three main types, namely mechanical DC circuit breakers (MCBs), solid-state DC circuit breakers (SSCBs) and hybrid DC circuit breakers (HCBs) [6–9]. MCBs use fast mechanical switches to interrupt the fault current, and its action speed is relatively slow. Besides, because there is no zero-crossing point in the fault current of the HVDC grid, the MCB requires auxiliary circuit to manually create it [6]. The SSCB use the current-block capability of power electronic devices to interrupt fault current and it can operate extremely fast (within 1 ms). However, it requires high investment cost and may cause large power losses [7]. SSCBs are usually used in the power systems of ships, submarines, etc. [8]. The HCB combines the advantages of the MCB and the SSCB, which has the characteristics of low conduction loss and fast action speed [9]. However, it requires many semiconductor switches in series to withstand the transient interruption voltage (TIV), so the investment cost is relatively high. At present, Nanrui Electric Co., Ltd., China and China Xidian Electric Co. Ltd., China have both successfully developed the 500 kV HCBs.

Due to the low-impedance characteristic of the HVDC grid, the fault current develops extremely fast, and within a few milliseconds it can reach several times or even tens of times the rated current. To suppress the rising speed of the fault current, many fault current limiters have been proposed [10–14]. A fault current limiter based on thyristors has been proposed [10]. The device can put a current limiting reactor into operation to limit the fault current during the fault. However, in order to achieve the bidirectional current limiting effect, it is necessary to pre-charge the two capacitors, and the structure is more complicated. To limit the rise speed of the fault current, a method by connecting thyristors and energy dissipation resistors in parallel of the current limiting reactor has been proposed [11]. In addition to the current limiting capability, this method can also shorten the energy dissipation time of the current limiting reactor after the DCCB operates. A high inductance solid-state fault current limiter based on DC reactor has been proposed, which can decrease the fault current with small time delay [12]. A liquid metal current limiter is proposed for medium voltage DC (MVDC) networks [13]. After 1.53 ms of the current limiting reaction time, the current limiter can limit the fault current to half of that without the current limiter. A current-commutation-based fault current limiter has been proposed [14]. By combining the half-control unit and the full-control unit, the fault current can be greatly limited without much negative influence on the DC system.

Most of the fault current limiters proposed at present are independent devices, so installing the fault current limiter requires additional investment costs. Fault current limiting devices have fault current limiting function, HCB on the cut off the fault current has a superior performance. HCB which has the capability of fault current limiting can be implemented in fault current limiting. FCL-HCB can further inhibit the rise of the fault current, and reduce the pressure of the HCB to cut off the fault current, Therefore, a current limiting hybrid DC circuit breaker topology is proposed [15], but it still relies on the DC reactor in the line for fault current limiting. Li et al. proposed a fault current limiting method [16,17]. When a fault occurs, the shunt reactor will be in series state, thus inhibiting the fault current. However, the fault breaking speed of the

shunt reactor is not significantly improved compared with the traditional ABB HCB. To solve this problem, this paper proposes a fault current limiting hybrid DC circuit breaker (FCL-HCB). By integrating the current limiting circuit (CLC) into the HCB, additional equipment investment is avoided. Compared the proposed FCL-HCB with the traditional HCB, the peak value of the fault current is reduced by 35.63%, the energy consumption of the main breaker (MB) is reduced by 47.13%, and the energy dissipation time is shortened by 18.28%.

The rest of the paper is organized as follows. The traditional HCB and the proposed FCL-HCB are introduced in Section 2. In Section 3, the operation principle of FCL-HCB is elaborated. The effectiveness of the proposed FCL-HCB is verified in Section 4. The comparison of the traditional HCB and the proposed FCL-HCB is developed in Section 5. In Section 6, some discussions are given.

2 Topology of FCL-HCB

2.1 Traditional HCB

The HCB has been first proposed by ABB [7], and its topology is shown in Fig. 1.

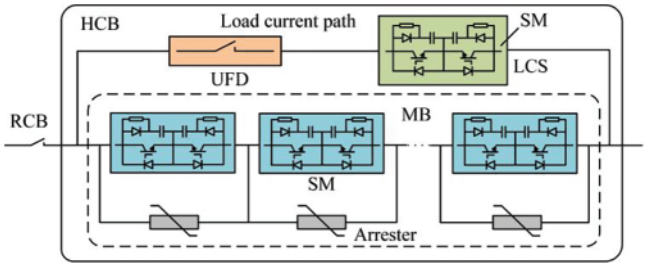

Figure 1: The topology of the traditional HCB

The traditional HCB consists of a residual current breaker (RCB), a load current branch and an MB (Fig. 1). The load current branch is a series branch of the load commutation switch (LCS) and the ultra-fast disconnector (UFD). The MB is composed of many IGBT-based SMs connected in series and arresters. The number of SMs connected in series in the MB may reach hundreds for the high-voltage application, and this will result in high manufacturing cost. The RCB is used to isolate the faulty line physically after the completion of the current interruption process.

When the HCB receives the trip command from the protection, the MB is turned on and the LCS is turned off. At this time, the fault current starts to be transferred to the MB. When the fault current of the load current branch drops to zero, the UFD starts the opening action. The opening time of UFD in zero current state is about 2 ms [18]. After the UFD completes the opening action, the MB is turned off, and the fault current is transferred to the arresters to be dissipated.

2.2 FCL-HCB

The topology of the FCL-HCB proposed in this paper is shown in Fig. 2. It contains an RCB, a load current path, a CLC, an MB and four diode branches D_1–D_4. The RCB and the load current path are the same as those of the traditional HCB. The MB in the FCL-HCB contains many SMs and arresters. However, the SMs in the MB of the FCL-HCB are

different from those of the traditional HCB. The comparison of those two kinds of SMs is illustrated in Fig. 3. Because the direction of the current flowing through the MB of FCL-HCB has been fixed, the SM in the FCL-HCB requires only one IGBT, while the SM in the traditional HCB requires two IGBTs to achieve the bidirectional current interruption. The CLC is composed of two thyristor branches T_1, T_2, a capacitor C, a current limiting inductor L, an energy absorption resistor R_e and a diode branch D_e. The capacitor C is pre-charged, and the polarity of the pre-charged voltage is negative. Several pre-charging methods for capacitors have been proposed [19–21]. Reference [19] proposes to use an isolated auxiliary power supply to charge the capacitor. A laser energy charging scheme for high-voltage capacitors is proposed in [20]. In [21], the authors realize high-voltage capacitor charging by the DC system. The pre-charging methods of the capacitor can be selected according to the actual situation. The operation principles of the proposed FCL-HCB are elaborated in the next section.

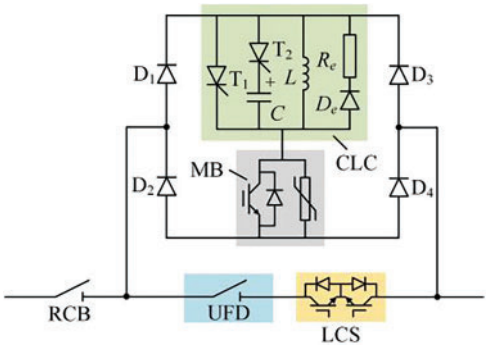

Figure 2: The topology of the FCL-HCB

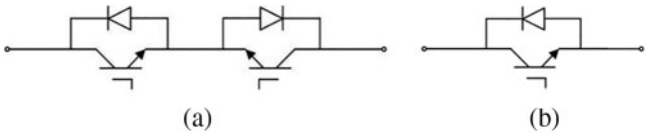

Figure 3: The comparison of SMs in the MB of the traditional HCB and the proposed FCL-HCB. (a) The traditional HCB; (b) The proposed FCL-HCB

3 Operation Principle of FCL-HCB

For the safety of the electronic devices, the HVDC grid usually has very high requirements for fault isolation speed. Taking the Zhangbei four-terminal HVDC grid in China as an example, the protection is required to send trip signal within 3 ms, and the HCB is required to interrupt fault current within 3 ms [22]. For the traditional HCBs, the time from the occurrence of the fault to the fault current being interrupted is 6 ms, so the rise time of the fault current is 6 ms. At this time, the fault current has reached an extremely high value which causes great pressure to the MB. In addition, because the fault identification time left for the protection system is only 3 ms, the reliability of the protection system is greatly challenged.

In order to solve the above problems, the FCL-HCB proposed in this paper puts the CLC into operation immediately when the overcurrent of the protected line is detected, instead of

waiting for the trip command of the protection system. Because the detection time of the overcurrent can be extremely short (less than 0.5 ms), the CLC in the FCL-HCB can greatly reduce the rising speed of the fault current. If the cause of the overcurrent is a fault in the protected line, the FCL-HCB can continue to operate to interrupt the fault current. Otherwise, if the cause of the overcurrent is a non-fault factor or the fault is an external fault, the CLC can exit and the normal operation can be resumed. It is worth noting that during the process of fault current interruption of the FCL-HCB, because the current limiting inductor in the CLC is bypassed by the energy dissipation resistor Re, the energy consumed by the arresters in the MB and the total energy consumption time are both greatly reduced. Thereby, the pressure of devices in the HVDC grid to withstand large currents is greatly reduced.

3.1 Operation Principle After Occurrence of Internal Fault

The detailed operation principle of the proposed FCL-HCB is as follows:

1. Stage I: $t_0 \leq t < t_1$

The two-terminal test system is utilized to analyze the operation principle of the FCL-HCB (Fig. 4). The converters S_1 and S_2 are MMCs, and their output voltages are assumed to be constant during the fault current limiting and the fault current interruption, and their values are considered as U_{dc}. Therefore, during the analysis process, the converters S_1 and S_2 can be assumed as an ideal voltage source U_{dc} in series with an equivalent arm inductance L_{eq}. The pre-charged voltage of the capacitor C is $-U_{cp}$. The length of the DC line is l km. The L-model of the DC line has been adopted to simplify the analysis, and the inductance of the DC line is L_{line}. The load current is I_{load}. In addition, the DC inductor L_{dc} is configured. The occurring time of a short-circuit fault F is assumed as t_0 at αl km from the converter S_1. After the occurrence of the fault, both converters S_1 and S_2 feed fault current into the fault point. The FCL-HCB1 in Fig. 4 is selected as the research objective. The overcurrent is detected at time t_1. The fault current in the FCL-HCB has been illustrated in red (Fig. 5).

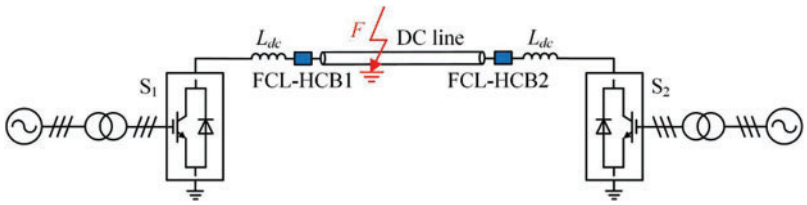

Figure 4: The test system

2. Stage II: $t_1 \leq t < t_3$

When the overcurrent is detected at time t_1, the FCL-HCB starts to operate. At the same time, the thyristor branch T_1 is triggered and the LCS and the MB are both turned on. The fault current starts to be transferred from the load current path to the thyristor branch T_1 and the MB via the diode branches D_1 and D_4. At time t_2, the current flows through the load current path decays to zero, and the UFD starts to open. The UFD completes the open process at time t_3. The time interval between t_2 and t_3 can be considered as 2 ms. During this stage, the equivalent diagram of the FCL-HCB is shown in Fig. 6. The dotted red line in Fig. 6 indicates that the

fault current has been decreased. The total fault current $i_s(t)$ during the period from time t_0 to time t_3 can be adopted as follows:

$$i_s(t) = I_{load} + \frac{U_{dc}}{L_{eq} + L_{dc} + \alpha L_{line}}(t - t_0) \tag{1}$$

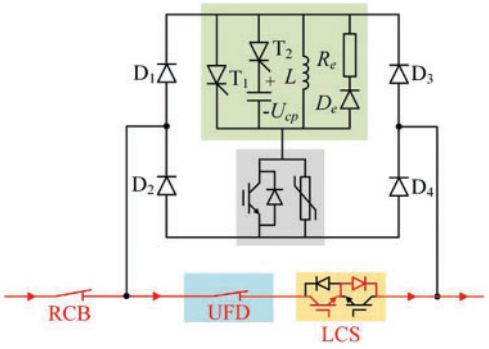

Figure 5: The current in the FCL-HCB in Stage I

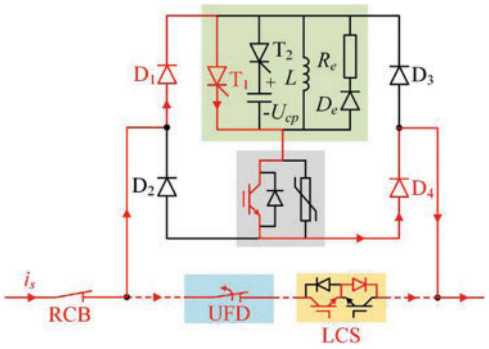

Figure 6: The current in the FCL-HCB in Stage II

3. Stage III: $t_3 \le t < t_4$

At the end of the opening action of the UFD at time t_3, the thyristor branch T_2 is triggered. Because of the reverse voltage applied on the thyristor branch T_1 by the pre-charged voltage of the capacitor C, the current flowing through the thyristor branch T_1 has been decreased. After the thyristor branch T_1 withstands the reverse voltage for a period, its forward blocking ability can be restored at time t_4. The block time of the existing fast thyristor requires about tens to hundreds of microseconds [10]. Stage 3 starts at the trigger time of thyristor T2 and ends at the time when the thyristor T1 is blocked completely. During this stage, since the thyristor T1 is in the process of blocking and has not been completely blocked, no current will flow in the current limiting inductor and De-Re. During this stage, the current paths in the FCL-HCB are illustrated in Fig. 7.

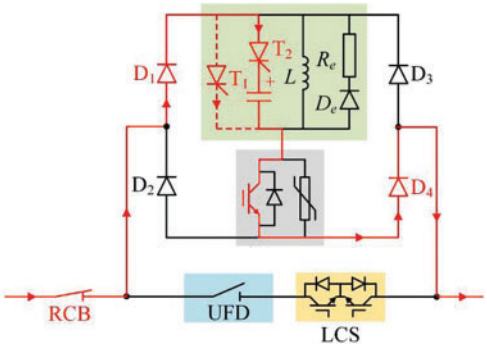

Figure 7: The current in the FCL-HCB in Stage III

4. Stage IV: $t_4 \leq t < t_5$

After the block of the thyristor T_1, the capacitor C and the current limiting inductor L are connected in parallel. The current continues to charge the capacitor C, and the voltage of the capacitor changes from negative value to positive value. After the positive voltage of the capacitor rises to its peak value, the current of the capacitor decays to zero at time t_5. At this time, the thyristor branch T_2 is blocked due to its reverse voltage and zero current condition. Then, the current limiting inductor L is connected in series to the current path, and the operation of the current limiting is completed. The current paths in the FCL_HCB are shown in Fig. 8. The equivalent circuit in this stage is shown in Fig. 9.

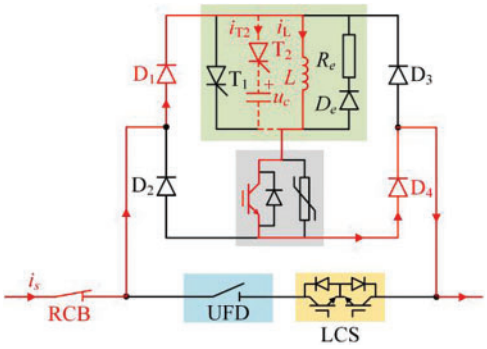

Figure 8: The current in the FCL-HCB in Stage IV

According to Fig. 9, the following differential equations can be obtained.

$$\begin{cases} U_{dc} = \left(L_{dc} + L_{eq} + \alpha L_{line}\right) \dfrac{di_s}{dt} + u_c \\ C\dfrac{du_c}{dt} + i_L = i_s \\ L\dfrac{di_L}{dt} = u_c \end{cases} \tag{2}$$

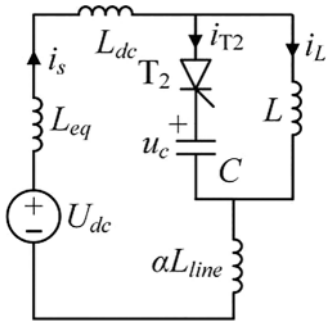

Figure 9: The equivalent circuit in Stage IV

The initial value conditions of the above differential equations can be described by the following equations:

$$\begin{cases} u_c(t_4) = -U_{cp} \\ i_L(t_4) = 0 \\ i_s(t_4) = I_{load} + \dfrac{U_{dc}}{L_{eq} + L_{dc} + \alpha L_{line}}(t_4 - t_0) \end{cases} \tag{3}$$

The expressions of the current $i_L(t)$ and the voltage $u_c(t)$ can be obtained by (2) and (3).

$$\begin{cases} u_c(t) = \sqrt{K_1^2 + K_2^2}\sin[\beta(t - t_4) + \varphi] - K_1 - U_{cp} \\ i_L(t) = -\dfrac{\sqrt{K_1^2 + K_2^2}}{\beta L}\cos[\beta(t - t_4) + \varphi] - \dfrac{K_1 + U_{cp}}{L}(t - t_4) + \dfrac{K_2}{\beta L} \end{cases} \tag{4}$$

where

$$\begin{cases} \beta = \sqrt{\dfrac{L_{eq} + L_{dc} + \alpha L_{line} + L}{L(L_{eq} + L_{dc} + \alpha L_{line})C}} \\ K_1 = -\dfrac{U_{dc}L}{L_{eq} + L_{dc} + \alpha L_{line} + L} - U_{cp} \\ K_2 = \dfrac{i_s(t_4)}{\beta C} \\ \varphi = \tan^{-1}\left(\dfrac{K_1}{K_2}\right) \end{cases} \tag{5}$$

5. Stage V: $t_6 \le t < t_7$

After time delay, the trip signal is received by the FCL-HCB from the protection system at time t_6. The MB is commanded to turn off immediately. Then, the fault current is commutated from the SMs to the arresters to be dissipated. Besides, due to the large TIV generated by the arresters, the fault current in the current limiting inductor L is forced into the R_e-D_e branch. Therefore, the energy dissipation time of the arresters can be greatly reduced. At time t_7, the current through the MB and the RCB decreases to zero. However, the energy dissipation of the

L-R_e-D_e loop may have not completed due to a larger time constant. The current paths in the FCL-HCB are shown in Fig. 10.

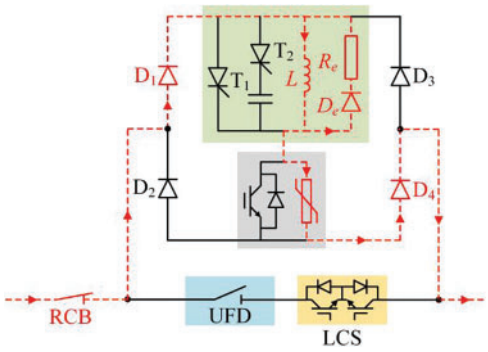

Figure 10: The current in the FCL-HCB in Stage V

6. Stage VI: $t_7 \leq t$

After the fault current interruption at time t_7, the RCB is forced to open to isolate the fault line physically. The current in the current limiting inductor will be dissipated by the resistor R_e and it decreased to zero finally. The current paths during this stage are shown in Fig. 11.

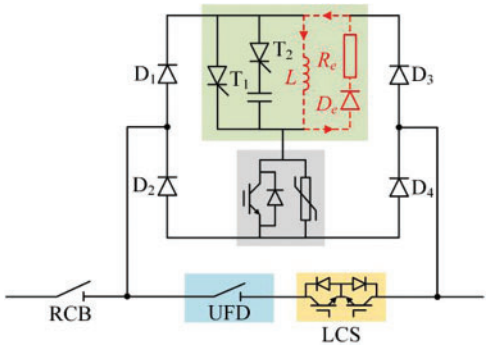

Figure 11: The current in the FCL-HCB in Stage VI

3.2 Operation Principle after Overcurrent Interference

If the fault detection result obtained at time t_6 shows that there is no fault in the DC line, and the FCL-HCB needs to be restored from the current limiting state to the normal state. The operation process is listed as follows:

Firstly, the UFD is commanded to close. After a small period, the close action of the UFD is completed. Then, the LCS is turned on. After that, because the equivalent resistance of the load current path is much smaller than the total equivalent resistance of the current path D_1-L-MB-D_4, the current is gradually transferred into the load current path. After the completion of the current transfer, the MB is turned off, and the FCL-HCB enters the normal operation state.

3.3 Parameter Design

According to the above analysis, the parameters of the main components in the proposed FCL-HCB are designed, including the selection of inductive components and capacitance

components. At present, current limiting reactants are widely used in fault current limiting of MMC-HVDC transmission lines. Considering thet current limiting reactants used in current projects are generally 150 mH, and combined with the current limiting demand of 500 kV MMC-HVDC, the inductance value of current limiting reactance is selected as 200 mH in this paper. Considering the maximum forward voltage the capacitor must withstand is:

$$U_{c\max} = \sqrt{K_1{}^2 + K_2{}^2} - K_1 + U_{cp} \tag{6}$$

The capacitance value is selected according to the maximum forward voltage to be sustained by the capacitor voltage. In this paper, the capacitance of 10 uF is selected.

According to formula (4), we can get the time when the capacitor provides reverse voltage to thyristor T1 is:

$$t_r = \frac{1}{\beta}\left(\arcsin\frac{K_1 + U_{cp}}{\sqrt{K_1{}^2 + K_2{}^2}} - \varphi\right) \tag{7}$$

Based on the formula (7), shut off time of thyristor T1 and the selection of capacitance and the capacitance selection on charging voltage, in order to ensure the thyristor reliably shut off, and we keep reverse voltage is greater than the thyristor turn-off time, therefore, on the basis of considering capacitance value selection, combined with reverse voltage thyristor of capacitance time request, to the selection of charging voltage of capacitor. Since the turn-off time of the thyristor is within tens to hundreds of milliseconds, the time for selecting the capacitor to provide the reverse voltage to the thyristor is no less than 300 ms. Combined with the selected capacitance value, the appropriate pre-charging voltage of the capacitor can be selected.

4 Simulation Analysis

4.1 Test System

To prove the effectiveness of the proposed FCL-HCB, a unipolar test system us built with the PSCAD/EMTDC software (Fig. 4). The R-L model of the DC line is adopted. The detailed model of the MMC is utilized [23]. The pre-charge voltage of the capacitor C is −150 kV. The short-circuit fault F is detected at the midpoint of the DC line. The key parameters of the test system are shown in Table 1.

Table 1: The key parameters of the test system

Parameter	Value
Nominal voltage U_{dc}	500 kV
DC inductance L_{dc}	50 mH
Nominal power of S_1, S_2	500, 500 MW
Number of SMs per arm	100
SM capacitance	10 mF

(Continued)

Table 1 (continued)

Parameter	Value
Arm inductance	29 mH
Nominal voltage of MOV	500 kV
Protection threshold of MOV	800 kV
Capacitance C	10 μF
Current limiting inductance L	200 mH
Energy absorption resistance R_e	20 Ω
Inductance of the DC line	0.85 mH/km
Resistance of the DC line	9.32 mΩ/km
Length of the DC line	200 km

4.2 Simulation Results after Occurrence of Short-Circuit Fault F

The short-circuit fault F is detected at 4.0 s and the overcurrent is detected at 4.0005 s (Fig. 12). At the same time, the FCL-HCB starts to operation. At 4.006 s, the fault current interruption process is performed by the FCL-HCB. The operation principles are shown in Section 3.1.

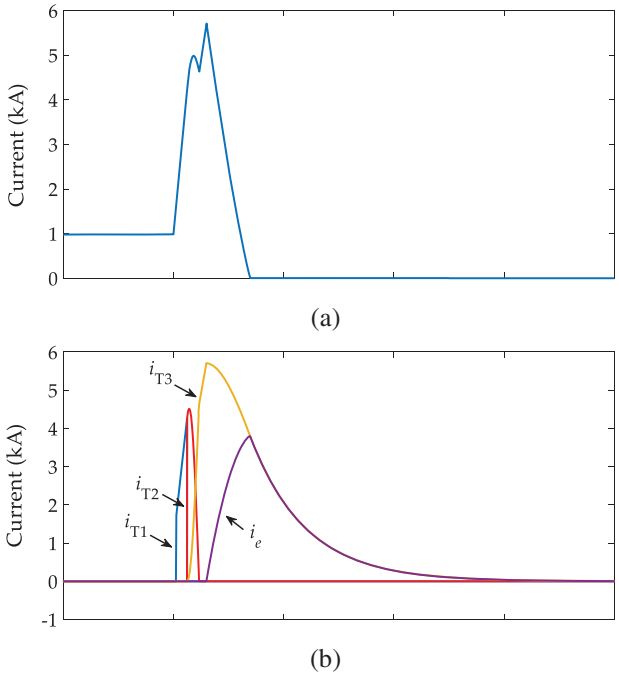

Figure 12: (Continued)

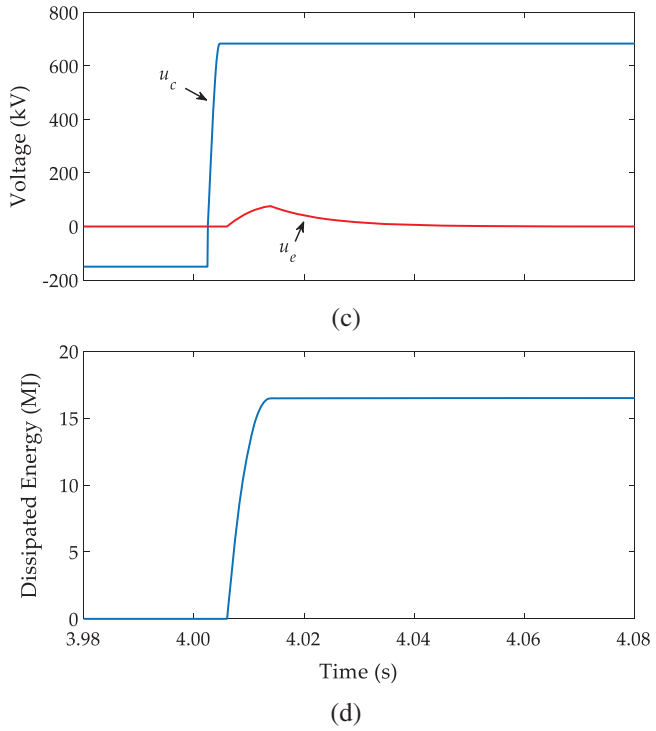

Figure 12: Simulation results after occurrence of the internal short-circuit fault F. (a) The line current; (b) The currents in the CLC (iT1 represents the current in the thyristor branch, iT2 represents the current in the capacitor branch, iT3 represents the current in the limiting inductor branch, i.e., represents the current in the resistance branch); (c) The voltages of the capacitor C and the resistor Re; (d) The dissipated energy of the arresters in the MB

During the current limiting process of the FCL-HCB, the current has transferred from the thyristor branch T_1 to the thyristor branch T_2, and then it transfers from the thyristor branch T_2 to the current limiting inductor L. The capacitor C in the CLC reaches the peak value of nearly 700 kV. When the MB is turned off in 4.006 s, the fault current flowing through the current limiting inductor L starts to be transferred to the energy absorption resistor R_e. This can speed up the energy absorption of fault current in the DC line. The fault current in the DC line decays to zero at 4.0136 s, and the current in the current limiting inductor L decays to zero at 4.061 s due to the much larger time constant. During the fault current limiting and fault current interruption process of the FCL-HCB, the peak value of the fault current flowing through the DC line is about 5.6 kA, the fault current absorption time is about 7.6 ms, and the energy consumption of the arrester in the MB is about 16.6 MJ.

4.3 Simulation Results after Overcurrent Interference

It is assumed that an overcurrent interference occurs at 4.0 s, and the overcurrent is detected after 0.5 ms. Then, the FCL-HCB changes from the normal operation state to the fault current limiting state. At 4.006 s, the FCL-HCB starts to exit the fault current limiting state, and the operation process is shown in Section 3.2. The simulation waveforms show that the current flowing through the CLC is nearly all transferred to the load current path at about 4.5 s (Fig. 13). The results indicate that the proposed FCL-HCB can exit the fault current limiting mode to the normal operation.

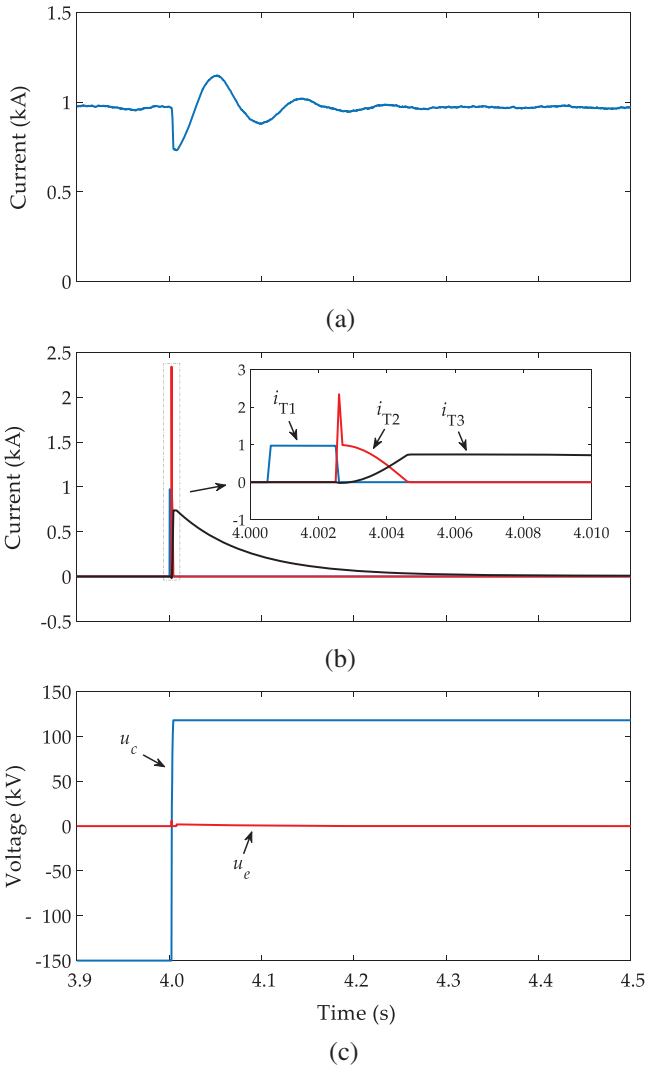

Figure 13: Simulation results after the overcurrent interference. (a) The line current; (b) The currents in the CLC (iT1 represents the current in the thyristor branch, iT2 represents the current in the capacitor branch, iT3 represents the current in the limiting inductor branch); (c) The voltages of the capacitor C and the resistor Re

5 Comparison

5.1 Performance of Fault Current Interruption

Compared the FCL-HCB proposed in this paper with the traditional HCB, and the traditional HCB is used to interrupt the fault current. The fault condition is the same as that in Section 4.2.

The simulation results show that the peak value of the fault current flowing through the DC line is about 8.7 kA, the fault current absorption time is about 9.3 ms, and the energy consumption of the arrester in the MB is about 31.4 MJ (Fig. 14). Compared the proposed FCL-HCB with the traditional HCB, the peak value of the fault current is reduced by 35.63%, the

energy consumption of the arresters in the MB is reduced by 47.13%, and the energy dissipation time is shortened by 18.28%.

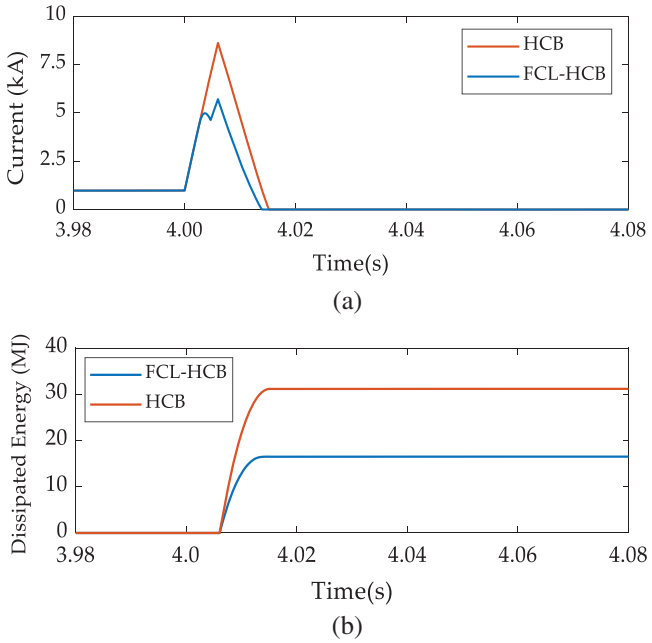

Figure 14: Simulation results (a) The line current; (b) The dissipated energy of the arresters in the MB

5.2 Investment Cost

Because the traditional HCB and the FCL-HCB both have the RCB and the load current, their costs will no longer be considered in the economic comparison. It is assumed that the IGBT FZ3600R17HE4PHPSA1 (1.7 kV, \$1524.85), the diode VS-SD1100C20C (2 kV, \$80.18) and the thyristor VS-ST1230C16K1 (1.6 kV, \$416.33) are used [24]. The rated voltages of the two DCCBs are all 500 kV. The protection threshold of the arresters is considered as 800 kV, and it is 1.6 times of the rated voltage. The peak value of the capacitor C in the CLC is 700 kV.

For the traditional HCB and the FCL-HCB, their MB both needs to withstand the protection voltage of the arresters which is 800 kV. In addition, for the diode branches D_1–D_4 of FCL-HCB, they also need to withstand the protection voltage of the arresters. For the thyristor branches T_1, T_2 and the diode branch D_e of the FCL-HCB, they need to withstand the voltage peak value of the capacitor C which is 700 kV. Therefore, the cost of the semiconductor switches of the traditional HCB and the FCL-HCB are shown in Table 2 when the voltage margin is 50%.

Table 2: Cost of semiconductor switches of the traditional HCB and the FCL-HCB

DCCB type	IGBT	Thyristor	Diode	Total cost
Traditional HCB	1884	0	0	\$2872817.4
FCL-HCB	942	1750	3900	\$2477688.2

The cost of semiconductor switches of the FCL-HCB is less than that of the traditional HCB (Table 2). The energy consumption of the arresters in the FCL-HCB is about half of that of the traditional HCB. Therefore, the cost of arresters of FCL-HCB is lower. Compared with the traditional HCB, the FCL-HCB has the additional cost of the capacitor and the energy absorption resistor, but their cost is much lower than the cost of semiconductor switches and surge arresters. Therefore, the proposed FCL-HCB is more economical than the traditional HCB.

6 Discussion

This paper proposes an FCL-HCB which has the ability of bidirectional current limiting and fault current interruption. Once an overcurrent current is detected, the CLC of FCL-HCB can be quickly put into operation, thereby the rising speed of the current is suppressed. Then, once the internal fault is identified, the FCL-HCB can quickly interrupt the fault current. Extensive simulations have proved the effectiveness of the FCL-HCB.

Compared with the traditional HCB, the FCL-HCB reduces the peak value of the fault current by 35.63%, the energy consumption of the arresters in the MB is reduced by 47.13%, and the energy dissipation time is shortened by 18.28%. In addition, the economic analysis results show FCL-HCB is more economical.

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