

**ARTICLE**

# Design and Analysis of Cascaded Hybrid-Bridge Multi-Cell Multilevel Inverter with Reduced Total Harmonic Distortion Profile

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**ABSTRACT**

This multilevel inverter methodology is the center of focus among researchers in recent era. It has been focused due to its advantages over existing topologies, drawbacks and improvement of power quality, Multi-level inverter has the ability to generate nearly sinusoidal waves. This sinusoidal wave can be further improved by increasing the level of output voltage or with the help of filter design, and this manuscript presents single-phase Multi cell Multi-Level Inverter (MLI). It has been considered for reducing component count to get a higher number of output voltage levels and lower Total harmonics distortion profile. It comprises with four symmetric DC input voltage and 10 IGBT switches to produces stepped output of 9 level, and when deploy asymmetric Dc voltage source the same circuit will produce 31 level output with some changes in firing scheme, moreover this circuit is the family of cascaded hybrid bridge inverter so this circuit covered advantage of CHB MLI, This circuit uses lower no. of switch as compared to existing conventional MLIs such as FC-MLI, CHB-MLI, NPC-MLI, This paper also provides one of most pertinent controls and modulation mechanisms for a MLI using a hybrid reference/carrier-oriented sinusoidal PWM mechanism. At last, simulated outcomes are to validate the performance of both architectures in MLI structure as well as verify the concept.

**KEYWORDS**

Conventional topology; multi-level inverters (MLIs); pulse width modulations (PWM); reduced component counts; total of harmonics distortion (THD)

## 1 Introduction

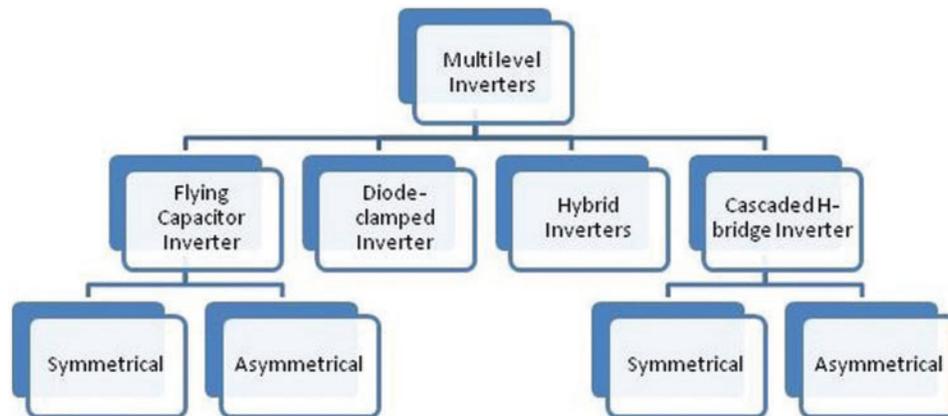
MLI has been increasingly noticed in current decades due to their capacity to operate at high voltages, with maximum ease, and with minimal electromagnetic interference (EMI) [1]. MLI has no IGBT; this IGBT has different stress voltage, conduction, and switch times [2]. The multi-level inverter has the lowest total harmonic profile [3] without in type of filter [4]. The quality of a multi-level inverter can be enhanced by increasing its number of output voltage levels [5]; however, this process increases number of power switches [6], which leads to an increase in its cost & system complexity [7], so researchers are focusing on decreasing its number of switch count and increasing its output levels [8].

Popular MLI are categorized into two main categories: one of them, whose shared single Dc voltage source, like diodes clamped MLIs (DC-MLI) [9] & flying capacitors MLIs (FC-MLI) [10],



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and another one, isolating Dc voltage source [11], like cascade, as mentioned in Fig. 1. Newest MLI family and architectures at which Dc Input voltage remain the same here in [12]. The MLI is an appropriate option for significant power ratings, good quality output waveforms, and decent dynamic performance [13].



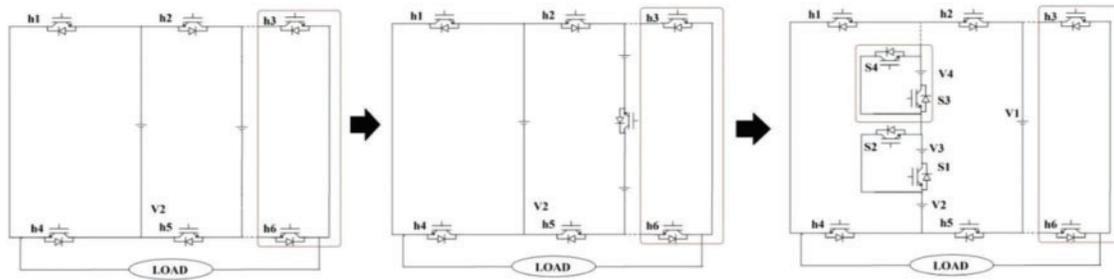
**Figure 1:** Types of multilevel inverters [10]

The drawback is MLI requires a higher number of power switching devices to produce output [14], and due to a higher number of devices, we need higher firing gate pulses to synthesize the output voltage [15]. As a result, the entire system could become more costly and complicated [16].

Among all such topologies [17], the cascaded hybrid bridge inverter [18] also has the most popular topology [19]; this inverter topology continues to focus on research due to its simplicity of expansion to the appropriate number of levels [20]. Cascaded MLIs have been built by connecting multiple 1-phase inverters in sequence; the above architecture may achieve moderate output voltages [21]. In determining the magnitude of the Dc voltages employed [22], cascaded hybrids bridge MLIs [23] may also be broken into two classes based on Dc source amplitude [24]. If the entire Dc voltages source has the same magnitude [25], then MLI is said to be symmetrical; otherwise, it is considered asymmetrical [26]. The adaptability of an asymmetrical cascaded hybrid bridge inverter [27] is appropriate for achieving a higher number of levels, although it typically needs a higher semiconductor device [28]. The modularity of symmetric Cascaded H-Bridge (CHB) MLIs is reasonable, but it uses many semiconductor devices [29]. As a result, asymmetric cascaded Hybrid Bridge MLIs [30] is used to obtain a high voltage level for a given switch [31]. And here, we discussed the CHB family's topology with the implementation of Symmetric and asymmetric methodology [32] and a smaller number of power devices compared to the existing MLI topology [33]. This new topology can achieve 31 levels with asymmetric Dc voltage, and when deploying a symmetric Dc voltage source [34], the same circuit will produce nine-level voltage output; here, we define controllability [35], methodology, & THD (Total Harmonic Distortion) [36] profile with the help of MATLAB simulation.

## 2 Multilevel Topology

As we have seen in Fig. 2, modification of the basic main circuit to the modified circuit, the question is, what is the need for this type of modification required, as we have considered the multi-level inverter (MLI) base circuit for the modification and enhanced the performance [36].



**Figure 2:** General single-phase circuit of MLI (a) Base circuit (b) Semi cross switched multi-level inverter (c) Semi-cascaded multilevel inverter

We observe that the Base circuit, modified with an additional IGBT and one Dc source [37], means the circuit's output voltage increase one level [38], so the circuit output voltage waveform improved; next stage, the same circuit is modified with another Dc voltage source and IGBT's [39], effectively increases no. of output voltage levels so the output of circuit would be improved [40].

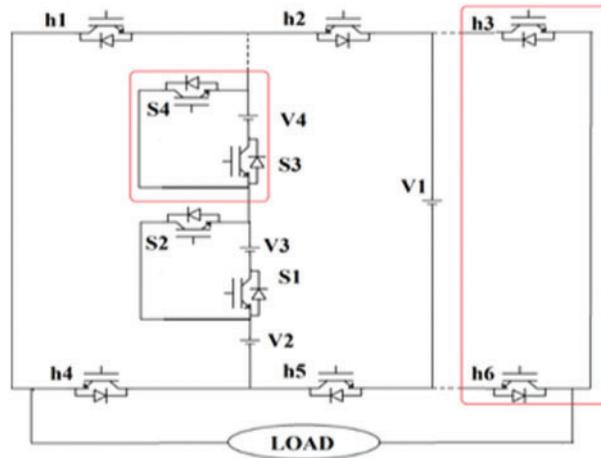
Here are some reasons to move this multilevel inverter modification.

- We will not be able to get a MLI, as demonstrated in Fig. 2c without the development of circuit (b).
- In another one, we will not be able to use an asymmetric voltage source to achieve higher no. of levels with circuit (b), so it is mandatory part to modify another stage, as shown in Fig. 2c.
- Circuit (c) can be utilized to attain 31 levels of voltage output with the help of an asymmetric voltage source.

### 2.1 Generalized Structure of Semi-Cascaded MLI

The number of components needed in MLI topologies according to the input Dc voltage. It indicates that no. of levels increase as input DC voltage increases. The essential components in MLI configuration are semiconductor devices and accompanying simple drive circuits. As even the number of components rises, so the size and price of the multilevel inverter will also increase, and the complexity of the control system will increase. Fig. 3 depicts the structure of a Multi-Cell Multilevel Inverter.

This circuit is implemented with the help of the symmetric Dc voltage supply, and when we use 4 symmetric voltage sources, it can achieve a 9-level of output and further increase its output level by increasing the number of cells or employing an asymmetric Dc voltage supply, it can achieve 31-level of output voltage with the same circuit by some modification in firing scheme, this is the one advantages of this circuit.



**Figure 3: Semi-cascaded MLI**

The presented circuit is motivated by preceding semi Cross Circuit switching Multi-level Inverters, as mentioned in Fig. 2b, and the appropriate linkage of many forms of cells with the help of 10 semiconductor devices that provide divergent routes to start generating the output voltage waveform within all phases with both positively and negatively polarization in output. Every cell is made up of semiconductor devices and one direct current source (Dc voltage source). It is also worth noting that  $V_1 = V_{dc}$  inside the described architecture. Unique Dc sources voltage in each cell generates a given output voltage waveform. The offered inverters can supply the number of each Dc supply in the outputs. As a result, the highest voltage inside the outputs would equal the total of the amplitudes of the DC supply. Max output voltage ( $V_{o,max}$ ) of architecture has represented by Eq. (1)

$$V_{o,Max} = \sum_{i=1}^n V_i \quad (1)$$

Wherever  $n = \text{no. of Dc sources}$

Each switching causes an unwanted drop of voltage, which seems referred to as power losses in the form of switching and conduction loss. Switching loss occurs when the switch moves from an OFF to an ON and conversely. Conduction loss will create over the duration of one state. To compute the maximal voltage output, however, the ON-mode power loss of switching is considered to be  $V_{dc}$ , therefore Eq. (2) assesses the maximal voltage output when everyone switching power loss is included.

$$V_{o,Max} = \sum_{i=1}^n V_i - (n + 2) V_d \quad (2)$$

For asymmetric topology

$$V_{o,Max} = \sum_{i=1}^n V_i - (n + 1) V_d \quad (3)$$

For symmetrical topology

The switch voltage ratings are a key issue in multilayer inverters. The overall peak inverse voltages (PIV) of the switch is determined using the Eq. (4) below.

$$PIV = \sum_{j=1} PIV_{Switchj} \quad (4)$$

### 2.1.1 Symmetrical

Magnitude value of all Dc voltage sources is equivalent to  $V_{dc}$  for symmetric inverters. In considering the symmetric architecture, the switch associated with a single Dc supply, Fig. 3, depicts the symmetrical inverter provided. The possible max voltages and also the number of operating voltages (m) inside the intended symmetrical inverters are described in the subsequent formula.

$$V_{o,max} = n \times V_{dc} \quad (5)$$

$$m = 2n + 1$$

### 2.1.2 Asymmetric

The Dc power supplies of the different cells in the intended asymmetrical MLI are not equivalent. With the same cell count, asymmetrical inverters deliver more stages in the output current than in their symmetrical equivalent.

The DC voltage of the separated cell in Fig. 3 is determined as per a geometric sequence with a component of p in the asymmetrical scheme.

$$V_i = p_{i-1} V_{dc} \quad (6)$$

It belong from 1 to n, whenever there are 2

For n-Dc source, max. Voltage and no. of Voltage stages are as follows:

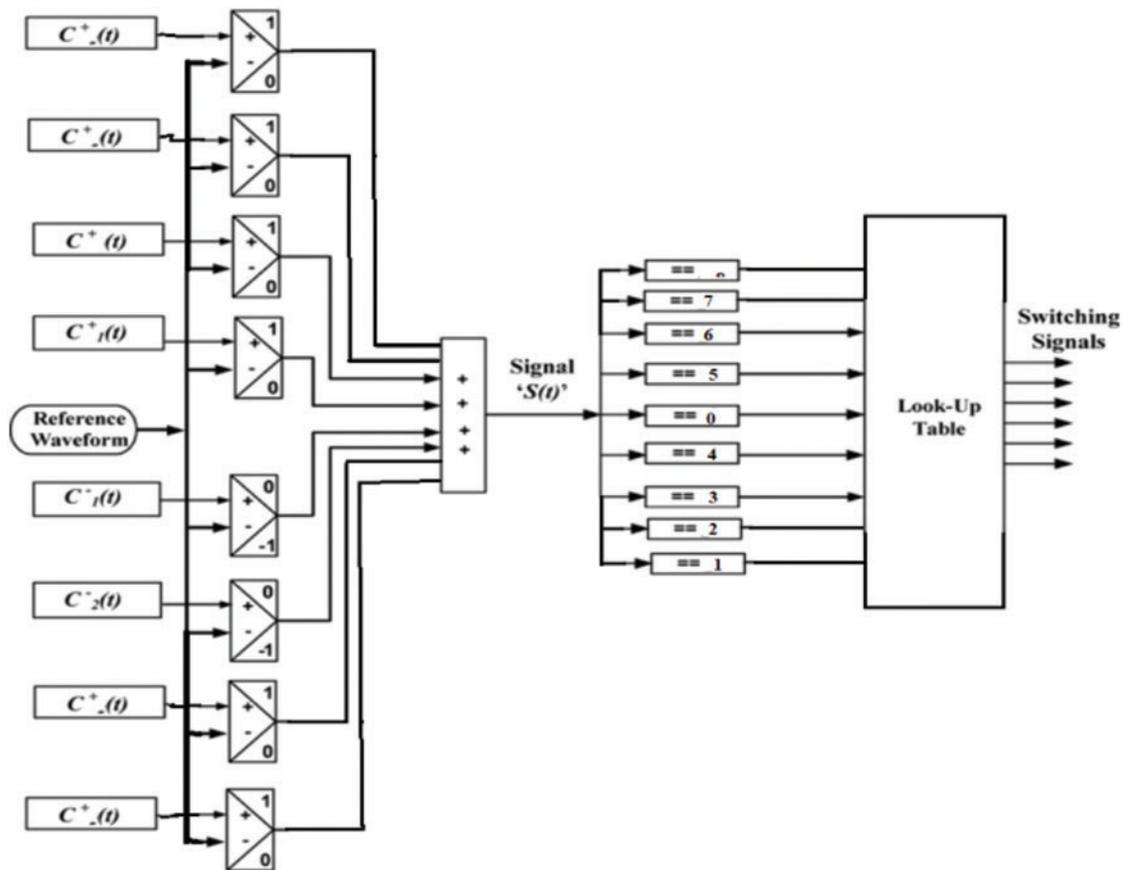
$$V_{o,Max} = \frac{1 - p^n}{1 - p} V_{dc} \quad (7)$$

$$M = 2 \frac{1 - p^n}{1 - p} + 1 \quad (8)$$

Wherever n = no. of Dc source

## 3 Switching Scheme

The inverter's modulation schemes are critical since they are directly connected to the system's total performance [41]. MLI has investigated many forms of modulation schemes [42]. It is utilized to manage the output voltage/current and to calculate MLI's two key parameters, low switching & percentage of THD [43]. A modulating signal's goal was to provide a stepwise waveform which is the closest estimate of the particular reference signal, including variations in amplitude level, frequencies, and a vital element, i.e., typically sine's wave in steady-state [44]. The simple visual depiction of total modulation approaches is displayed in Fig. 4. Depending on the switch's frequencies, the two main modulation methods used in Multi-cell multi-level inverters [45] are Fundamental carrier frequency & fast switching frequency [46]. The two basics fast switching frequencies are PWM and space vector modulations [47].



**Figure 4:** Multi-level inverter using a control scheme

In Multi-cell, Multi-level inverter modulator controls [48], high-switching-frequency modulation approaches such as the multi-carrier levels switch Pulse width modulation have been applied [49]. Low-switching-frequency approaches, on the other side, low-switching-frequency approaches include proactive harmonics removal [50], selective harmonic [51], and the Fundamental switching frequency technique [52]. This design may be changed using any one of these ways with appropriate adaption [53]. The multi-carrier PWM system is employed in this article. Inside a multi-carrier PWM system [54], the carrier's signals are equated by the reference signals [55], & also the resulting waveforms are utilized to switch tools at different voltage levels [56]. In this design, one switch can assist in the synthesizing of many levels at the output terminals. Furthermore, as previously stated, appropriate usage of 10 modes (namely, modes 1, 2, 3 . . . , & 10) would result in basic  $T_2$  and  $T_2$  switches that carry voltage stress of  $2 \cdot V_{dc}$  each one as opposed to other switches that carry voltage stress of  $V_{dc}$ , respectively. As a result, in this part, a control method is provided where such a move is used to generate 9-level outputs. Nevertheless, the operation could be applied to high-level inverters.

### 3.1 Modulation Scheme

The figure depicts the modulation scheme's circuit illustration in the Fig. 4, and also the waveform is represented in Fig. 5. The four triangular waves with frequencies of 2.2 kilohertz each are employed for the carrier. Carrier's signals [57] are typically arranged in alternating phases oppositional [58].

This reference signal is a sine waveform [59] with a frequency of 50 hertz, but it has been converted sine wave into a full-wave rectified signal because of ease of use, so half rectified signal finished at 0.01 another rectified signal has started after a phase shift of 0.01 and finished at 0.02, which is similar to the 50 hz frequency. Carrier signals [60] that are higher than the 0 reference value are denoted by way of “ $C_{k(t)}^+$ ” where  $k \in 1, 2, 3,$  and  $4$ , whereas all individuals who are lower than the 0 reference value are marked by way of “ $C_{k(t)}^-$ ” where  $k \in 1, 2, 3$  and  $4$ . This reference is compared to the carriers continually [61]. Then the comparator returns “ $k$ ” if the references are higher to carriers  $C_{k(t)}^+$ ; else, it returns “ $k(t)$ ”. Whether the reference frequency is more than the frequency of the carrier. “ $C_{k(2)}^+$ ” then the comparator returns. “ $C_{k(2)}^+$ ”, else returns “ $C_{k(1)}^+$ ”. The acquired signals have combined for making an aggregate signal, i.e.,  $a(t)$ . To generate the switching signal via signaling  $a(t)$ , a 1:1 correspondence between both the level in aggregate signal  $a(t)$  displayed in Fig. 6 and the level in output waveforms are used (t). Signals  $a(t)$  are checked to constant current density, and also the outputs are sent to switching correlating to a level to use the hash table provided in Table 2. The ORed signals for the levels give 0 to gates for every switch.

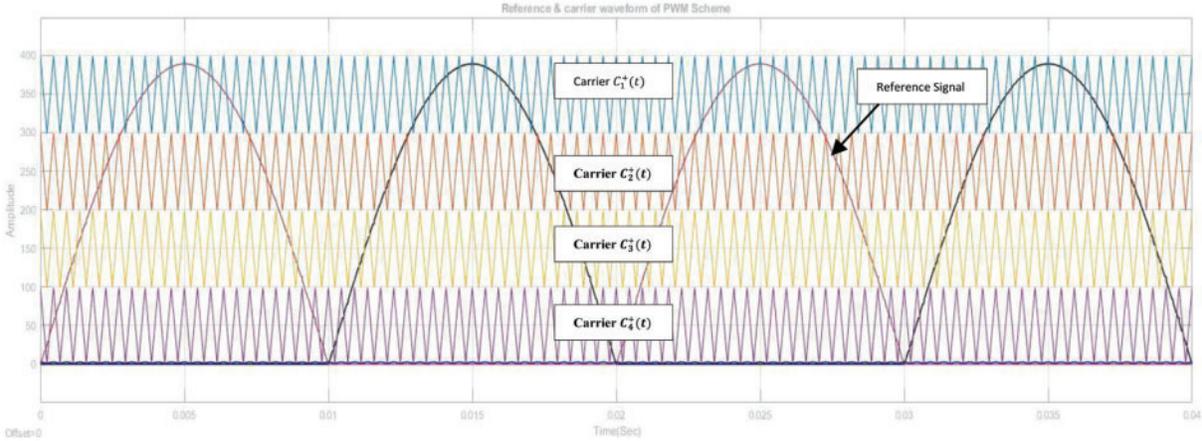


Figure 5: Reference waveform & carrier waveform for 9-level output scheme

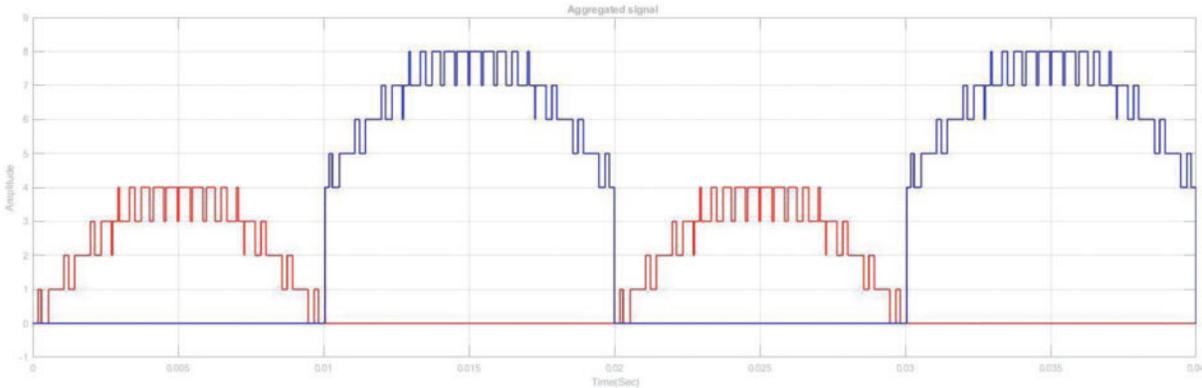
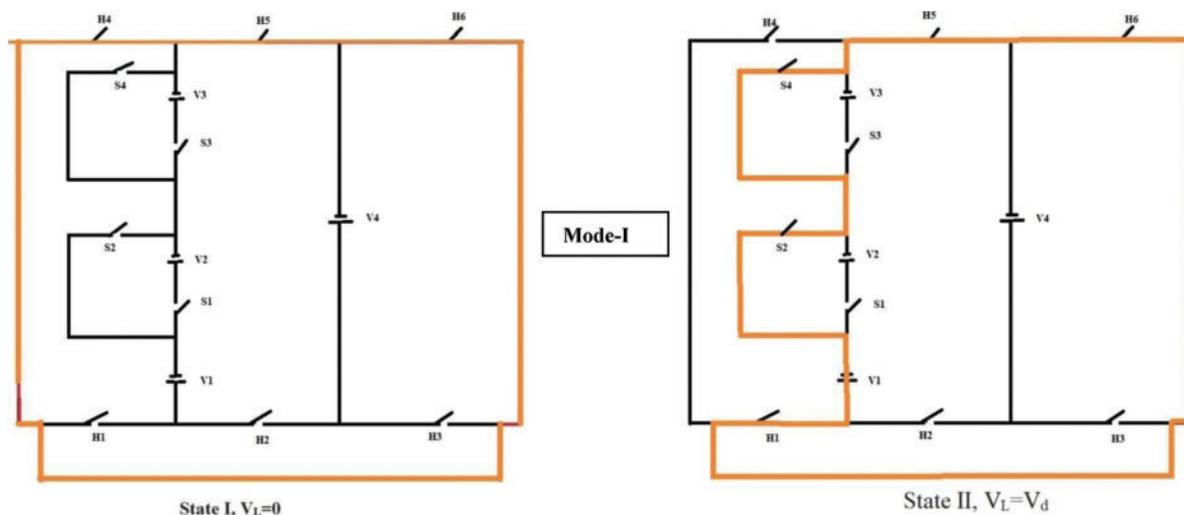


Figure 6: Aggregated signal

The MATLAB/Simulink tool is employed to make a MLI. 4 input Dc sources are employed, where  $E_1 = 100\text{ v}$ ,  $E_2 = 100\text{ v}$ ,  $E_3 = 100\text{ v}$ , and  $E_4 = 100\text{ v}$  as detail system specification mentioned in Table 1. The resulting switch pulses are displayed in Fig. 8, and their switch statistics are presented in Table 2 and Fig. 7; this reveals that switching  $h_2$  &  $h_5$  function at a core frequency of approximately 50 Hz, whereas switching  $h_1$ ,  $h_4$ ,  $h_3$ , and  $h_6$  work at a freq. of 2.2 kHz. Therefore, lower-voltage-rated switches run at the higher frequencies, incurring switching loss, whereas higher-voltage-rated switches work at core frequencies, incurring a higher conductive loss. The net loss among the switching is allocated in this way.

**Table 1:** Parameters for system

Parameters	Values
Reference freq.	50 Hertz
Carrier freq.	2200 Hertz
Load inductance	3 mH
aLoad resistance	1 ohm
Dc source	$E_1 = 100\text{ v}$ $E_2 = 100\text{ v}$ $E_3 = 100\text{ v}$ $E_4 = 100\text{ v}$



**Figure 7:** (Continued)

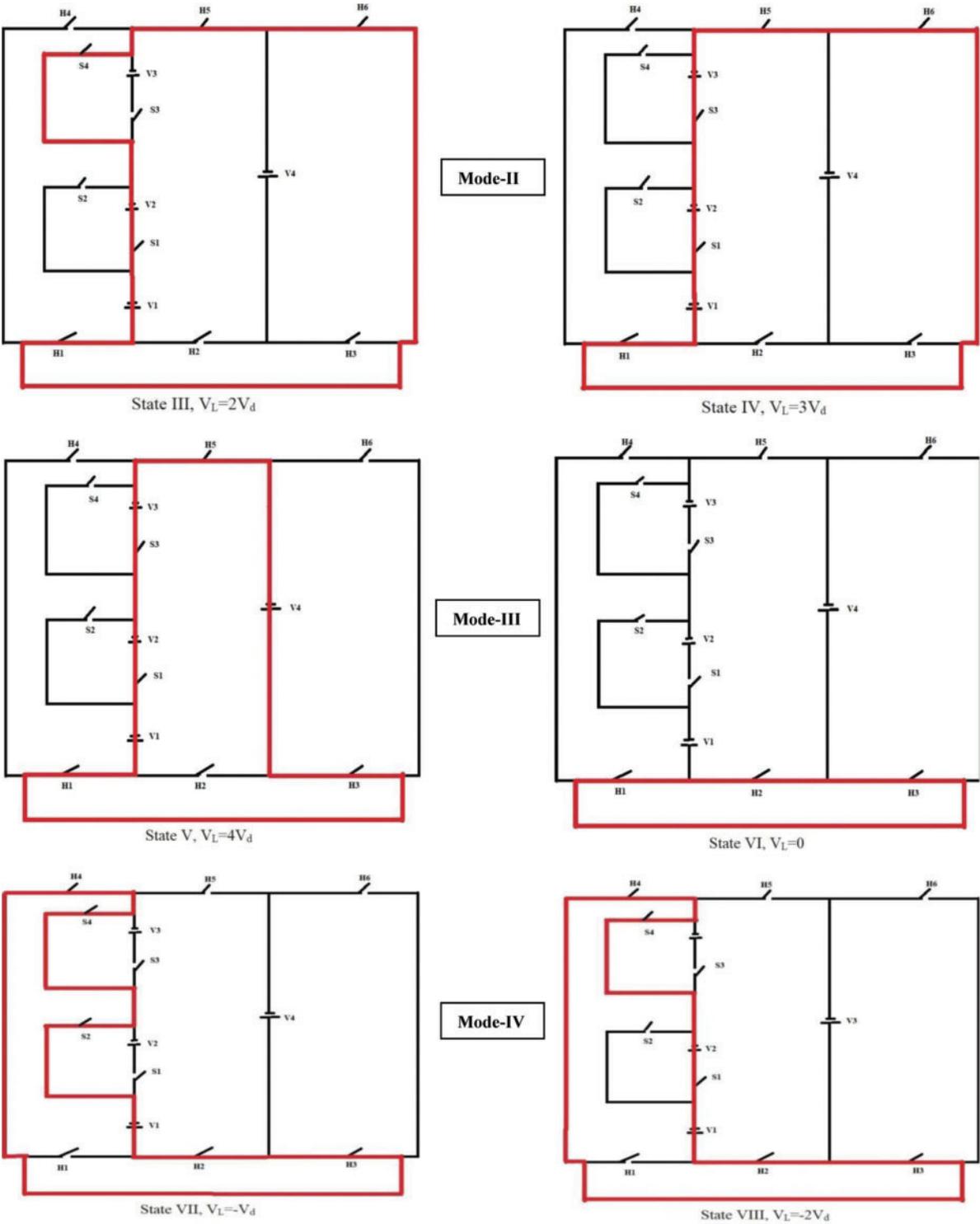


Figure 7: (Continued)

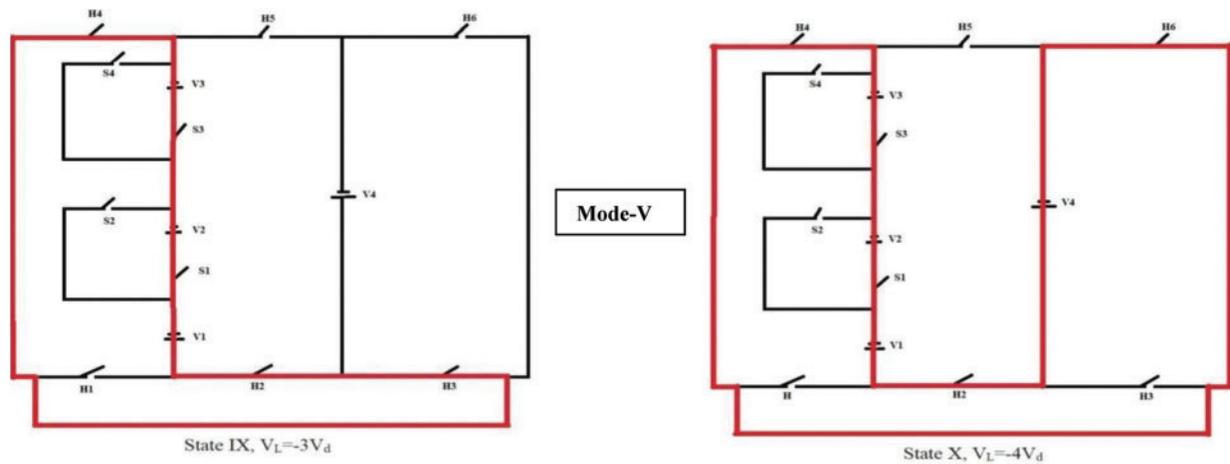
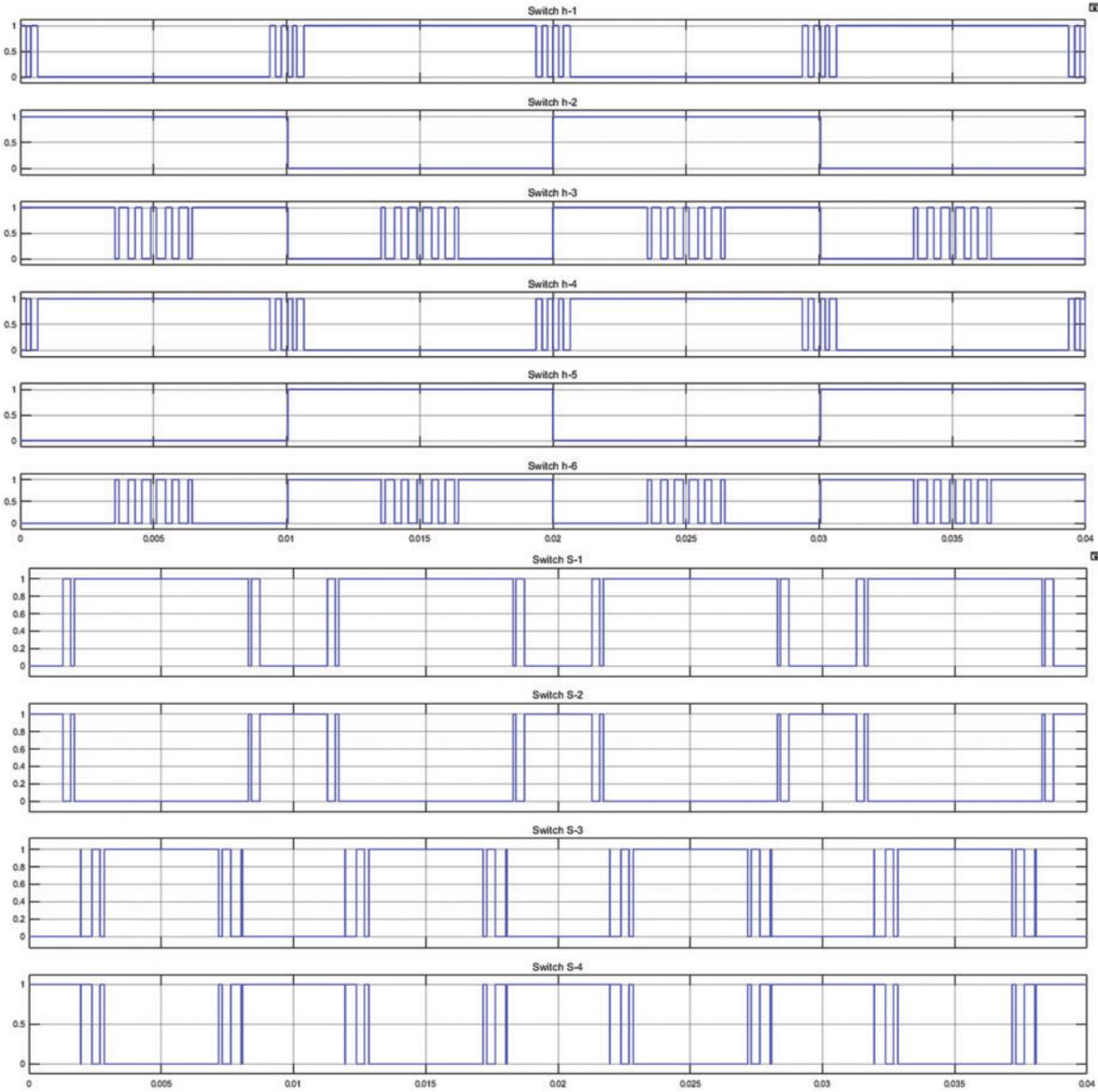


Figure 7: Multi-level working modes

Table 2: Number of modes, nodal voltages, switch states & source currents for topologies on 4-input sources

Voltage levels	Modes	Load voltage [v]	Switches ON state									
			S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	S <sub>4</sub>	H <sub>1</sub>	H <sub>2</sub>	H <sub>3</sub>	H <sub>4</sub>	H <sub>5</sub>	H <sub>6</sub>
0	1	0	0	1	0	1	1	1	1	0	0	0
E1	2	100	0	1	0	1	0	1	1	1	0	0
E1 + E2	3	200	1	0	0	1	0	1	1	1	0	0
E1 + E2 + E3	4	300	1	0	1	0	0	1	1	1	0	0
E1 + E2 + E3 + E4	5	400	1	0	1	0	0	1	0	1	0	1
0	6	0	1	0	1	0	1	0	0	1	1	1
-E1	7	-100	0	1	0	1	1	0	0	0	1	1
-(E1 + E2)	8	-200	1	0	0	1	1	0	0	0	1	1
-(E1 + E2 + E3)	9	-300	1	0	1	0	1	0	0	0	1	1
-(E1 + E2 + E3 + E4)	10	-400	1	0	1	0	1	0	1	0	1	0



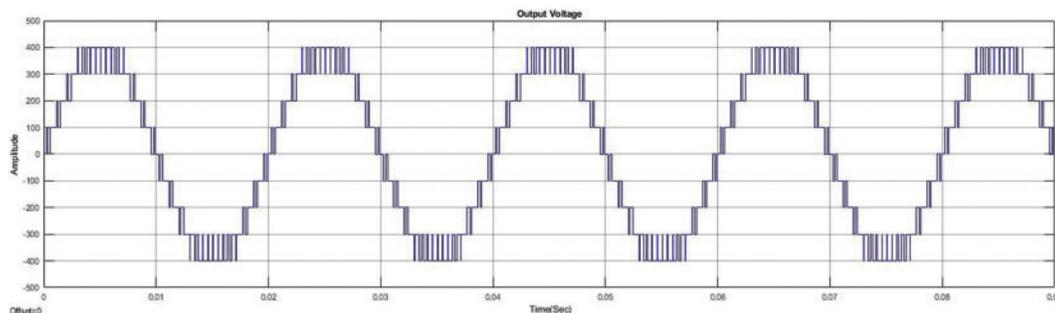
**Figure 8:** Gate switching pulses for the 9-level inverter

There are ten working states of the proposed circuit, by which got different nine levels, four different output produce positive half-wave another four sates produce a negative half-wave which as follows:

- State I.** To achieve voltage level ( $V_L = '0'$ ) on the connected load side, switches  $H_4, H_5,$  and  $H_6$  are switched ON. In this state, the total output voltage is zero at Load.
- State II.** To achieve a voltage level ( $V_L = '+V_1' = 100$  v) on the connected load side, switches  $H_1, S_2, S_4, H_5,$  and  $H_6$  are switched ON. In this state, the total output voltage is 100 v at Load.

- State III.** To achieve a voltage level ( $V_L = 'V_1 + V_2' = 200$  v) on the connected load side, switches  $H_1, S_1, S_4, H_5,$  and  $H_6$  are switched ON. In this state, the total output voltage is 200 v at Load.
- State IV.** To achieve a voltage level ( $V_L = '+V_1+ V_2+ V_3' = 300$  v) on the connected load side, switches  $H_1, S_1, S_3, H_5,$  and  $H_6$  are switched ON. In this state, the total output voltage is 300 v at Load.
- State V.** To achieve a voltage level ( $V_L = 'V_1 + V_2 + V_3 + V_4' = 400$  v) on the connected load side, switches  $H_1, S_1, S_3, H_5,$  and  $H_3$  are switched ON. In this state, the total output voltage is 400 v at Load.
- State VI.** To achieve a voltage level ( $V_L = '0'$ ) on the connected load side, switches  $H_1, H_2$  and  $H_3$  are switched ON. In this state, the total output voltage is 0 v at Load.
- State VII.** To achieve a voltage level ( $V_L = '-V_1' = -100$  v) on the connected load side, switches  $H_3, H_2, S_2, S_4,$  and  $H_4$  are switched ON. In this state, the total output voltage is  $-100$  v at Load.
- State VIII.** To achieve a voltage level ( $V_L = '-V_1 - V_2 = -200'$ ) on the connected load side, switches  $H_3, H_2, S_1, S_4,$  and  $H_4$  are switched ON. In this state, the total output voltage is  $-200$  v at Load.
- State IX.** To achieve a voltage level ( $V_L = "-V_1 - V_2 - V_3" = -300$ ) on the connected load side, switches  $H_3, H_2, S_1, S_3,$  &  $H_4$  are switched ON. In this state, the total output voltage is  $-300$  v at Load.
- State X.** To achieve a voltage level ( $V_L = '-V_1 - V_2 - V_3 - V_4 = -400'$ ) on connected load side, switches  $H_6, H_2, S_1, S_3,$  &  $H_4$  are switched ON. In this state, the total output voltage is  $-400$  v at Load.

Figs. 9 and 11 illustrate the load voltage, current waveforms respectively Figs. 10 and 12 illustrate its harmonic spectra of load voltage and load current; results reveal that the 9-level reference voltage has equivalent stages at 100 volts each and a THD of 1.07 percent. Furthermore, given an R–L load, the load current waveforms (where  $R = 2$  &  $L = 2$  mH), then also its harmonics spectra, that is 0.14 percent.

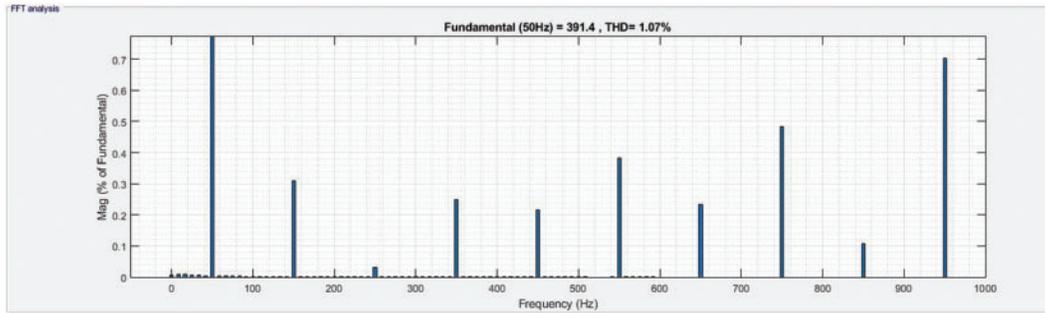


**Figure 9:** Simulation result of 9-level voltage output

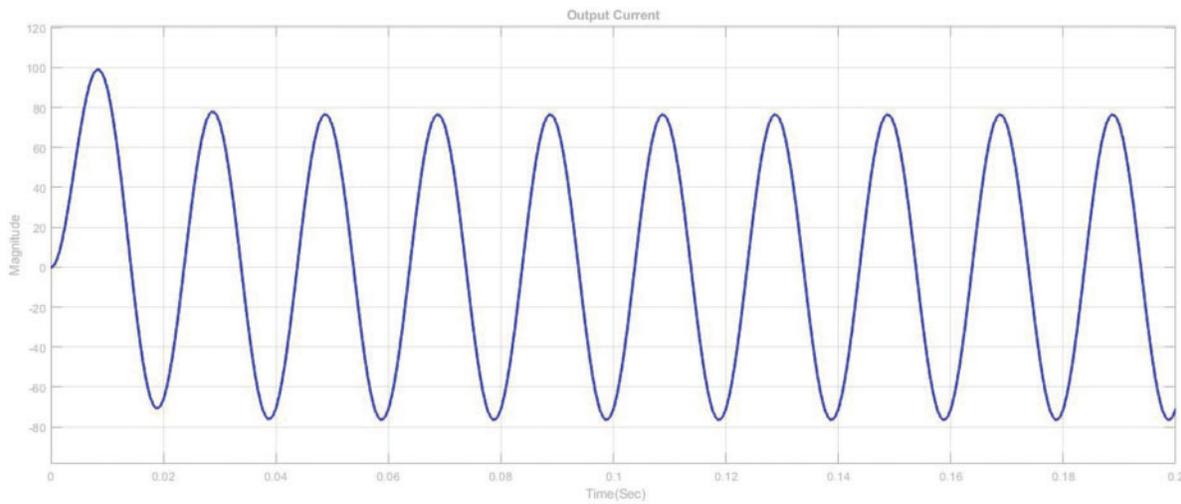
#### 4 Losses Calculation

The related loss of voltage source converters is equivalent to the sum of energy losses caused by individual semiconductors. Loss sustained by a semiconductor diode is often classified into two types:

1. Whenever the circuit is in a block condition (that is, OFF-mode);



**Figure 10:** Total Harmonic distortion (THD) of output voltage



**Figure 11:** Simulating outcome of 9-level MLI current output

2. Whenever the circuit is in a conduct condition (that is, ON-mode).

While the circuit switches (that is, the changing mode from ON mode to OFF mode or conversely). Because leakage currents have been almost non-existent during block conditions [62], the loss remains small. As a result, just conduct & switch loss were taken into account when calculating loss related to these inverters.

#### 4.1 Conduction Loss

As illustrated in Fig. 7, all switching needed in this architecture is unidirectional conduct & bidirectional block. The instant conduction loss of conventional transistors and diodes is.

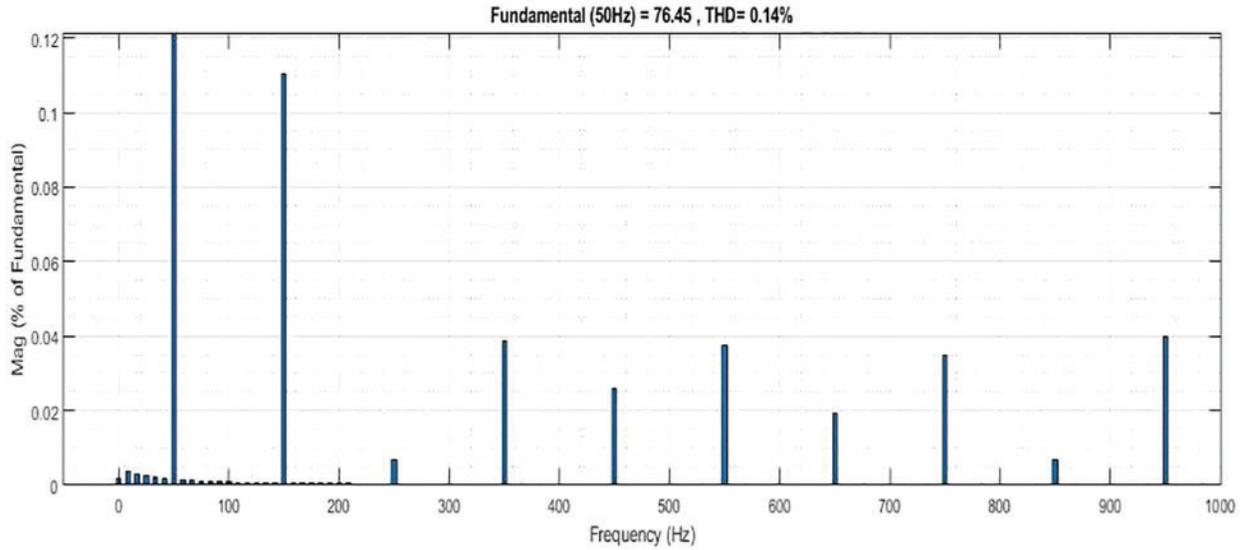
$$\tau_{c,T}(t) = [V_T + R_T i_\alpha(t)]i(t) \tag{9}$$

$$\tau_{c,D}(t) = [V_D + R_D i(t)]i(t) \tag{10}$$

Here,

$\tau_{c,T}(t)$  &  $\tau_{c,D}(t)$  = instant conduction loss of the transistors circuit & diodes, correspondingly.

$V_T$  &  $V_D$  = ON-mode voltage drops.



**Figure 12:** THD of output current

RT & RD = equivalent ON-mode resistance of the transistors circuit & diodes, correspondingly.

$\alpha$  = constant governed by transistors features.

The conductive switch must carry the load current  $s i_L(t)$  at any specified period. Furthermore, based on the output voltage level and the  $i_L(t)$  Direction, a specific switch's transistors circuit or diodes operate. As illustrated in Fig. 7 in modes 4, if the  $i_L(t)$  is greater than zero, the transistors circuits of switching h3 & h2 current, whereas the diodes of switching q1 flow. Whenever  $i_L(t) = 0$ , the transistors circuit of switching T1 current, together with the diode of switching T3 & T2. Letting  $N_D(t)$  &  $N_T(t)$  Represent the number of the current diode and transistor circuits, correspondingly, at every point in time. The averaged conduction loss may therefore be stated by the following Eqs. (9) and (10):

$$\tau_{c,avg} = \frac{1}{\pi} \int_0^{\pi} [\{N_T(t) V_T + N_D(t) V_D\} i_L(t) + \{N_T(t) R_T i_L^{\alpha+1}(t)\} + \{N_D(t) i_L^{\alpha^2}(t)\}] d(\omega t) \quad (11)$$

#### 4.2 Switching Loss

To determine the overall switch loss, a standard switch is firstly analyzed, then separate power loss is therefore summed to give the overall switch loss of these inverters. For evaluating the isolated switch loss, current linear function & voltage linear function are utilized throughout the transient cycle (transit as OFF mode to ON mode & conversely). Power loss at start-up may be computed like

$$E_{on,j} = \int_0^{t_{on}} V(t) i(t) dt \quad (12)$$

$$\int_0^{t_{on}} \left[ \left\{ V_{o,j} \frac{t}{t_{on}} \right\} \left\{ -\frac{I}{t_{on}} (t - t_{on}) \right\} \right] dt \quad (13)$$

$$\frac{1}{6} V_{o,j} I t_{on} \quad (14)$$

where,  $E_{on,j} = j^{th}$  switch loss of turn-ON,  $t_{on} =$  time for turn-ON,  $I =$  when switching upon that switch, electric current flows through all of it,  $V_{o,j} =$  voltage that must be blocked by the  $j^{th}$  switch Likewise, the  $j^{th}$  switch's energy dissipation when turned off may be computed as

$$\int_0^{t_{off}} v(t) i(t) = \int_0^{t_{off}} \left[ \left\{ V_{o,j} \frac{t}{t_{off}} \right\} \left\{ -\frac{I}{t_{off}}(t - t_{off}) \right\} \right] \tag{15}$$

$$= \left( \frac{1}{N} \right) V_{o,j} * I * t_{off} \tag{16}$$

where  $t_{off}$  is the time it takes for the  $j^{th}$  switches to turn it off, and  $I$  indicate the current that flows using switches before this turns off?

The  $j^{th}$  switch performs  $f_j$  changes in 1 s, wherein  $f_j$  would be its carrier frequency. As a result, given  $I = I$ , the total switch power loss may be estimated as follows:

$$\tau_s = \sum_{j=1}^{2n+2} \left[ \frac{1}{10} V_{o,j} I (t_{on} + t_{off}) f_j \right] \tag{17}$$

The next Section V (14) can be used to demonstrate that such a topology has reduced switch loss to the traditional CHB design. The overall inverter loss may now be calculated by Eqs. (11) and (14) as functions.

$$\rho_{losses} = \rho_{c,avg} + \rho_s \tag{18}$$

### 5 Component Requirements

In this section, the presented topology has been compared in the manner of component requirement with the existing traditional topology such as NPC, CHB, and FC-MLI; as per the above discussion, seen that proposed MLI is the family of CHB multilevel inverter, proposed converter has four symmetrical input dc voltage, 10 IGBT switches producing stepped output with 1.07% THD without any type filter as shown in Figs. 10 and 12, in this category circuit has lowest THD profile with lower component count moreover level can be further increased by increasing number of cell or using asymmetrical DC voltage source. Table 3 shows a comparison of component needs for this proposed topology concerning the number of DC input sources for a single-phase 9-level arrangement. The table indicated that the number of components throughout this architecture is lower than that of other architecture, specifically for a greater level of voltage. Furthermore, the overall voltage load carried by the primary switches and diodes throughout this design is almost the same as conventional topologies.

**Table 3:** Component require for 1-Phases multilevel inverters ( $L_{nis}$  Levels Number in the Phase Voltage) [63]

Type of inverters	NPC	FC	Cascaded H-bridge	Used symmetrical DC voltage topology
No. of main switch	$6(L_n - 1)$	$6(L_n - 1)$	$6(L_n - 1)$	$(L_n + 1)$
No. of main diodes	$6(L_n - 1)$	$6(L_n - 1)$	$6(L_n - 1)$	$(L_n + 1)$
No. of (DC) diode clamping	$3(L_n - 1)$ $(L_n - 2)$	0	0	0

(Continued)

**Table 3 (continued)**

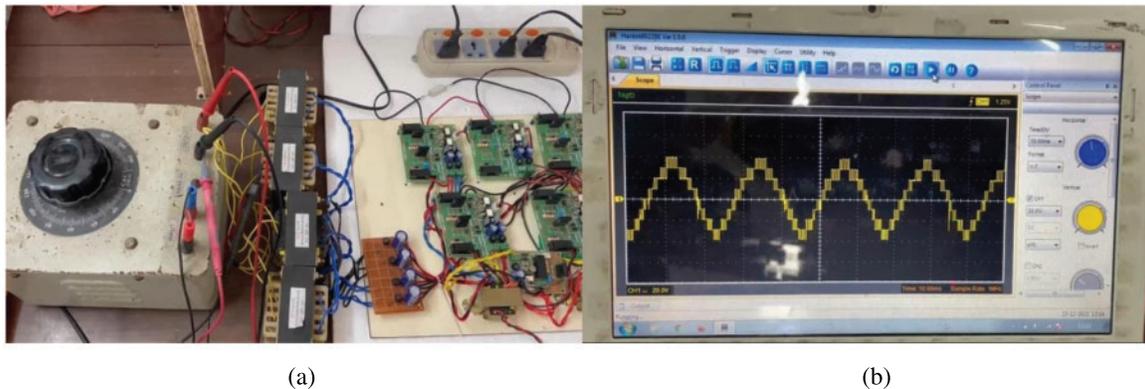
Type of inverters	NPC	FC	Cascaded H-bridge	Used symmetrical DC voltage topology
Isolated supply	$(L_n - 1)$	$(L_n - 1)$	$3(L_n - 1)/2$	$(L_n - 1)/2$
No. of FC (flying capacitor)	0	$(3/2)(L_n - 1)$ $(L_n - 2)$	0	0
Aggregate components count	$(L_n - 1)$ $(3L_n + 7)$	$(1/2)(L_n - 1)$ $(3L_n + 20)$	$(27/2)(L_n - 1)$	$(2 * L_n + 2)$

## 6 Experimental Results

As stated earlier, for elaborated symmetric dc voltage source utilized in 9-level multi-cell MLI trade-off must be made among no. of power switch & standing voltage on power switches. Also, it has been presented that the number of switches = 10 can be a great choice when it balances the counting of power switches & standing voltage on switches. Thus, experimental & simulation results are stated for the condition in which the number of switches  $n = 10$ . It is considered that two sub-multi cells are connected to each other. Consequently, the output of symmetric MLI depends upon the presented optimal device topology will be as demonstrated in Figs. 13a and 13b. This 9-level multi-cell MLI has four equal sources of DC voltage, leading to a 9-level multi-cell MLI. Amplitude of sources is  $E_1 = E_2 = E_3 = E_4 = 40$  V & so peak of load voltage is 160 V. A series-connected (R–L) load with resistance & inductance of 82 mH & 60 is paired to output. 9-level MLI dependent upon presented topology (Figs. 13a and 13b) utilizes 10 power switch (IGBTs).

In order to optimize the 9-level multi-cell, MLI staircase methodology is preferred. In this method, at any given point in time, the chosen level is the one closest to the reference output voltage. This process is also known as the nearest level approach. Using this technique, the output staircase voltage has the least inaccuracy concerning the reference voltage. Fig. 13a displays the prototype model. The prototype model has many circuits, each of which consists of IGBT power switch and a gate driver circuit for controlling the IGBT power switch gate. In addition to connection points for connecting the power circuit through wires and controller signals, the boards also provide connection points for the power circuit. Each board has its own power supply, which is used by a multi-tap-controlled power source. Also processed onboard are the rectifiers. In this design, MOSFET (IRF460) power switches (IGBTs) with internal anti-parallel diodes are employed. Each switch (GBT) is equipped with a gate driver circuit.

Gate firing signals of IGBT's power switches are generated using the TMS320F28 Development kit. The microcontroller produced the gate firing pulses as per the table and connected it for gate driver topology, which drives power switches. As DC sources, the lab's existing source voltage has been used. Figs. 13a and 13b depict the simulated and experimental output voltage findings, respectively. As indicated in the figures above, 9-level multicell MLI generates all anticipated voltage levels, resulting in a 9-level staircase output voltage. Output waveforms and their total harmonic profile seem to be in close accord with the getting of the corresponding simulations. The output AC load voltage is a stepped staircase waveform with levels of symmetrical magnitude. It's also very important to note that power balance amongst input dc supplies is required with all dc sources to be having an equivalent lifespan. So, when dc sources, like PV cells, power rebalancing is especially critical.



**Figure 13:** (a) Experimental setup (b) Experimental output voltage

## 7 Conclusion

This work presents a revolutionary architecture for MLIs to minimize the power switches and decrease their THD profiles. This topology's operating principles have already been discussed, and mathematical formulas for o/p voltage and source current flow. This topology produces staircase results using different input DC voltage sources, which has the lowest THD profile, 1.07%, with a lower no. of switches count compared with the existing MLI topology; simulating experiments were carried out on a 9-level MLI with symmetrical DC voltage supply; when deploying asymmetric DC voltage source, the same circuit will produce 31 level output with some changes in firing scheme. This topology is best to apply where a separate DC Supply is needed, such solar photovoltaic system. MATLAB Simulink was used to test this design.

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