

Computerised Gate Firing Control for 17-Level MLI using Staircase PWM

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Abstract: A basic 7-level MLI topology is developed and the same is extended to the 9-level then further increased to 17-levels. The developed structure minimizes the component's count and size to draw out the system economy. Despite the various advantages of MLIs, efficiency and reliability play a major role since the usage of components is higher for getting a low Total Harmonics Distortion (THD) value. This becomes a major challenge incorporated in boosting the efficiency without affecting the THD value. Various parametric observations are done and realized for the designed 9-level and 17-level MLI, being the Total Standing Voltage (TSV), efficiency, cost function per level count, and power loss. The respective parameters are compared with several existing and modern circuits and found to be effective in their performance. A novel single-phase 17-level asymmetrical Multi-Level Inverter (MLI) topology is developed to reduce the number of overall components. The developed topology generates 17-levels by using unequal DC sources. The developed MLI is proved under various tests conducted experimentally for the various loads like resistive, inductive, and combinational loads. A detailed comparison is done on several factors and represented graphically represented. Further, the proposed design provides a less TSV value is $6 V_{dc}$, efficiency is 94.21% and cost factor per level CF/L value for both values of α is 2.01 and 2.05 and devices count with a low THD value 41.4% with respectively.

Keywords: Inverters; 9-level and 17-level MLI; switches count; load current; voltages; round-robin staircase PWM

1 Introduction

The multilevel inverter has grown in popularity in recent years due to several advantages, such as less harmonic content, fewer switching losses, and lower electromagnetic interferences [1]. Most commonly the demand for the MLIs is gradually increasing with the power conversion process i.e., from Direct Current (DC) - (AC) Alternating Current, DC-DC & AC-DC, and along with the applications like AC motor



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drives, active capacitive filters, electric vehicles, uninterrupted power supplies, etc. [2]. These types of MLIs provide a step voltage wave at the output and employ several DC sources with a power semiconductor interface, consisting of several switches [3]. Even though the traditional MLI topologies like Neutral point clamped (NPC), Flying capacitors (FC), and Cascaded H-bridge (CHB) are utilized at maximum in various industrial automated applications, still there are some disadvantages such as high device count in CHBs and unequal voltages in FC and NPC MLI topologies. The reliability of the NPC type of MLI has diminished due to the usage of diodes in the system [4].

The most demanding issues in operating the MLI are commonly the devices and switches count, balancing the capacitive voltages, TSV, employing the chance of incorporating asymmetric sources in the structure [5]. In the modern advanced technology, several MLI topologies are proposed concerning the combinations of several capacitors and DC sources concerning the various switching states. In [6], an advanced H-bridge MLI with various DC sources is presented. A 7-level MLI topology proposed in [7], utilizes 9 switches and 3 DC sources and tends to combine all DC levels at its voltage output. In [8], an MLI is introduced with eight switches making up the 7-level output and 3 DC sources having a cascaded structure that utilizes a half-bridge circuitry. Several modulation techniques are used in the MLI topologies, specifically the phase opposition and disposition technique is used in [9]. Novel 7-level MLI structure is proposed in [10] aims to reduce overall components like switches, sources, elements in the circuit and the A PI controller controls the current, which is not effective. The major disadvantage is that the modulation technique's complexity becomes high while the level count is raised, [11,12]. Further, the levels of MLI get increased to have more advantages related to reliability and efficiency. The topology presented in [13] is a 9-level MLI, consists of twelve switches, and the various units are cascaded in [14]. The author in [15] presented a 9-level MLI consisting of two capacitors and one DC source. An asymmetrical 17-level MLI topology is designed from the basic 7-level and 9-level MLI structures. Hence, both 9 and 17-level MLIs are accomplished in detail along their outcomes are observed to be advantageous when correlated with various conventional and modern topologies. The major advantages of the proposed structure involve the rapid increase in its output levels with lesser devices count. The TSV shows the peak voltage which is blocking at the switches and is obtained. However, the cost-function and cost-function per level count values are calculated based on the TSV value. Efficiency calculations along with power losses are calculated in detail, these extracted outcomes are compared in detail along with the several modern topologies. Experimental efficiency is calculated and compared with the simulation results. A developed MLI is cost-effective since it uses a low TSV value and has a high-efficiency value. Comparison is made between the respective power losses and efficiencies for all loads. The THD value is following IEEE standards. The developed topology is applied to applications like active filters, UPS, renewable energy sources, and FACTS. In this paper, a 17-level switched diode MLI is precisely tested under numerous loads including resistive, inductive, and combinational loads including both resistive and inductive loads. The challenges and practical recommendations for developing an efficient system were highlighted. In order to motivate and guide society to focus on developing an efficient and cost-effective multi-level inverter associated scheme that combines most of the used and reported inverters' capabilities.

The information of the paper is laid out as follows: the basic 7-level and the developed 9 and 17-level MLIs are analyzed in section-II, section-III represents the validations of simulation and experimental outcomes. Several calculations like efficiency, TSV, cost factor, power loss, and various précised comparisons along with the existing structures are represented in segment IV. Lastly, the respective conclusions along with the future work are shown in segment V.

2 Literature Review

A modified topology is proposed in [16] with 7 switches and 2 capacitors, where it is essential to have two DC sources. To overcome the disadvantages, a compact switched-capacitor-based MLI is proposed [17] with reduced devices count. Several asymmetrical MLI topologies with various levels are proposed in [18–23] consists of high total standing voltage and THD. The MLI proposed in [24] consists of a high device count employing a heavy circuit with more THD employing less efficiency. The respective drawbacks are compensated among the topologies proposed in [25–27]. An asymmetrical type of topology is proposed in [28,29], where the respective DC links are continuously placed with their adverse polarities concerning the switches. An asymmetrical MLI proposed in [30], which is utilized in dynamic voltage restorer application. A 17-level asymmetric type MLI topology is proposed in [31], a square type representing a T-shape topology. A modified T-type topology is presented in [32], which utilizes two extra switches, and to provide 13-levels, the respective DC sources get reduced by altering the two capacitors. This type of topology with the absence of an H-bridge is proposed in [33] to provide higher levels of output consisting of ten unidirectional and two bi-directional switches. In [34], a cascaded topology with symmetric configuration is proposed, where the less total standing voltage is obtained and even extended to an advanced h-type topology utilized for symmetric and asymmetric configurations. The topology presented in [35], is well suited for high and low switching frequencies, which is a higher-level inverter configuration. Despite these topologies, several topologies are presented in [36–38] aim for the reduced switches and minimized devices count and voltage stress on the stress for the power switches.

3 Proposed MLI Structures

Several modulation techniques are used in the MLI topologies, specifically the phase opposition and disposition technique, and the different types of topologies are as follows,

3.1 Proposed 9-Level MLI Topology

To develop a 9-level MLI, the seven-level inverter topology is enhanced with an addition of one extra DC excitation, and two switches. The developed 9-level MLI consists of eight unidirectional types of switches S_1 to S_8 and three DC excitations V_1 , V_2 , and V_3 represented in Fig. 1. The magnitude of voltage for all the sources has opted with various values where the topology is to be termed as asymmetrical type. The DC excitations are selected concerning the ratio of 1:2:1, which are $V_{dc} = V_1 = 100$ V, $V_2 = 200$ V and $V_3 = 100$ V. The switching table for 9-level MLI is represented in Tab. 2. The operation of the 9-level MLI is employed from the respective pulses provided by the switches. For the generation of pulses, the modulation technique used is round-robin staircase type, whereas the activation of the switches is with a symbol '\(\surd\)', where the switch is turned ON. In other states, the switch becomes turned OFF. The operating modes are represented in Tab. 1, whereas the path of load current is I_o . An expected output waveform and several operating modes are denoted in Fig. 2.

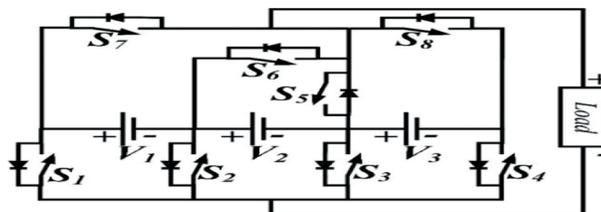


Figure 1: 9-Level asymmetrical MLI structure

Table 1: Modes of operation for the 9-level MLI

Modes	The direction of load current	Sources	V_0 (volt)
M ₁	V ₁ -S ₇ -L-S ₄ -V ₃ -V ₂ -V ₁	V ₁ +V ₂ +V ₃	400
M ₂	V ₁ -S ₇ -L-S ₃ -V ₂ -V ₁	V ₁ +V ₂	300
	V ₂ -S ₆ -L-S ₄ -V ₃ -V ₂	V ₂ +V ₃	
M ₃	V ₂ -S ₆ -L-S ₃ -V ₂	V ₂	200
M ₄	V ₁ -S ₄ -L-S ₂ -V ₁	V ₁	100
	V ₃ -S ₅ -L-S ₄ -V ₃	V ₃	
M ₅	L-S ₃ -S ₅ -L	–	0
	L-S ₂ -S ₆ -L		
	L-S ₄ -S ₈ -L		
	L-S ₁ -S ₇ -L		
M ₆	V ₁ -S ₁ -L-S ₆ -V ₁	-V ₁	-100
	V ₃ -S ₃ -L-S ₈ -V ₃	-V ₃	
M ₇	V ₂ -S ₂ -L-S ₅ -V ₂	-V ₂	-200
M ₈	V ₁ -S ₁ -L-S ₅ -V ₂ -V ₁	-(V ₁ +V ₂)	-300
	V ₂ -S ₂ -L-S ₈ -V ₃ -V ₂	-(V ₂ +V ₃)	
M ₉	V ₁ -S ₁ -L-S ₈ -V ₃ -V ₂ -V ₁	-(V ₁ +V ₂ +V ₃)	-400

Table 2: Switching states of the 9- level Inverter

Levels	Conducting Switches								Sources			V_0
	S ₁	S ₂	S ₃	S ₄	S ₅	S ₆	S ₇	S ₈	V ₁	V ₂	V ₃	
L ₁				√			√		√	√	√	+4 V _{dc}
L ₂			√				√		√	√		+3 V _{dc}
				√		√				√	√	
L ₃			√			√				√		+2 V _{dc}
L ₄		√					√		√			+1 V _{dc}
				√	√						√	
L ₅		√				√			–			0 V _{dc}
				√				√				
	√						√					
L ₆	√					√			√			-1 V _{dc}
			√					√			√	
L ₇		√			√					√		-2 V _{dc}
L ₈	√				√				√	√		-3 V _{dc}
		√						√		√	√	
L ₉	√							√	√	√	√	-4 V _{dc}

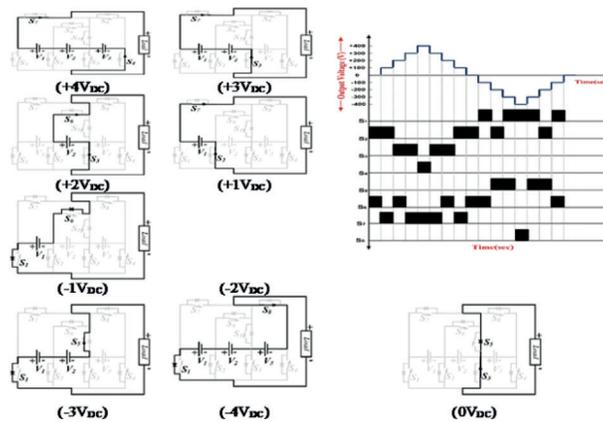


Figure 2: Operating modes and expected output waveform of nine-level MLI topology

Let ‘p’ be the fundamental units’ count, where P is only one unit

The number of switches N_{SW} is evaluated as Eq. (1)

$$N_{sw} = 8p \tag{1}$$

Number of DC sources N_{DCS} is evaluated as Eq. (2)

$$N_{DCS} = 3p \tag{2}$$

Levels count N_{LEL} is evaluated as Eq. (3)

$$N_{LEL} = 2(4^p) + 1 \tag{3}$$

N_{SW} is 8, which is the number of switches, N_{DCS} is 3, DC excitations count and the levels count is N_{LEL} is 9. In mode 1 operation, the switches S_4 , and S_7 conducts and the respective load current I_o follows over V_1 - S_7 -L- S_4 - V_3 - V_2 - V_1 , all three sources V_1 , V_2 , and V_3 excites the network and produces a voltage of $+4 V_{dc}$. In the operation of mode 7, the switches S_2 , and S_5 conduct and the respective load current I_o path of V_2 - S_2 -L- S_5 - V_2 , where the source V_2 excites the network and produces a voltage of $-2 V_{dc}$. In the operation of mode 8, the switches S_2 , and S_8 conducts and the respective load current I_o follows the path V_2 - S_2 -L- S_8 - V_3 - V_2 , where the sources V_1 and V_2 excites the network and produces a voltage of $-3 V_{dc}$. In the operation of mode 9, the switches S_1 , and S_8 conducts and the load current I_o follows the path over V_1 - S_1 -L- S_8 - V_3 - V_2 - V_1 , where all three sources V_1 , V_2 , and V_3 excite the network and produces a voltage of $-4 V_{dc}$.

The 9-level structure is precisely incorporated for addressing various issues that affect the quality of power such as a THD, to have a lesser switches count, the reduced voltage stress on the components i.e., dv/dt stress these features are further enhanced to generate a higher number of levels with fewer switches count, the developed 9-level MLI topology helps in achieving this scenario with less switch count. The simulation output waveforms regarding voltage and currents are represented in Figs. 5 and 6. It is found that the simulation and experimental THD are the same and are represented in Figs. 7 and 10. The developed MLI is experimentally tested in a hardware prototype represented in Fig. 10.

‘√’ indicates the conducting switch

3.2 Proposed 17- Level MLI Topology

To develop a 17-level MLI, the nine-level inverter topology is enhanced with an addition of one extra DC excitation, and two switches count. The developed 17-level MLI contains ten unidirectional types of switches S_1 to S_{10} and four DC excitations V_1 , V_2 , V_3 , and V_4 represented in Fig. 3. Voltages for all the sources have opted with various values; hence, the developed topology is to be termed asymmetrical. The DC excitations are selected concerning the ratio of 1:2:4:1, which are $V_{dc} = V_1 = 50$ V, $V_2 = 100$ V, $V_3 = 200$ V, and $V_4 = 50$ V. The switching states for 17 level inverter is represented in Tab. 3.

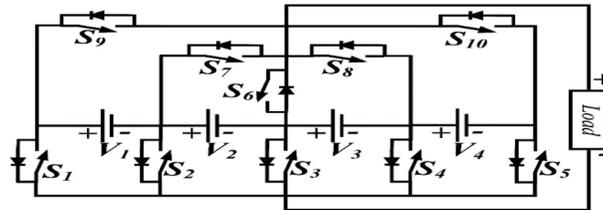


Figure 3: Proposed asymmetrical 17-level MLI topology

N_{SW} is 10, which is the number of switches, N_{DCS} is 4, the DC excitations count and N_{LEL} is 17, the number of levels. In the operation of mode 1, the switches S_5 , and S_9 conducts and the respective load current I_o follows the path V_1 - S_9 -L- S_5 - V_4 - V_3 - V_2 - V_1 , where the four sources V_1 , V_2 , V_3 , and V_4 excite the network and produces a voltage of $+8 V_{dc}$. In the operation of mode 2, the switches S_4 , and S_9 conducts and the respective load current I_o follows the path V_1 - S_9 -L- S_4 - V_3 - V_2 - V_1 , where the sources V_1 , V_2 , and V_3 excite the network and produces a voltage of $+7 V_{dc}$. In the operation of mode 3, the switches S_4 , and S_7 conducts and the respective load current I_o follows the path V_2 - S_7 -L- S_4 - V_3 - V_2 , where the sources V_2 , and V_3 excite the network and produces a voltage of $+6 V_{dc}$. In the operation of mode 4, the switches S_5 , and S_6 conducts and the respective load current I_o follows the path V_3 - S_6 -L- S_5 - V_4 - V_3 , where the sources V_3 and V_4 excite the network and produces a voltage of $+5 V_{dc}$. In the operation of mode 5, the switches S_4 , and S_6 conducts and the respective load current I_o follows the path V_3 - S_6 -L- S_4 - V_3 the source V_3 excite the network and produces a voltage of $+4 V_{dc}$. In the operation of mode 6, the switches S_3 , and S_9 conducts and the respective load current I_o follows the path V_1 - S_9 -L- S_3 - V_2 - V_1 , where the sources V_1 and V_2 excite the network and produces a voltage of $+3 V_{dc}$. In the operation of mode 7, the switches S_3 , and S_7 conducts and the respective load current I_o follows the path V_2 - S_7 -L- S_3 - V_2 , where the source V_2 excite the network and produces a voltage of $+2 V_{dc}$. In the operation of mode 8, the switches S_2 , and S_9 conducts and the respective load current I_o follows the path V_1 - S_9 -L- S_2 - V_1 , where the source V_1 excite the network and produces a voltage of $+1 V_{dc}$. In the operation of mode 9, the switches S_1 , and S_9 conducts and the respective load current I_o follows the path L- S_1 - S_9 -L, where the excitation is absent in this scenario and generates a voltage of is $0 V_{dc}$.

The 17-level MLI operation is employed from the pulses provided by switches. For the generation of pulses, the modulation technique used is round-robin staircase type, whereas the activation of the switches is with a symbol ' \surd ', where the switch is turned ON. In other states, the switch becomes turned OFF. The respective operating modes of the 17-level MLI along with the load current path I_o whereas the switching states are represented in Tab. 3. The expected output waveform and several operating modes of the proposed 17-level structure are exposed in Fig. 4.

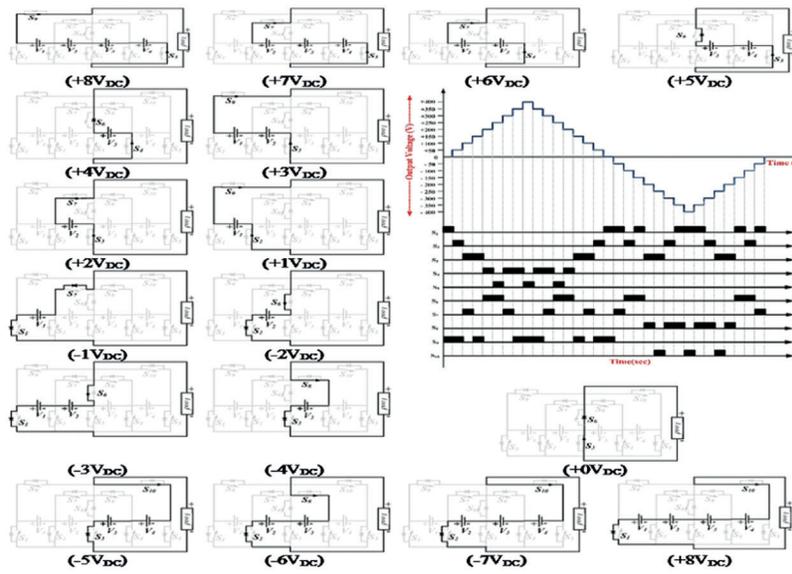


Figure 4: Operating modes and expected output waveform of seventeen level MLI topology

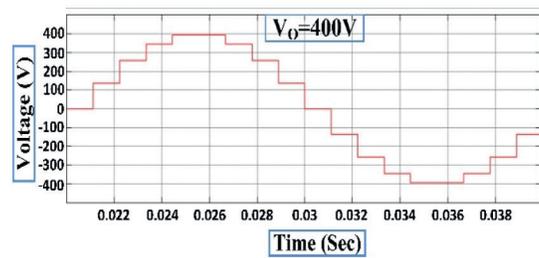


Figure 5: Simulation output voltage

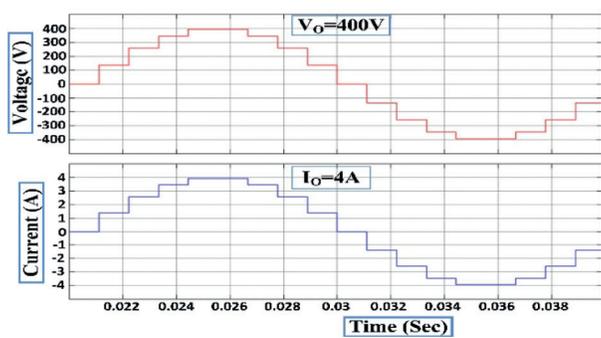


Figure 6: Simulation voltage and current waveform of 9-level MLI

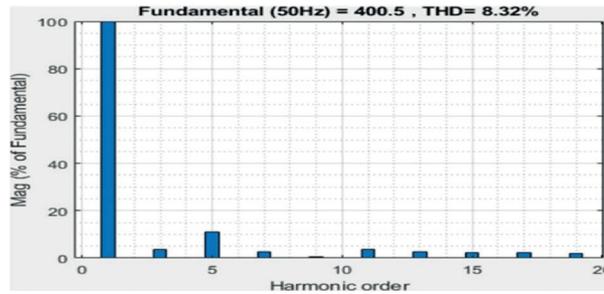


Figure 7: Simulation THD of 9 level MLI

Let ‘p’ be the fundamental units’ count, where P is only one unit

The number of switches N_{sw} is evaluated as Eq. (4)

$$N_{sw} = 10p \quad (4)$$

Several DC sources N_{DCS} is evaluated as Eq. (5)

$$N_{DCS} = 4p \quad (5)$$

Levels count N_{LEL} is evaluated as Eq. (6)

$$N_{LEL} = 2(8^p) + 1 \quad (6)$$

Table 3: Switching states of the 17- level inverter

Modes	The direction of load current	Sources	V_0 (volt)
M_1	$V_1-S_9-L-S_5-V_4-V_3-V_2-V_1$	$V_1+V_2+V_3+V_4$	400
M_2	$V_1-S_9-L-S_4-V_3-V_2-V_1$	$V_1+V_2+V_3$	350
M_3	$V_2-S_7-L-S_4-V_3-V_2$	V_2+V_3	300
M_4	$V_3-S_6-L-S_5-V_4-V_3$	V_3+V_4	250
M_5	$V_3-S_6-L-S_4-V_3$	V_3	200
M_6	$V_1-S_9-L-S_3-V_2-V_1$	V_1+V_2	150
M_7	$V_2-S_7-L-S_3-V_2$	V_2	100
M_8	$V_1-S_9-L-S_2-V_1$	V_1	50
M_9	$V_4-S_8-L-S_5-V_4$	V_4	0
	$L-S_1-S_9-L$	–	
	$L-S_2-S_7-L$		
	$L-S_3-S_6-L$		
	$L-S_4-S_8-L$		
M_{10}	$L-S_5-S_{10}-L$		–50
	$V_4-S_4-L-S_{10}-V_4$	$-V_4$	
	$V_1-S_1-L-S_7-V_1$	$-V_1$	
M_{11}	$V_2-S_2-L-S_6-V_2$	$-V_2$	–100

(Continued)

Table 3 (continued)			
Modes	The direction of load current	Sources	V_o (volt)
M_{12}	$V_1-S_1-L-S_6-V_2-V_1$	$-(V_1+V_2)$	-150
M_{13}	$V_3-S_3-L-S_8-V_3$	$-V_3$	-200
M_{14}	$V_3-S_3-L-S_{10}-V_4-V_3$	$-(V_3+V_4)$	-250
M_{15}	$V_2-S_2-L-S_8-V_3-V_2$	$-(V_2+V_3)$	-300
M_{16}	$V_1-S_1-L-S_8-V_3-V_2-V_1$	$-(V_1+V_2+V_3)$	-350
M_{17}	$V_1-S_1-L-S_{10}-V_4-V_3-V_2-V_1$	$-(V_1+V_2+V_3+V_4)$	-400

In the operation of mode 10, the switches S_1 , and S_7 conducts and the respective load current I_o follows the path $V_1-S_1-L-S_7-V_1$, where the source V_1 excites the network and produces a voltage of $-1V_{dc}$. In the operation of mode 11, the switches S_2 , and S_6 conducts and the respective load current I_o follows the path $V_2-S_2-L-S_6-V_2$, where the source V_2 excites the network and produces a voltage of $-2 V_{dc}$. In the operation of mode 12, the switches S_1 , and S_6 conducts and the respective load current I_o follows the path $V_1-S_1-L-S_6-V_2-V_1$, where the sources V_1 , and V_2 excites the network and produces a voltage of $-3 V_{dc}$.

In the operation of mode 13, the switches S_3 , and S_8 conducts and the respective load current I_o follows the path $V_3-S_3-L-S_8-V_3$, where the source V_3 excites the network and produces a voltage of $-4 V_{dc}$. In the operation of mode 14, the diode D_2 and switches S_3 , and S_{10} conducts and the respective load current I_o follows the path $V_3-S_3-L-S_{10}-V_4-V_3$, where the sources V_3 , and V_4 excites the network and produces a voltage of $-5 V_{dc}$. In the operation of mode 15, the switches S_2 , and S_8 conducts and the respective load current I_o follows the path $V_2-S_2-L-S_8-V_3-V_2$, where the sources V_2 and V_3 excites the network and produces a voltage of $-6 V_{dc}$. In the operation of mode 16, the switches S_1 , and S_8 conducts and the respective load current I_o follows the path $V_1-S_1-L-S_8-V_3-V_2-V_1$, where the sources V_1 , V_2 , and V_3 excites the network and produces a voltage of $-7 V_{dc}$. In the operation of mode 17, the switches S_1 , and S_{10} conducts and the respective load current I_o follows the path $V_1-S_1-L-S_{10}-V_4-V_3-V_2-V_1$, where the sources V_1 , V_2 , V_3 , and V_4 excites the network and produces a voltage of $-8 V_{dc}$. The 17-level structure is precisely incorporated for addressing various issues that affect the quality of power such as a THD, to have a lesser switches count, the reduced voltage stress on the components i.e., dv/dt stress these features are further enhanced to produce a higher number of levels with fewer switches count, the developed 17-level MLI topology helps in achieving this scenario with less switch count. The simulation output waveforms regarding currents and voltage are represented in Fig. 14. An experimental output with R-load is exposed in Fig. 15. It appears that that the simulation and experimental THD are the same and are represented in Figs. 13 and 16. An experimental output current and a voltage waveform of 9 levels MLI is exposed in Figs. 8 and 9.

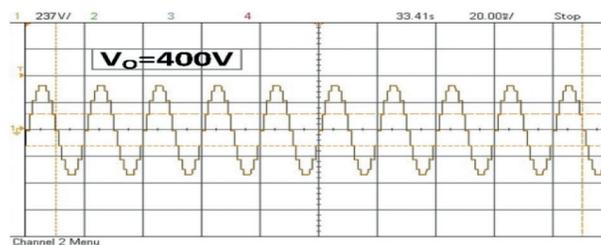


Figure 8: Experimental voltage waveform of 9-level MLI

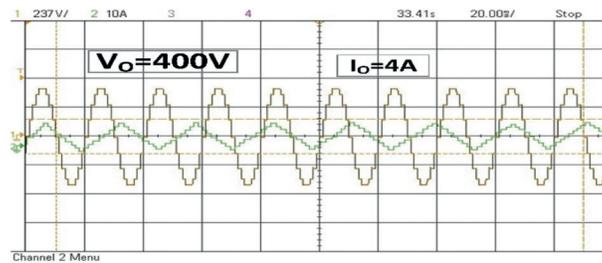


Figure 9: Experimental output voltage and current waveform of 9 level MLI

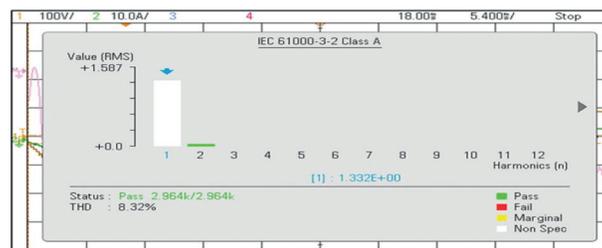


Figure 10: Experimental THD of 9-level MLI

4 Results and Discussions

The result and discussions of different levels of MLI are as follows,

4.1 9-Level MLI

A proposed simulation 9-level MLI structure is done in MATLAB/Simulink, whereas, a generation of switching pulses can be done at 2 kHz frequency and is related with a frequency of 50Hz, the structure is precisely tested for the resistive load of 100 Ω , the maximum voltage of 400 V is obtained via provide input DC sources $V_{dc} = V_1 = 100$ V, $V_2 = 200$ V, and $V_3 = 100$ V respectively. Figs. 8 and 9 represent an outcome of simulation results such as current and voltage waveforms of the developed 9-level MLI topology, respectively. From Fig. 5 and 6, it concludes that the maximum peak voltage is 400 V and the respective load current is 4 A.

A proposed asymmetrical topology of the 9-level MLI structure is proved experimentally using a setup in the laboratory shown in Fig. 10. An inverter modeled setup used CM75DU-12H IGBT which are fed with MCT2E optocouplers, three exists three unequal DC excitations with $V_1 = 100$ V, $V_2 = 200$ V, and $V_3 = 100$ V, 100 Ω R-load then the generation of pulses can be done from dSPACE RTI1104. The hardware prototype with R-Load under SteadyState output voltage $V_0 = 400$ V is 282.84 V_{rms} , load current $I_0 = 4$ A, which is 2.82 A I_{rms} the THD value measured is 8.32% by using with power analyzer and is voltage represented in Fig. 7.

4.2 17-Level MLI

A proposed simulation 17-level MLI structure is done in MATLAB/Simulink, whereas the generation of switching pulses can be done at 2 kHz frequency and is compared with a frequency of 50 Hz, the structure is precisely tested for the resistive load of 100 Ω , the maximum voltage of 400 V is obtained *via* providing input DC sources $V_{dc} = V_1 = 50$ V, $V_2 = 100$ V, $V_3 = 200$ V, and $V_4 = 50$ V respectively. Figs. 11 and 12 represent outcomes of simulation results such as Current and Voltage waveforms of the developed 17-level MLI topology, respectively. From Figs. 11 and 12, it is found that the maximum peak voltage is 400 V and the respective load current is 4 A. A simulation THD is shown in Fig. 13. The proposed asymmetrical

topology of the 17-level MLI structure is proved experimentally using a setup in the laboratory. The setup of inverter modeled using CM75DU-12H IGBT which are fed with MCT2E optocouplers, three exists four unequal DC excitations with $V_1 = 50\text{ V}$, $V_2 = 100\text{ V}$, $V_3 = 200\text{ V}$, and $V_4 = 50\text{ V}$, R-load with a value of $100\ \Omega$ and the generation of pulses can be done from dSPACE RTI1104. The hardware prototype with R-Load under SteadyState output voltage $V_0 = 400\text{ V}$ is $282.84\text{ V}_{\text{rms}}$, load current $I_0 = 4\text{ A}$ which is $2.82\text{ A}_{\text{rms}}$ for R-load and $V_0 = 400\text{ V}$ is $282.84\text{ V}_{\text{rms}}$, load current $I_0 = 6.8\text{ A}$ which is $4.8\text{ A}_{\text{rms}}$ for RL-load are shown in Figs. 14 & 15 respectively. The THD value measured is 4.14% by using a power analyzer and is represented in Fig. 16.

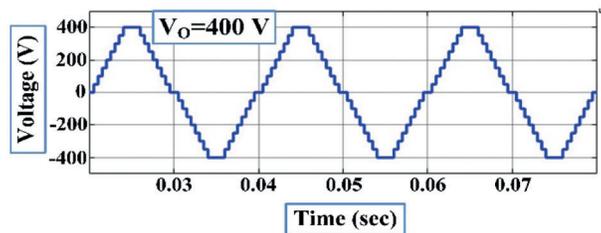


Figure 11: Simulation output voltage of 17 levels MLI

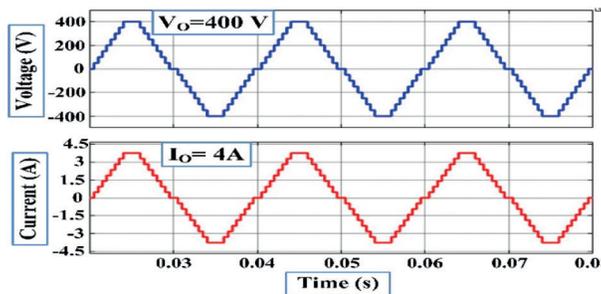


Figure 12: Simulation voltage & current waveform of 17 levels MLI

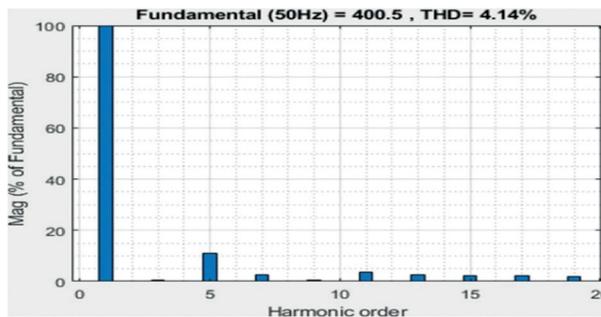


Figure 13: Simulation THD of 17 levels MLI

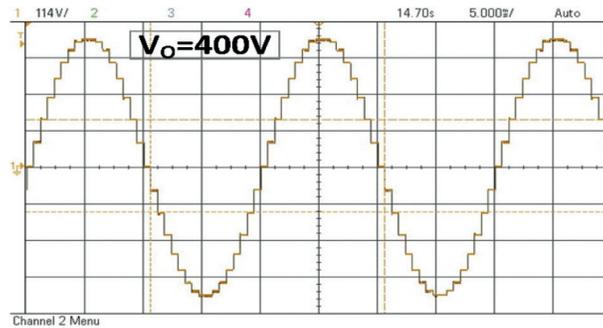


Figure 14: Experimental voltage waveform 17 levels MLI

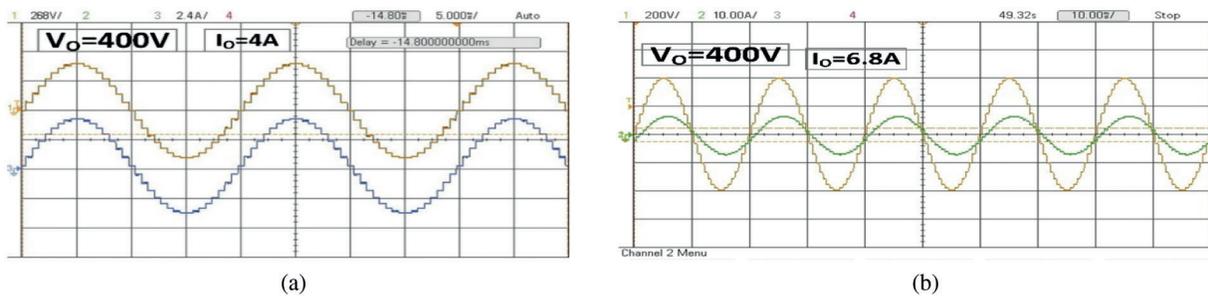


Figure 15: Experimental voltage and current waveform of 17 level MLI for (a) R-load (b) RL-load

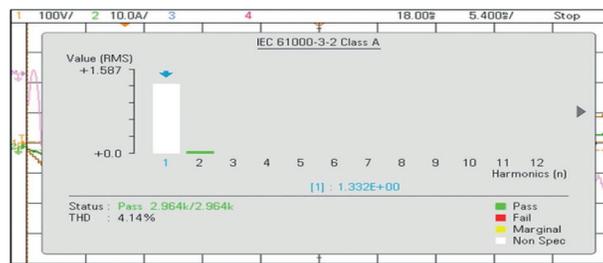


Figure 16: Experimental THD of 17 levels MLI

5 Calculations and Comparative Studies

The entire inefficiencies are categorized under two groups: conduction and switching losses, both of that are intimately tied toward the switching devices.

5.1 Losses and Efficiency

Conduction losses contribute a significant role in these losses anytime the switch is turned on at any time, hence conduction losses are calculated using the following formula. Eq. (7) and the overall MLI for efficiency and total power loss for the proposed 7, 9, and 17 levels MLI is tabulated in Tab. 4

$$P_{C_{ls}} = [V_S + R_S i^{\alpha}(t)]i(t) \tag{7}$$

where, V_S is the voltage across the IGBT switch. The resistance of the switch is represented as R_S .

Table 4: Efficiency and Power loss for the proposed 7, 9, and 17 levels MLI

Parameters	7 level	9 level	17 Level
Vrms (v)	282.84	282.84	282.84
Irms (A)	2.82	2.82	2.82
Conduction losses (W)	29.23	38.98	48.72
Switching losses (W)	0.052	0.091	0.223
Total losses (W)	29.282	39.071	48.943
Output power (W)	797.6	797.6	797.6
Efficiency (%)	96.45	95.33	94.21

The calculation of switching losses can be done using the following relation Eq. (8)

$$P_{Sl} = f \sum_{K=1}^{N_{switch}} \left[\sum_{j=1}^{N_{on,k}} E_{n_{on,kj}} + \sum_{j=1}^{N_{off,k}} E_{n_{off,kj}} \right] \tag{8}$$

where E_{on} and E_{off} are the utilized energies by the switches under conduction state.

The overall power losses ($P_{total\ loss}$) are calculated according to the following relation Eq. (9)

$$P_{totalloss} = P_{cl} + P_{sl} \tag{9}$$

Overall topology efficiency (η) can be determined used the following Eq. (10)

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{10}$$

where, P_{out} and P_{in} are the respective powers of output and input.

Respective output power can be determined using Eq. (11)

$$P_{out} = V_{rms} * I_{rms} \tag{11}$$

5.2 Total Standing Voltage (TSV)

A multilayer inverter's cumulative standing voltage is crucial in obtaining the greatest blocking voltage over the individual switches. It is an important issue to consider while choosing switches. To get the TSV value, all of the respective maximal blocking voltages over the switches are added together. The tension over the switch is represented by the amount of blocking voltage. A voltage stress changes depending on the switch type, including bi-directional and unidirectional switches. As a result, the voltage stress on bidirectional and unidirectional switches is determined: $V_{Sbi} = V_i$ and $V_{Suni} = 2 V_i$ respectively, where $i = 1, 2, 3, \dots, n$ number of complementary switches. Concerning the tertiary operating mode, the maximum output voltage ($V_{O, MAX}$) is

$$V_{0,max} = 400V$$

In the developed MLI, voltages are equal for the switches that are in the complementary design and here, all the switches are unidirectional. Therefore, TSV determined from the below equations:

For 9-level MLI.

$$TSV = V_{S1} + V_{S3} + V_{S5} + V_{S7} = 5V_{dc}$$

For 17-level MLI.

$$TSV = V_{S1} + V_{S3} + V_{S5} + V_{S7} = 6V_{dc}$$

The TSV per unit (TSV_{pu}) can be calculated by Eq. (12).

$$TSV_{PU} = \frac{V_{TSV}}{V_{OMAX}} \quad (12)$$

5.3 Cost Function (CF)

A cost function may be used to evaluate the economic assessments for the construction of MLI. A cost function for the proposed 9, and 17-level MLI may be calculated using several factors such as NSW, the number of switches, NDCS, the number of sources, ND, the number of diodes, ND, the number of capacitors, NC, TSV, NDK, the number of driver circuits, and the number of sources NSDC. As a result, the cost factor is calculated using the Eq. (13) and the formula below [39].

$$CF = (N_{SW} + N_{SDC} + N_{DK} + N_D + N_C + \alpha TSV_{PU}) \quad (13)$$

where ‘ α ’ is the weight coefficient. Generally, the value of α is greater than 1 and less than unity. In the proposed MLI, the value of α is analyzed as 0.5 (<1) and 1.5 (>1) for the optimal calculation of the cost factor. The MLI is found to be cost-effective based on the calculation of component level count (CF/L).

For 9 – level CF/level = 3.07 for $\alpha = 0.5$ and 3.21 for $\alpha = 1.5$

For 17 – level CF/level = 2.01 for $\alpha = 0.5$ and 2.05 for $\alpha = 1.5$

The total components utilized in the topology can be determined by using component level factor and is calculated using the Eq. (14).

$$F_{ccl} = \frac{N_{SW} + N_D + N_C + N_{DK} + N_{SDC}}{N_L} \quad (14)$$

5.4 Comparison Studies

A detailed comparison is done on various parameters used in the process of realization such as switches count N_{SW} , diodes count N_D , driver circuits count N_{DK} , capacitors count N_C , the total standing voltage per unit TSV_{PU} , voltage sources count N_{SDC} , components count factor CC/L with a cost function per level CF/L .

The 7-level structure compared with the existing and modern topologies is precisely done then tabulated in Tab. 5 and the respective graphical representations are represented in Fig. 17. Similarly, the respective comparisons of 9-level and 17-level MLI with several parameters are done and are compared with the traditional and modern topologies and are represented in Tab. 6 and Tab. 7 respectively, where the graphical representations are exposed in Figs. 18 and 19 respectively.

Overall performance of MLI proposed method in represented by Tab. 8. where the graphical representations are shown in Fig. 20 respectively.

Table 5: Comparison of various parameters for 7-level MLI

Components	CHB	NPC	FC	[40]	[18]	Proposed
N_s	12	12	12	12	10	6
N_d	12	12	12	15	10	6
N_{cap}	3	6	6	6	0	–
n	3	1	1	3	3	2
N_{dk}	12	12	12	12	10	10
F_{cc}	6	6.14	6.14	7.85	4.71	3.42

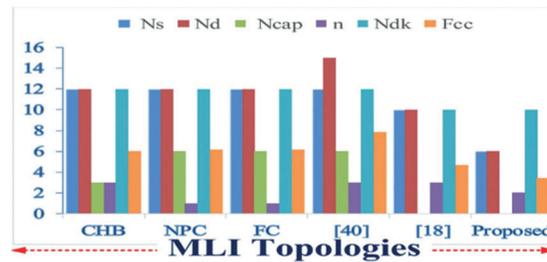


Figure 17: Comparison of parameter for 7-level MLI topology with existing topologies

Table 6: Comparison of cost with various parameters for 9-level MLI

Components required	CHB	NPC	FC	[3]	[13]	[15]	[16]	[41]	[42]	[43]	[44]	[45]	[46]	Proposed	
N_s	16	16	16	7	12	10	8	12	11	9	8	10	10	8	
N_d	16	16	16	8	12	10	8	12	11	11	8	10	10	8	
N_{cap}	0	8	8	2	4	2	2	2	2	0	2	0	2	–	
n	4	1	1	2	2	1	2	1	1	4	1	4	1	3	
N_{dk}	16	16	16	7	12	10	7	12	11	9	8	10	10	8	
F_{cc}	5.77	6.33	6.33	2.88	4.22	3.66	3	4.33	4	3.66	3.11	3.77	3.66	3	
TSV	16	16	16	5	1	–	9	–	11	11	10	16	24	5	
THD	–	–	–	8.7	–	19.4	9.30	–	–	–	–	8.0	–	8.32	
CF/ N_{Lev}	$\alpha = 0.5$	6.666	7.22	7.22	3.166	5.27	–	3.5	–	4.611	4.278	3.55	4.66	5	3.07
	$\alpha = 1.5$	8.44	9	9	3.722	6.5	–	4.833	–	5.833	5.5	4.66	6.44	7.66	3.21

Table 7: Comparison of cost with various parameters for 17-level MLI

Components required	CHB	NPC	FC	[3]	[15]	[16]	[41]	[43]	[45]	[47]	[48]	[49]	Proposed
N_s	32	32	32	14	20	16	24	14	20	10	10	10	10
N_d	32	32	32	16	20	16	24	20	20	10	10	12	10
N_{cap}	0	16	16	4	4	4	4	4	0	4	0	0	–
n	8	2	2	4	2	4	2	8	8	2	4	2	4

(Continued)

Components required		CHB	NPC	FC	[3]	[15]	[16]	[41]	[43]	[45]	[47]	[48]	[49]	Proposed
N_{dk}		32	32	32	14	20	14	24	14	20	20	10	10	10
Fcc		6.11	6.70	6.70	3.05	3.88	3.17	4.48	3.52	4	3.88	2	2	2
TSV		32	32	32	11	–	11	–	22	36	–	36	40	6
THD		–	–	–	4.23	–	–	–	–	3.7	–	7.1	–	4.14
CF/ N_{Lev}	$\alpha = 0.5$	7.05	7.64	7.64	3.38	–	3.5	–	4.17	5.05	–	4.94	5.18	2.01
	$\alpha = 1.5$	8.94	9.52	9.52	4.02	–	4.14	–	5.47	7.17	–	9.18	9.88	2.05

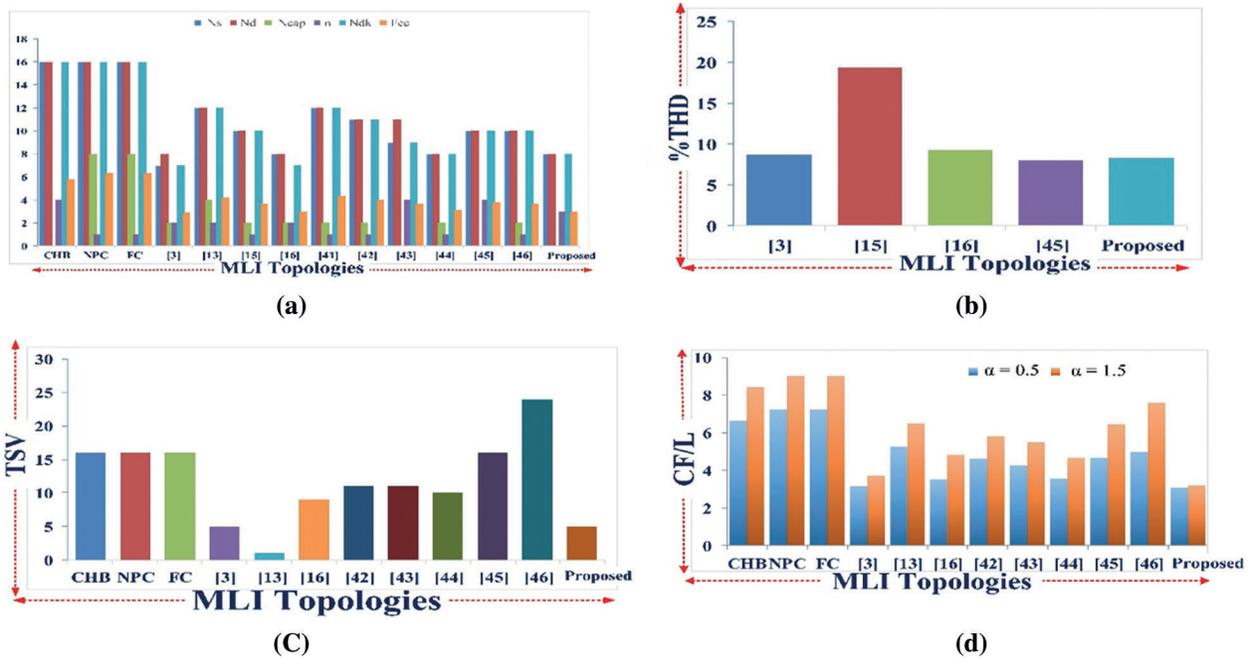


Figure 18: Comparison of parameters for 9-level MLI topology with (a) N_s , N_d , N_{cap} , n , N_{dk} , F_{cc} (b) %THD (c) TSV and (d) CF/L

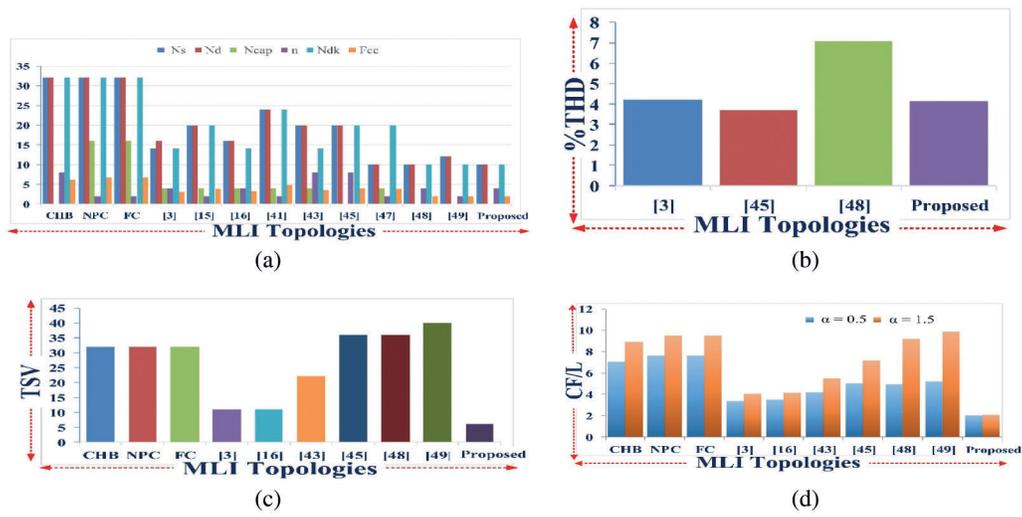


Figure 19: Comparison of parameters for 17-level MLI topology with (a) N_s , N_d , N_{cap} , n , N_{dk} , F_{cc} (b) % THD (c) TSV and (d) CF/L

Table 8: Overall performance of MLI

Components required	Proposed 9-level MLI	Proposed 17-level MLI
N_s	8	10
N_d	8	10
N_{cap}	—	—
n	3	4
N_{dk}	8	10
F_{cc}	3	2
TSV	5	6
THD	8.32	4.14
CF/ N_{Lev}	$\alpha = 0.5$	3.07
	$\alpha = 1.5$	3.21

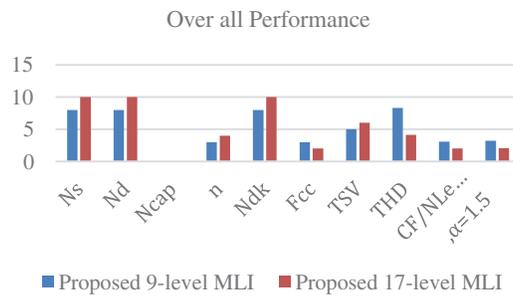


Figure 20: Overall Performance of MLI

6 Conclusion

A new asymmetrical 17-level MLI structure is established from the basic 7-level and 9-level MLI topologies. The basic 7-level MLI and 9-level MLI are realized with several parameters and further developed to 17-level MLI. The developed MLI consists of fewer components, due to which the size and cost of the inverter get compact. Therefore, the reliability and efficiency of the proposed MLI get improved. The MLI requires a lesser component to deliver expected output voltage levels with less THD. Also, the TSV and respective cost factor is calculated and found to be cost-effective. Various comparisons are made concerning the several parameters with various conventional and modern pre-existing topologies. The comparisons prove that a developed MLI is very much efficient and there exists less utilization of power. Also, it is observed that the results obtained in both simulation and experimental THD are the same and are 4.14%. The TSV is $6 V_{dc}$, efficiency is 94.21% and cost factor per level CF/L value for both values of α is 2.01 and 2.05 respectively, representing a developed MLI is cost-effective with all existing topologies. A developed MLI is verified with load variations with resistive load and inductive load and the combinational loads and found to be stable. Future scope of the proposed work can be obtained by improving the efficiency of the inverter by addition of further Level to 18 or 19.

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