

# Performance Analysis of AODV Routing for Wireless Sensor Network in FPGA Hardware

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Abstract: Wireless sensor network (WSN) is a group of interconnected sensor nodes that work wirelessly to capture the information of surroundings. The routing of the network is a challenging task. The routing of WSN is classified as proactive, reactive, and hybrid. Adhoc on-demand distance vector (AODV) routing is an example of reactive routing based on the demand route formations among different nodes in the network. The research article emphasizes the design and simulation of the AODV routing hardware chip using very-high-speed integrated circuit hardware description language (VHDL) programming in Xilinx integrated synthesis environment (ISE) 14.7 software. The performance of the chip is studied based on the field-programmable gate array (FPGA) hardware parameters such as slices, lookup table (LUTs), input/output block (IOB), flipflops, and memory for the different configurations of the network (N = 10, 20 ....100). The delay and frequency are also estimated on the Virtex-5 FPGA. The performance of the WSN with AODV routing is also analyzed based on the packet delivery ratio, throughput, delay, and control overhead. The simulation test cases verified the 8-bit, 64-bit, and 128-bit data communication within the nodes.

**Keywords:** Wireless sensor network; FPGA synthesis; AODV routing; simulation and synthesis; VHDL simulation

### **1** Introduction

The wireless sensor network is an infrastructure-less organized wireless network [1], used in a large space by deploying the wireless sensors in an ad-hoc way that can be used to monitor the physical, system, or environmental conditions. The WSN consist of several nodes with the onboard processor to manage and monitor the environmental conditions in a specific area. The nodes are connected to the main processing unit or the base station in the WSN System. The base station is connected to the internet to share the information among the nodes. The Components of WSN are sensors, radio nodes, wireless local



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area network (LAN) access points [2], and evaluation software. The sensor nodes capture the environmental parameters which can be used for data acquisition. The signals are converted to electrical signals. The radio nodes receive the information processed by the sensors and process it into the wireless LAN access points. It is a transceiver, power source, microcontroller-based system, or a memory element. The wireless LAN access points receive the data of radio nodes through the internet. The evaluation software process the data of wireless LAN access points. The software process the data to the destination and users for further monitoring, storage, analysis, processing, or mining. The sensor nodes are limited in computational capabilities, power, and memory.

The main challenges of the WSN are energy efficiency, performance, quality of service (QoS), scalability over large-scale deployment, node failure, routing, security, network throughput, cross-layer optimization, and capability to cope with node failure. The topology of a WSN changes very regularly. The major applications of WSN [3] are in monitoring environmental parameters such as temperature, air pressure, and humidity. Other applications are agriculture, landslide detection, weather forecasting, the internet of things (IoT), medical science as patient monitoring, security, and threat detection.

The routing protocol [4] is a method to choose the appropriate route for processing data from source to destination. The method meets numerous problems while deciding the route that probably depends on the channel characteristics, type of network, and WSN performance metrics. The sensors forward the sensed data to the base station and connect the sensor networks to the specific network using the internet in which the data is gathered, analyzed, and processed accordingly in WSN. The design work routing methods for WSN are relatively thought because of several characteristics of the network that distinguish them from wireless infrastructure-less networks. Different types of routing concerns are involved in WSN.

Most of the time it is difficult to allocate a common identification method for a large-scale network in which multiple sensor nodes are working together. Therefore, wireless sensor nodes are not capable of using conventional IP-based protocols. The data flow of the detected node is necessary from a large number of sources to a definite base station. It is not occurring in the usual communication networks. The traffic packets have substantial redundancy in all of the cases. The reason is that multiple nodes can create the same data while sensing the environmental parameters. Therefore, it is required to exploit the cause of such redundancy with the help of routing protocols and make them feasible to utilize more bandwidth and efficient energy as required. Furthermore, the nodes are firmly limited in the relations of transmission energy, capacity, storage, bandwidth, and onboard energy. Due to such differences, several new routing protocols are to manage the routing issue and challenges in WSNs.

The routing protocols of WSNs are categorized as network structure-oriented protocols (Flat, location, and Hierarchical), route dispensation protocols (reactive, proactive, and hierarchical), and network operations-oriented protocols (Queue based, multipath, coherent, QoS, and negotiation). The reactive protocols are activated based on the demand and do not follow the exact network topology. The route is created based on the demand raised by the node when a source node wishes to send the packets to the destination. The commonly used reactive protocols are dynamic state routing (DSR) and Ad-hoc on-demand distance vector routing system (AODV). On the other hand, the proactive protocols are table-oriented and keep a routing table when data packets are transferred from the source node to the destination node. The generally used proactive protocols are optimized link state routing (OLSR) and destination sequenced distance vector (DSDV) protocol [5]. Moreover, the hybrid routing protocol (HRP) is having the quality of proactive routing and reactive routing. These protocols are applied to choose the path for optimum network solutions and the data transfer requirements for the state of network topology. The behavior of routing protocols depends on the network performance matrices which are

*Packet delivery ratio (PDR)* - It is a ratio of the number of packets received by destination to the number of the packet sent by the source.

*End to end Delay (EoD)* - End to end delay (seconds) is the time it takes a data packet to reach the destination. In the network layer, the end-to-end delay is calculated by the sum of processing delay, transmission delay, packet, propagation delay, and queuing delay. The end-to-end delay is estimated as the sum of the node delay at each node and the link delay on each link in the path.

*Routing Overhead (RH)* - Routing overhead is the total number of routing packets divided by the total number of delivered data packets.

RH= Full number of routing packets/Full number of packets delivered.

*Throughput* - The rate of successfully transmitted data per second in the network during the simulation. It is a measure of the date rate (bits per second) experienced in the network.

#### 2 Related Work

The performance of the WSN [6] depends on the three major parameters throughput, packet delivery ratio, and energy levels. WSN faces the issue of jamming and quick battery energy depletion. The authors worked on the sensor mechanism used for rechargeable WSNs, in which anchor points are moved along with the intended trajectory and recharge the placed sensors using wireless power transmissions. WSN has different security concerns and algorithms for WSN. The WSN system and more vulnerable to attacks [7]. Therefore, security systems are primarily required to secure the network and confirm the network security threats. Cryptography plays a very important role and leading protocols are used to address the security concerns in WSN. They discussed different protocols such as security protocols for sensor networks (SPIN), low entropy authentication (LEA), regular and predictable times (RPT), tiny security, lightweight mutual authentication, etc protocols for WSN security. Several routing methods are applicable for data transmission in WSN. They mainly considered the widespread methods AODV and (DSR) [8]. To compare the performance based on the calculation of, throughputs packet delivery ratio, and end to end delay. They used a network simulator version-2 (NS2) software simulation to evaluate the performance of the system. AODV is much better than DSR in terms of packet delivery ratio and DSR is much better than AODV in terms of throughput. The comparative analysis of AODV and DSDV protocols [9] in terms of packet delivery ratio, routing overhead, end-to-end delay, and throughput. It had been analyzed that AODV is better than DSDV in terms of packet delivery ratio, throughput, and routing overhead. The DSDV is a proactive routing protocol and having an optimal end-to-end delay in comparison to AODV. The energy responsive green cluster-based routing system [10] is used to avoid the early death of large-scale dense WSNs. In clustered-based networks, clustering forms inadequate load distribution from cluster heads and cluster member nodes. They focused on the fuzzy rule-based method to classify the clustering approach. The main advantage of the method is in the selection of effective cluster heads and their distribution among other nodes so that it can prevent the overhead in large dense areas. The suggested routing method balances the traffic load among all sensors. The most suited routing protocols for WSN [11] are AODV, Bellman-Ford, OLSR, and dynamic mobile Adhoc network ondemand routing. The performance of these protocols depends on the parameters such as average end-toend delay, average throughput, and average energy consumption. The simulation work proved that routing is best among all in terms of end-to-end delay, throughput, and energy consumption. The routing protocols of WLAN are reactive [12] and proactive. In the network of 40 nodes, it is estimated the OLSR provides a minimum delay in comparison to AODV and DSR. DSR provides the highest value of presented throughput. WSN sensor and device should have optimal energy consumption [13] and fast operating speed. The network should be designed in such a manner that it can maintain network lifetime, enhance network capacity, and optimize delay. So, the designer should decide the simulation platform in which all constraints can meet. They introduced the CASTALIA simulation software that works on the objective modular network testbed in C++(OMNeT++) platform for the low-power sensor devices in

WSN. The WSN nodes follow the tier-based energy efficient (TBEE) protocol [14] and cluster-based energyefficient (CBEEP). In TBEE protocol, all nodes are distributed into three areas based on their distance from the base station, usually identified as tires. Energy is divided homogeneously among all sensor nodes in the network and a minimum spanning tree is formed. A head node is decided from each tier group that has the maximum energy to send the sensed data to the base station. In the CBEEP protocol, the full function device (FFD) is the cluster head and sends data to the base station. Both protocols are much helpful for the calculation of the lifetime and energy consumption in the network. The routing algorithm is maximizing based on the quality [15] of WSN. Authors compared the network based on different algorithms such as AODV, Genetic algorithm (GA) based AODV, Dijkstra algorithm, and GA based Dijkstra algorithm. The concept of faulty nodes is also considered that 50% of nodes may be faulty among dynamic functioning nodes. The GA has proved the better performance in WSN when embedded with the algorithm. The energyefficient clustering protocol (EECP) can be applied for heterogeneous wireless sensor networks (HWSN) [16]. The suggested protocol is designed with three types of nodes and their communication namely general, advanced, and excellent, respectively. The protocol improved, lifetime, stability, throughput, and energy of the network. The algorithm outperforms other than other protocols. The WSN nodes are based on internet protocol version 4 (IPv4) addressing [17] in the AODV protocol. The work was carried for 50, 100, 150, 200, and 250 nodes with a simulation time of 10 minutes. It was based on used for battery charge monitoring model for 60 seconds using 1200 mill ampere-hour (m.A.h) battery. In this way, the behavior of WSN and AODV is justified for transport and physical layer applications in WSN. The WSN protocols [18] are limited limitations for energy-saving points of view. They focused on the concept that a routing protocol is said to more energy-efficient if it accomplishes one or more aspects of the following: reducing the number of data transmissions, reducing total energy consumed in the network, exploiting the maximum number of alive nodes in overtime and balancing the load among different sensor in WSN.

The research work has been done in the direction of study the WSN performance with different routing and performance indices. The limited work is reported in which the routing algorithm is designed using hardware description language in the form of chip and performance is estimated on the hardware. The problem statement of the work is to design the chip of AODV algorithm and performs simulation with different cluster size and data size with the verification on FPGA. The state of the art of the work is that the successful data transfer will provide a new hardware platform in which the WSN nodes and security features can be integrated.

### 3 Ad-hoc on Demand Distance Vector (AODV) Routing System

AODV [19] is reactive on request protocol used for mobile infrastructure-less networks. It works based on the demand routing method for route formations among different nodes in the network. The protocol does not retain any routes but builds the path as per requirements. AODV is used to limit the disadvantages of DSR Protocol as the routing keeps information between the source node and destination node which makes it slow. In a large-scale network, it becomes very difficult to keep complete information of data packets header as multiple routes are existing from source node to destination node. Fig. 1 presents the sample of the AODV routing.

The behavior of AODV can be understood by considering a network consisting of 5 nodes that are 'S', 'A', 'B', 'C', and 'D', placed at unit distance from each other. The node 'S' is the source node and node 'D' is the destination node as depicted in Fig. 2. In AODV routing [20], two things are required to maintain one is sequence number and another is broadcast identity document (ID). The information of the destination ID is already. So, it is easy to maintain the destination sequence number and updated the route from source to destination. Route request (RREQ) and route response (RRES) are two signals used to send the request from source to destination as route discovering and reply from destination to source as response respectively. The IP addresses of the source and destination nodes are already known. The routing in AODV is based on the following fields. RREQ (Destination\_IP, Destination\_Sequence\_Number, Source IP, Source Sequence Number, Hop Count).

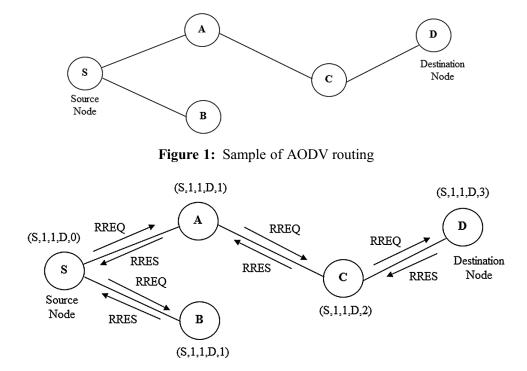


Figure 2: AODV routing network

The main objective of AODV routing is to process the data packets by identifying, discover and maintain the optimal path [21] between source and destination. The following steps are given to know the functionality of AODV.

*Step 1:* Let source node 'S' need to route destination 'D'. It will create a route request by entering (S, 1, 1, D, 0). Node 'S' broadcasts the request RREQ packet to its neighbors 'A' and 'B'. Nodes 'A' and B are identified as (S, 1, 1, D, 1) and (S, 1, 1, D, 1) respectively.

*Step 2:* The node 'A' & 'B' will check the availability of routes and will reply using RRESP packet return to source node 'S'. In this operation node 'B' is the last node and replies to 'S' by RREQ packet stating "route is not available", but node 'A' replies by RREP packet by stating 'route available'. The node 'A' further broadcast to node 'C', identified as (S, 1, 1, D, 2).

*Step 3:* Node A receives RREP and makes a forward route by counting the field of net hop in the RREQ format is updated. The node 'C' will send the return signal "route available" to node 'A' and will update the hop field in advance.

*Step 4:* The node 'C' broadcasts and the RREQ packet is sent to destination node 'D'. The node 'D' is identified as (S, 1, 1, D, 3), with updating of the next-hop count. Afterward, it will send the RRES packet to node 'C', which is further return to the source node 'S' by passing through intermediate node 'A' and node 'C. In this way, AODV routing provides an optimal path from source to destination.

#### 4 Methodology

The chip design, simulation, and synthesis steps are depicted in Fig. 3. The chip design of the AODV routing algorithm is carried out in Xilinx ISE 14.7. The steps are: design constraints, algorithm selection, modeling approach, register transfer level (RTL) analysis, function simulation and data communication with test benches FPGA synthesis, hardware parameters report analysis, and perform comparative

analysis [22] based on performance indices. The waveform is functionally checked on the Xilinx integrated synthesis environment simulator (ISIM). The data is analyzed in binary, hexadecimal, and American standard code for information interchange (ASCII) format.

| Design Aspects        | • Decide the size of the WSN Network. In the design<br>the size of the WSN is considered of nodes (5, 10, 20,<br>30100) based on the modular design approach  |
|-----------------------|---|
| Algorithm Selection   | • Select the appropriate routing algorithm to perform<br>the node intercommunication. In the design we have<br>taken AODV routing   |
| Modeling              | • The design is based on the behavior model in the Xilinx ISE 14.7 software. The design can be based on the dataflow or structural model.   |
| RTL                   | • The design is check for the number of the pins used in the design. It is checked based on the number of the input and output directed pins  |
| Functional Simulation | • The simulation of the chip is carried in the ISIM software to check the chip design is working or not and verified that the communication is taken from the source node to the destination  |
| Test Cases            | • To verify the functional simulation, some test cases<br>are applied. The ISIM waveform simulator shows the<br>test cases input given on the design  |
| Synthesis             | • The logic synthesis is carried out in real time data<br>communication on the FPGA hardware kit. The<br>Virtex-5 FPGA isused for the same. The main steps<br>for FPGA synthesis are logic placement, routing and<br>implementation to burn the bit file in FPGA. |
| Parameters            | • The FPGA synthesis includes the hardware summary of utilization. The hardware and timing parameters are analyzed for different cluster configuration of the network   |
| Comparative Analysis  | • Evaluate the comparative performance of AODV routing based on perormance indices: throughput, delay, control overhead and packet delivery ratio.  |

Figure 3: Methodology and flow

### **5** Results and Discussions

The AODV routing algorithm chip is designed using Xilinx ISE 14.7 software and simulation is carried to check the data packets transmitted from source to destination in the form of simulation waveforms. Fig. 4 presents the data transfer among nodes in the AODV routing protocol in WSN. The simulation is carried for the maximum 100 nodes  $M_0$  (0000000) - $M_{99}$  (1100100).

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| Name  | Value    | <br>171,120 ns | 171, 125 ns | 171,130 ns | 171, 135 ns |
|---|----------|----------------|-------------|------------|-------------|
| ါ <mark>ြ</mark> clock  | 1        |                |             |            |             |
| 🔓 reset   | 0        |                |             |            |             |
| in_node_address[6:0]  | 0000010  |                |             |            | 0000010     |
| Image: state st | 0000100  |                |             |            | 0000100     |
| packet_data_in[7:0]   | 01000001 |                |             |            | 01000001    |
| Packet_data_out[7:0]  | 01000001 |                |             |            | 01000001    |
|   |          |                |             |            |             |

(a)

| Value           |                                    | 1,980 ns                           | 1,985 ns                              | 1,990 ns   | 1,995 ns  |
|-----------------|------------------------------------|------------------------------------|---------------------------------------|--|---|
| L               |                                    |                                    |                                       |  |   |
| )               |                                    |                                    |                                       |  |   |
| 0001111         |                                    |                                    | 0001111                               |  |   |
| 0010000         |                                    |                                    | 0010000                               |  |   |
| 010010010110113 | 010                                | 0100101101110011                   | 00100011010010110                     | 00010100000001000                                    | 00001000000   |
| )1001001011011) | 010                                | 0100101101110011                   | 00100011010010110                     | 00010100000001000                                    | 00001000000   |
|                 | 001111<br>010000<br>10010010110111 | 001111<br>010000<br>10010010110111 | 001111<br>010000<br>10010010110111011 | 001111<br>010000<br>100100101101110<br>0100100101101 | 001111<br>010000<br>10010010110111<br>0100100101101 |

(b)

| Name  | Value    | <br>1,999,994 ps | 1,999,995 ps | 1,999,996 ps |
|---|----------|------------------|--------------|--------------|
| 🗓 clock   | 0        |                  |              |              |
| 🔓 reset   | 0        |                  |              |              |
| in_node_address[6:0]  | 0001111  |                  |              | 0001111      |
| Image: state st | 0010000  |                  |              | 0010000      |
| 🕨 📑 packet_data_in[63:0]  | India@@@ |                  |              | India@@@     |
| 🕨 📲 packet_data_out[63:0]   | India@@@ |                  |              | India@@@     |

(c)

| Name  | Value           |                | 1,965 ns                 | 1,970 ns        | 1,975 ns         | 1,980 ns              | 1,985 ns         | 1,990 ns              | 1,995 ns       |
|---|-----------------|----------------|--------------------------|-----------------|------------------|-----------------------|------------------|-----------------------|----------------|
| ါြ clock  | 0               |                |                          |                 |                  |                       |                  |                       |                |
| 🔓 reset   | 0               |                |                          |                 |                  |                       |                  |                       |                |
| in_node_address[6:0]  | 0000001         |                |                          |                 | 0000             | 001                   |                  |                       |                |
| Image: state st | 1100100         |                |                          |                 | 1100             | 100                   |                  |                       |                |
| 🕨 📑 packet_data_in[127:0]   | 010000010100111 | 01000001010011 | 1 10 1000 1000 10 10 1 1 | 001000000101011 | 0101001101001110 | 0 10000000 10 100 100 | 1101111011101010 | 1 10 1000 1 10 100 10 | 10111001100111 |
| b acket_data_out[127:0]   | 010000010100111 | 01000001010011 | 11010001000101011        | 001000000101011 | 0101001101001110 | 0 10000000 10 100 100 | 1101111011101010 | 110100011010010       | 10111001100111 |
|   |                 |                |                          |                 |                  |                       |                  |                       |                |

(d)

| Name  | Value            | _ , , , , , | 1,965 ns | 1,970 ns | 1,975 ns | 1,980 ns  |
|---|------------------|-------------|----------|----------|----------|-----------|
| ါ်အ clock   | 1                |             |          |          |          |           |
| 🔓 reset   | 0                |             |          |          |          |           |
| in_node_address[6:0]  | 0000001          |             |          |          | 0000     | 001       |
| Image: state st | 1100100          |             |          |          | 1100     | 100       |
| packet_data_in[127:0]   | AODV@WSN@Routing |             |          |          | AODV@WS  | N@Routing |
| packet_data_out[127:0]  | AODV@WSN@Routing |             |          |          | AODV@WS  | N@Routing |
|   |                  |             |          |          |          |           |

(e)

**Figure 4:** Xilinx ISIM simulation for source to the destination data transfer (a) 8-bit data transfer in binary (b) 64-bit data transfer in binary (c) 64-bit data transfer in ASCII (d) 128-bit data transfer in binary (e) 128-bit data transfer in ASCII

**Test Case- 1:** The AODV data (8-bit) communication is verified from source node  $M_2$  to node  $M_4$ . In\_node\_address [6:0] = "0000010", Out\_node\_address [6:0] = "0000100", Packet\_data\_in [7:0] = 1'h41 (hexadecimal) = "01000001" (binary) = A (in ASCII). The verified data packet is Packet\_data\_out [7:0] = 1'h41 (hexadecimal) = "01000001" (binary) = A (in ASCII) with PDR=1.

The synthesis process is carried out in the kit of Virtex-5 FPGA hardware. Tab. 1 lists the utilization and summary of the available hardware resources [23] for the nodes cluster varying in number (10, 20, 30....100). Tab. 2 lists the summary timing relating parameters and frequency [24] for the nodes cluster varying in number (10, 20, 30....100). Tab. 3 lists the performance matrices of the WSN for the nodes cluster (10, 20, 30....100) synthesized on the same FPGA [25]. Figs. 5 and 6 show the FPGA hardware and timing summary of the designed chip. Fig. 7 presents the graph for the performance indices of the AODV.

| Nodes | Slices | Flip-flops | IOBs | LUTs | GCLK |
|-------|--------|------------|------|------|------|
| 10    | 590    | 705        | 132  | 138  | 1    |
| 20    | 672    | 692        | 132  | 169  | 1    |
| 30    | 825    | 915        | 132  | 192  | 1    |
| 40    | 1089   | 1495       | 132  | 225  | 1    |
| 50    | 1417   | 1605       | 132  | 331  | 1    |
| 60    | 1645   | 2109       | 132  | 402  | 1    |
| 70    | 1830   | 2280       | 132  | 462  | 1    |
| 80    | 2105   | 2652       | 132  | 515  | 1    |
| 90    | 2450   | 2815       | 132  | 552  | 1    |
| 100   | 2915   | 3150       | 132  | 625  | 1    |

 Table 1: FPGA hardware parameters summary for AODV

| Nodes | Maximum<br>Frequency (MHz) | Min period<br>(ns) | Time (ns) before clock (minimum) | Time (ns) after<br>clock (maximum) | Memory Usage<br>(kB) |
|-------|----------------------------|--------------------|----------------------------------|------------------------------------|----------------------|
| 10    | 115                        | 1.152              | 1.165                            | 4.250                              | 103511               |
| 20    | 123                        | 1.721              | 1.920                            | 5.359                              | 131451               |
| 30    | 145                        | 1.860              | 2.251                            | 5.720                              | 152135               |
| 40    | 172                        | 1.945              | 2.927                            | 5.985                              | 182415               |
| 50    | 205                        | 2.172              | 2.990                            | 6.206                              | 199280               |
| 60    | 210                        | 2.400              | 3.051                            | 6.315                              | 212517               |
| 70    | 215                        | 2.610              | 3.250                            | 6.625                              | 228096               |
| 80    | 248                        | 2.790              | 3.515                            | 7.510                              | 244510               |
| 90    | 295                        | 2.915              | 3.620                            | 8.215                              | 291526               |
| 100   | 325                        | 2.990              | 4.005                            | 9.015                              | 351240               |

 Table 2: AODV routing timing-related information

## Table 3: Performance parameters for AODV

|     | Delay<br>(sec) | Throughput<br>(bps) | Control overhead | PDR   |
|-----|----------------|---------------------|------------------|-------|
| 10  | 0.035          | 0.205               | 0.0058           | 0.990 |
| 20  | 0.082          | 0.186               | 0.0059           | 0.990 |
| 30  | 0.090          | 0.176               | 0.0055           | 0.997 |
| 40  | 0.135          | 0.169               | 0.0052           | 0.996 |
| 50  | 0.198          | 0.145               | 0.0042           | 0.969 |
| 60  | 0.290          | 0.156               | 0.0055           | 0.985 |
| 70  | 0.310          | 0.167               | 0.0057           | 0.962 |
| 80  | 0.325          | 0.183               | 0.0039           | 0.960 |
| 90  | 0.382          | 0.190               | 0.0032           | 0.951 |
| 100 | 0.400          | 0.210               | 0.0060           | 0.975 |

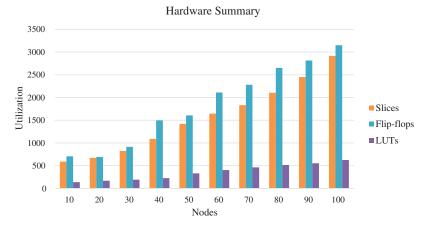
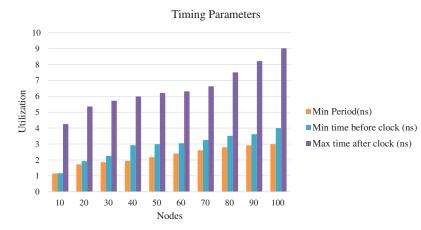


Figure 5: FPGA hardware summary



**Figure 6:** Timing information in AODV

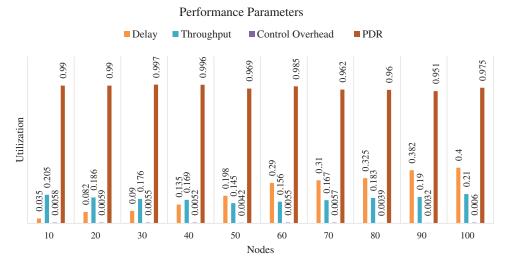


Figure 7: Performance matrices for AODV

#### **6** Conclusions

The hardware chip design of the AODV routing is done successfully in the Xilinx ISE 14.7. The internode communication is verified for the different cluster sizes (N = 10, 20, 30....100). The node behavior and effective data communication from source to destination are verified in the form of the Xilinx ISIM simulator that's shows verified effective data communication of 8-bit, 64-bit, and 128-bit among the different nodes. The data communication is verified successfully on the Virtex-5 FPGA hardware light-emitting diode (LED)\_ in the form of '1' and '0'. The estimated number of slices is 590, 672, 825, 1089, 1417, 1645, 1830, 2105, 2450 and 2915 for node cluster (N = 10, 20... 100). The number of LUTs are 138, 169, 192, 225, 331, 402, 462, 515, 552 and 625 node cluster (N = 10, 20... 100). The number of flip-flops are 705, 692, 915, 1485, 1605, 2109, 2280, 2652, 2815 and 3150 node cluster (N= 10, 20... 100). The total number of Input/output blocks is 132. The maximum frequency support of the design is 325 MHz for 100 nodes. It has been noticed that the hardware components and timing parameters are enhancing with the increase of node clusters. The performance matrices of the WSN are estimated. The minimum end-to-end delay is 0.035 s and the maximum delay is 0.400 s. The throughput varies for the different nodes and the maximum throughput is 0.210.

is approximate '1' in all the cases that signify the successful packet transfer from source to destination. In the future, we are planning to integrate the concept of cryptography and network security with data encryption and decryption algorithms in the designed hardware chip.

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**Conflicts of Interest:** The authors declare that they have no conflicts of interest to report regarding the present study.

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