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ARTICLE

A Fractional Order Fast Repetitive Control Paradigm of Vienna Rectifier for Power Quality Improvement

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ABSTRACT

Due to attractive features, including high efficiency, low device stress, and ability to boost voltage, a Vienna rectifier is commonly employed as a battery charger in an electric vehicle (EV). However, the $6k \pm 1$ harmonics in the ac-side current of the Vienna rectifier deteriorate the THD of the ac current, thus lowering the power factor. Therefore, the current closed-loop for suppressing $6k \pm 1$ harmonics is essential to meet the desired total harmonic distortion (THD). Fast repetitive control (FRC) is generally adopted; however, the deviation of power grid frequency causes delay link in the six frequency fast repetitive control to become non-integer and the tracking performance to deteriorate. This paper presents the detailed parameter design and calculation of fractional order fast repetitive controller (FOFRC) for the non-integer delay link. The finite polynomial approximates the non-integer delay link through the Lagrange interpolation method. By comparing the frequency characteristics of traditional repetitive control, the effectiveness of the FOFRC strategy is verified. Finally, simulation and experiment validate the steady-state performance and harmonics suppression ability of FOFRC.

KEYWORDS

Vienna rectifier; fast repetitive control; fractional order; performance analysis

1 Introduction

Industrialization requires a lot of energy consumption [1], and the pollution problem caused by the consumption of fossil energy [2] is becoming more and more serious. Therefore, new energy can flourish, and electric vehicle [3] is one of the hotspots. Supercapacitor [4] as an energy storage technology to provide energy for electric vehicles [5] has been widely concerned by scholars. Literature [6–8] has done research on the characteristics of new materials for capacitors. With the continuous expansion of the market scale of electric vehicles [9], the high-power DC charging technology of fast charging has developed rapidly, that is, the common DC charging pile in the market [10]. The main power of the DC charging pile is cascaded by the front stage rectifier and the rear stage DC/DC converter [11]. The front stage rectifier mainly includes traditional bridge PWM rectifier and Vienna rectifier. Compared with the traditional bridge PWM rectifier, Vienna rectifier has fewer switching

devices, and the voltage stress borne by the switch devices is half of the bus voltage on the DC side. There is no need to consider the direct connection of the upper and lower bridge arms and the dead band setting of the switch devices [9]. Therefore, Vienna rectifier is generally used as the front stage circuit. At the same time, as the interface converter between power grid and load, rectifier plays an important role in restraining current harmonics [12].

The key to restraining current harmonics, reducing total harmonic distortion (THD) and improving power quality lies in the control of AC current [13]. The literature [14] adopted the current control strategy based on PI control, which is widely used, but the control of AC harmonic by PI controller is not ideal. In order to control AC current harmonics, the control strategy based on internal model principle has been widely studied by scholars. The literature [15] used resonance control to suppress periodic current harmonics, but it can only be controlled for a specific harmonic.

Repetitive control (RC) can effectively realize the accurate tracking of harmonic signal by accumulating and tracking the error cycle by cycle [16], but there is an inherent delay of fundamental wave period [17]. In literature [18], a steady-state compensator is designed using H∞ theory for RC based on internal model principle. However, the computational complexity of the algorithm in a complex grid connected environment is a little complex, especially considering the nonlinear and unbalanced load. The literature [19,20] proposed a multi-rate RC control strategy and applied it in a PWM inverter. However, with nonlinear loads, the peak tracking error may become larger. The literature [21] proposed a filter that can estimate the unknown input of the system and effectively suppress the noise. The literature [22] used an auxiliary function based on linear interpolation to improve RC to shorten cycle delay. However, it does not take into account the situation when the grid frequency is offset. The literature [23] proposed a fast repetitive control (FRC), whose control period is only half of that of traditional RC, but when the RC frequency is further improved, the number of periodic delay points may be non-integers, which will affect the tracking accuracy. Moreover, the FRC cannot work normally when the frequency fluctuates. When the grid frequency shifts, its resonant frequency will deviate from the actual harmonic frequency of the grid [24], resulting in large control error. The literature [25] proposed two FRC methods to adapt to frequency fluctuation. One is to reduce the sensitivity to frequency fluctuation by reducing the internal model coefficient Q, but it will affect the gain; One is to change the traditional RC structure, so that the RC link becomes the sum of multiple resonant terms, so as to achieve frequency adaptation. However, due to the large resonant bandwidth, the rapidity of response is affected.

In order to solve the problem that the delay link of fast repetitive control becomes non-integer when the power grid frequency fluctuates, a fractional order fast repetitive control (FOFRC) strategy is proposed. The Vienna rectifier system is modeled, the Lagrange interpolation method is used, and the Lagrange interpolation method is used to replace the non-integer delay link with polynomial, which shortens the periodic delay of the traditional RC and makes the controller to accurately track the expected output. From the perspective of frequency characteristics, it is analyzed and compared with traditional RC and FRC. At the same time, a zero phase shift filter is designed to improve the stability and anti-interference of the system. The simulation and experimental results show that the FOFRC strategy has better steady-state performance, suppresses the THD of AC current at the grid side and has less AC harmonic component.

The rest chapters are arranged as follows: The second part introduces the topology and control strategy of Vienna rectifier; The third part analyzes the problems of rapid repetitive control; In the fourth part, a fractional order fast repetitive control strategy based on Lagrange interpolation

polynomial is proposed, and its stability is proved. In the fifth part, the proposed control strategy is verified by simulation and experiment. The sixth part summarizes the full paper.

2 Topology and Control Strategy of Vienna Rectifier

This article takes the Vienna rectifier as the research object. The topological of Vienna rectifier is shown in Fig. 1. e_a, e_b, e_c are the voltages of AC side, L is input side inductor, R is the equivalent resistance, i_a, i_b, i_c are the three-phase AC grid current, $D_1 \sim D_6$ are uncontrollable diodes, i_p and i_n are the current flowing through the DC bus respectively, and i_o is the neutral point current at the DC side, C_1 and C_2 are series equivalent capacitors on the output side, i_{c1} and i_{c2} are the currents flowing through capacitors C_1 and C_2, respectively, R_L is DC side resistive load, i_L is the load current, S_a, S_b, S_c are bidirectional switches, and each bidirectional switch is composed of two IGBT power devices in series.

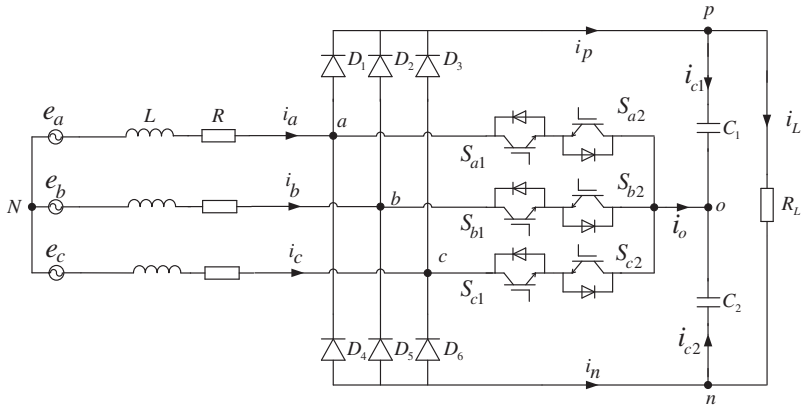


Figure 1: Three phase Vienna rectifier topology

The double closed-loop control strategy for Vienna rectifier is shown in Fig. 2. The current inner loop adopts the composite control strategy to effectively control the fundamental wave and 6k harmonics, reduce the THD of AC input current and improve power quality.

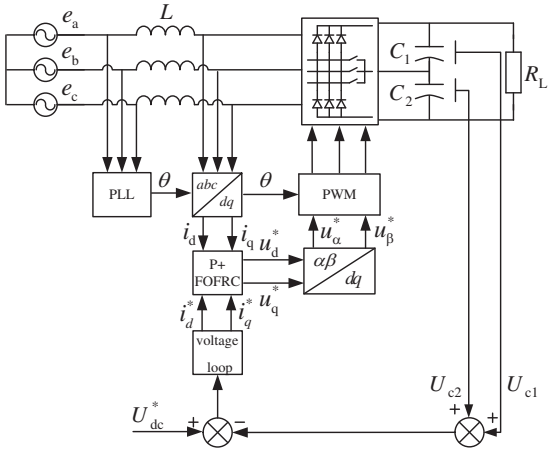


Figure 2: Droop control block diagram

3 FRC and Its Problems

3.1 Traditional RC and Its Rapidity

The current inner loop control [14] block diagram of traditional repetitive control is shown in Fig. 3. In Fig. 3, block diagram of traditional repetitive control, N is the number of samples in a cycle, that is, the ratio of sampling frequency to grid frequency. k_r is the gain coefficient, $Q(z)$ is the internal model coefficient, $S(z)$ is the correction link,z^k is the phase lead link, $P(z)$is the controlled object.

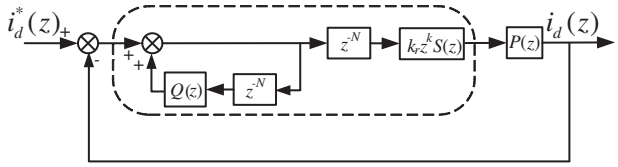


Figure 3: Current control block diagram of traditional repetitive control

The transfer function of traditional repetitive control is shown in Eq. (1).

$$G_{CRC}(z) = \frac{k_r z^{k-N} S(z)}{1 - Q(z) z^{-N}} \tag{1}$$

If the grid frequency is defined as f_0, there is a delay time $T_0(T_0=1/f_0)$, which just corresponds to a periodic sampling point N. Therefore, repetitive control does not work in the first cycle of dynamic response, resulting in poor dynamic response ability. Moreover, when N (periodic sampling points) is relatively large, it occupies a large memory.

Aiming at the problem of traditional RC, the sampling frequency is increased to reduce the number of periodic delay points and improve the dynamic performance. The dynamic performance of RC with different sampling frequencies is shown in Fig. 4. It can be seen that the delay time decreases with the increase of sampling frequency, and the occupied memory unit also decreases.

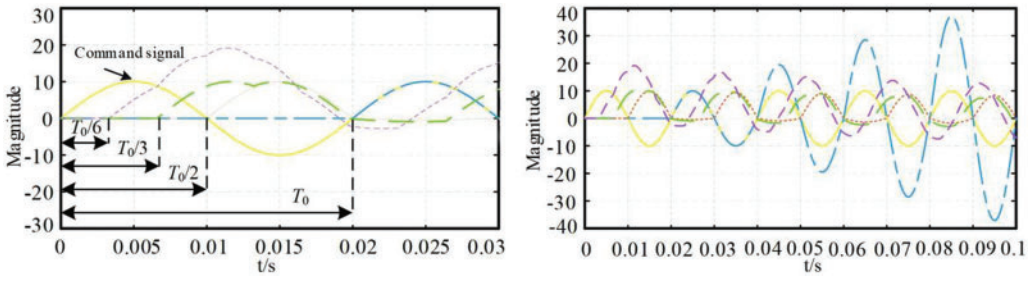


Figure 4: Dynamic performance curve of RC with different sampling frequencies

In practice, according to the requirements of the controlled object, only the harmonics at a specific frequency need to be suppressed. The harmonic of the three-phase Vienna rectifier AC side current in this paper is mainly 6k ± 1 harmonic [22], which changes into 6k harmonic in *dq* rotating coordinate system after coordinate transformation. According to the characteristics of 6k harmonics, six times frequency FRC strategy is adopted. The current inner loop control block diagram of six octave FRC strategy is shown in Fig. 5.

The transfer function of the FRC strategy in Fig. 5 is shown in Eq. (2).

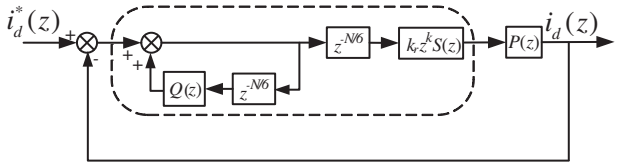


Figure 5: Current control block diagram of FRC

$$G_{FRC}(z) = \frac{k_r z^{k-\frac{N}{6}} S(z)}{1 - Q(z) z^{-\frac{N}{6}}} \tag{2}$$

3.2 Problems in FRC

Although FRC strategy improves the dynamic performance of the system and reduces the use of memory in digital implementation, when the designed sampling frequency is unreasonable, N/6 is not an integer and can only be approximately rounded in discrete, resulting in large deviation between discrete form $z^{-N/6}$ and continuous form $e^{-sT/6}$, deviation from the actual harmonic frequency and weak suppression effect. Bode diagram of FRC strategy in continuous domain and discrete domain is shown in Fig. 6. It can be seen from the figure that the discrete resonant frequency has deviated from the original continuous resonant frequency, which will certainly lead to poor tracking performance.

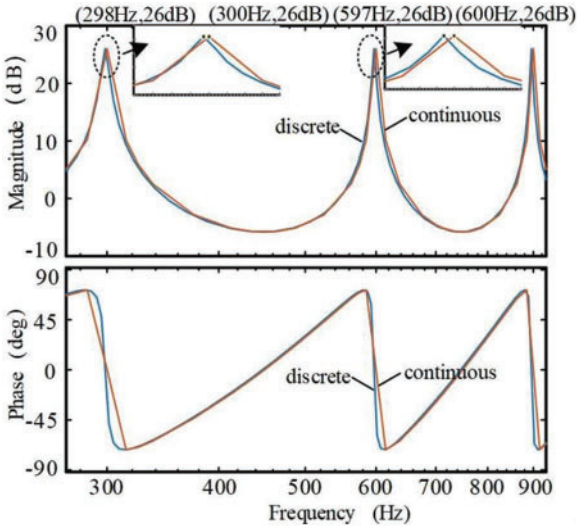


Figure 6: Comparison of Bode diagram of fast repetitive control in continuous domain and discrete domain

Even if the sampling frequency has been reasonably designed, because the actual grid frequency f_0 will offset, N/6 will not be an integer, resulting in attenuation of control gain and degradation of tracking performance. Assuming that the grid frequency offset is 0.6 Hz, the Bode diagram of FRC strategy near the 5th harmonic is shown in Fig. 7. At this time, the 5th harmonic frequency is shifted by 3 Hz, the corresponding gain is attenuated to 10.7 dB, and the control effect is obviously weakened.

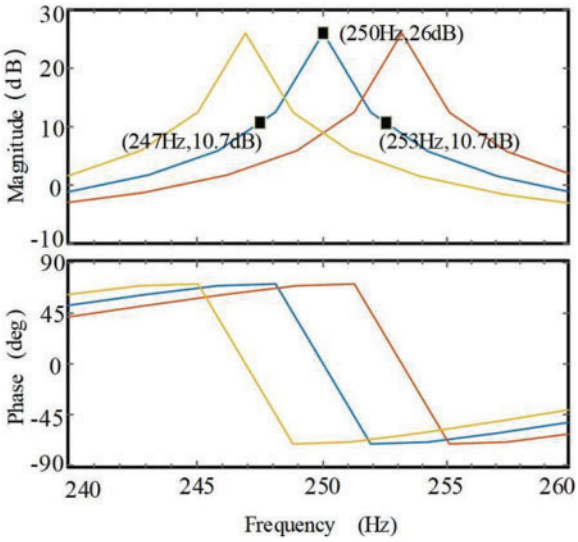


Figure 7: Fast repetitive control Bode diagram of power grid frequency offset ±0.6 Hz

4 Proposed Fractional-Order Fast Repetitive Control Strategy

4.1 Fractional Order Based Fast Repetitive Control

In this paper, a fractional order fast repetitive control strategy is proposed to solve the non-integer delay caused by power grid frequency offset. Firstly, Lagrange interpolation polynomial is used to replace the fractional part of non-integer delay link. Secondly, zero phase shift filter is used to design internal model link to improve the stability and gain of the system. Finally, good steady-state performance is achieved, the THD of AC current at the grid side is reduced, the harmonic suppression ability is improved, and the stable operation of the system is realized.

In order to approximate the non-integer part, fractional order fast repetitive control is introduced, and the delay points are divided into two parts [24], as shown in Eq. (3):

$$\frac{N}{6} = \text{int}\,(N_i) + d \tag{3}$$

where N_i is an integer and d is a non-integer. According to the Lagrange interpolation method, the approximate function expression of z^{-d} can be expressed as Eq. (4):

$$\begin{cases} z^{-d} \approx H\,(z) = \sum_{n=0}^{M} h\,(n)\, z^{-n} \\ h\,(n) = \prod_{k=0 \cap k \neq n}^{M} \dfrac{r-k}{n-k}, n = 0, 1, 2, \ldots, M. \end{cases} \tag{4}$$

where $h(n)$ is the polynomial coefficient, and M is the order of the interpolation polynomial. The direct form implementation based on Lagrange interpolation polynomial is shown in Fig. 8.

According to $h(n)$ from (4), the coefficients for M = 1, 2, and 3 are given, in Table 1.

The control block diagram of FOFRC strategy is shown in Fig. 9.

In order to realize the good control of fundamental and harmonic, the compound control strategy of PI control and fractional order fast repetitive control in parallel is adopted. The transfer function of the controlled object $P(s)$ is $1/(Ls+R)$, and $P(z)$ is discretized by bilinear transformation.

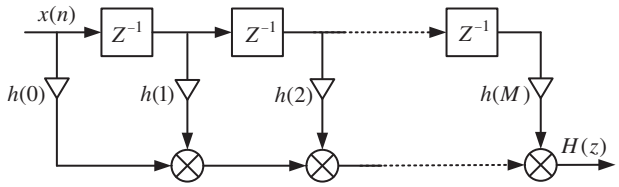


Figure 8: Direct form implementation of Lagrange interpolation

Table 1: Coefficients of the Lagrange interpolation of M = 1, 2, and 3

	$M=1$	$M=2$	$M=3$
$h(0)$	$1-d$	$(d-1)(d-2)/2$	$-(d-1)(d-2)(d-3)/6$
$h(1)$	d	$-d(d-2)$	$d(d-2)(d-3)/2$
$h(2)$		$d(d-1)/2$	$-d(d-1)(d-3)/6$
$h(3)$			$d(d-1)(d-2)/6$

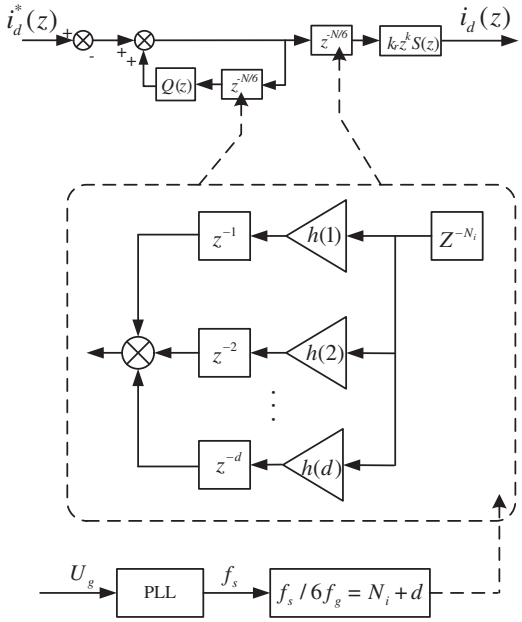


Figure 9: Block diagram of the proposed FOFRC

4.2 FOFRC Stability Analysis

According to Fig. 10, the transfer function of the current inner loop is in Eq. (5):

$$\frac{i_d(z)}{i_d^*(z)}=\frac{[G_1(z)+G_2(z)]P(z)}{1+[G_1(z)+G_2(z)]P(z)}=\frac{G_1(z)+G_2(z)}{1+G_2(z)G_3(z)}G_3(z)=\frac{G_1(z)-z^{-N/6}\left[Q(z)G_1(z)-k_rz^kS(z)\right]}{1-z^{-N/6}\left[Q(z)-k_rz^kS(z)G_3(z)\right]}G_{3(z)} \tag{5}$$

where

$$\begin{cases} G_1(z) = k_p \\ G_2(z) = \dfrac{k_r z^k S(z) z^{-\frac{N}{6}}}{1 - Q(z) z^{-\frac{N}{6}}} \\ G_3(z) = \dfrac{P(z)}{1 + G_1(z) P(z)} \end{cases}$$

then

$$\begin{cases} H_0 = 1 + G_1(z) P(z) \\ H_1 = Q(z) - k_r z^k S(z) G_3(z) \end{cases} \tag{6}$$

When the characteristic roots of the system are in the unit circle, the discrete system is stable. According to Eq. (6), the stability of the current inner loop needs to meet the following two conditions:

1) The roots of H_0 are inside the unit circle;

2) $|H_1| < 1$.

Condition 1) shows that the proportional control is stable when the root of H_0 is in the unit circle; Condition 2) shows that the FRC is stable.

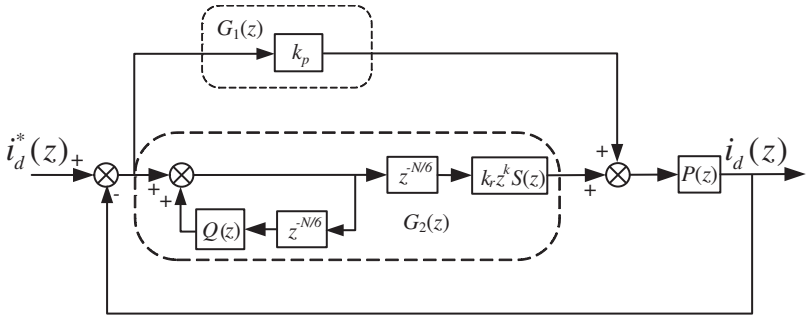


Figure 10: Current inner loop control block diagram based on FOFRC

4.3 FOFRC Controller Design

FOFRC is improved from the basis of the traditional RC, so the FOFRC controller can be designed using the method of the traditional controller.

The internal mode coefficient $Q(z)$ is usually a constant less than 1 or a low-pass filter. When $Q(z)$ is a constant less than 1, the closer the constant is to 1, the greater the gain of the system, but the easier it is to be unstable; When $Q(z)$ is in the form of low-pass filter, its amplitude gain is higher at low frequency, but there is a problem of phase lag. In order to ensure the control effect, the zero-phase shift filter is selected [26–28]. The general expression of zero phase shift filter is as Eq. (7):

$$Q(z) = \frac{a_0 + \sum_{i=1}^{M} (a_i z^{-i} + a_i z^{i})}{a_0 + 2\sum_{i=1}^{M} a_i} \tag{7}$$

where M is the order of the filter, a_0, a_i is the coefficient. In practical application, M is usually taken as 1. The expression is as Eq. (8):

$$Q(z) = \frac{a_0 + a_1 \left(z^{-1} + z\right)}{a_0 + 2a_1} \tag{8}$$

Convert it to frequency domain, the expression is as Eq. (9):

$$Q(\omega T_s) = \frac{a_0 + a_1\left(e^{-j\omega T_s} + e^{j\omega T_s}\right)}{a_0 + 2a_1} = \frac{a_0 + 2a_1\cos(\omega T_s)}{a_0 + 2a_1} \tag{9}$$

In order to ensure the stability of fast repetitive controller, $|Q(\omega T_s)| < 1$, let $a_0+2a_1 = 1$, the following Eq. (10) is obtained:

$$Q(\omega T_s) = a_0 + 2a_1\cos(\omega T_s) \tag{10}$$

From Eq. (10), the following expression in Eq. (11) is obtained:

$$|Q(\omega T_s)| = \begin{cases} a_0 + 2a_1, \omega T_s = 0 \\ a_0 - 2a_1, \omega T_s = \pi \end{cases} \tag{11}$$

Since the zero phase shift filter has high amplitude gain at low frequency and attenuation at high frequency, therefore, when $\omega T_s = 0$, let $|Q(\omega T_s)| = 1$; when $\omega T_s = \pi$, let $|Q(\omega T_s)| = 0$.

$$\begin{cases} a_0 + 2a_1 = 1 \\ a_0 - 2a_1 = 0 \end{cases} \rightarrow \begin{cases} a_0 = 0.5 \\ a_1 = 0.25 \end{cases} \tag{12}$$

its expression in Eq. (12) is given $Q(z) = \left(z^{-1} + 2 + z\right)/4$.

As shown in Fig. 10, the current inner loop is a parallel form of proportional control and fractional order fast repetitive control. The compensator $S(z)$ is designed according to the expected function correction method, and can be expressed as Eq. (13):

$$S(s) = \frac{(Ls + R)\omega^2}{s^2 + 2\xi\omega s + \omega^2} \tag{13}$$

The sampling frequency of the controller is 20 kHz, so the cut-off frequency of the compensator is selected as $f = 1$ kHz, $\omega = 2000\pi$, the damping coefficient is selected as 0.707, and the expression of the compensator in the discrete domain can be obtained as Eq. (14):

$$S(z) = \frac{2.382z^2 + 0.01425z - 2.368}{z^2 - 1.565z + 0.6437} \tag{14}$$

After adding the compensator, the phase of the controlled object lags, as shown in Fig. 11. At this time, the lead link z^k is needed for compensation.

The order of the lead link is determined according to the effect of the lead link. The phase frequency characteristics of $z^k S(z)P(z)$ under different lead orders are shown in Fig. 12. It can be seen that when $k = 3$, the compensation for phase lag is the best. In this paper, $k = 3$.

In order to make the system have better stability and dynamic performance, according to the stability condition of the current inner loop, the root of H_0 should be in the right half plane of the unit circle and close to the coordinate origin, and the Nyquist curve of H_1 should approach the center of the unit circle. Considering the situation of H_0 and H_1, $k_p = 20$ is taken in this paper. Generally, k_r is a constant less than 1. The smaller the value of k_r, the better the stability of the system. In this paper, the repetitive control gain k_r is selected as 0.2.

Assuming that the sampling frequency of the system is 20 kHz, the number of periodic delay points of fast repetitive control is $N = 20\text{K}/50/6 \approx 66.7$. Bode diagram of traditional RC, FRC and FRC after optimizing sampling frequency is shown in Fig. 13.

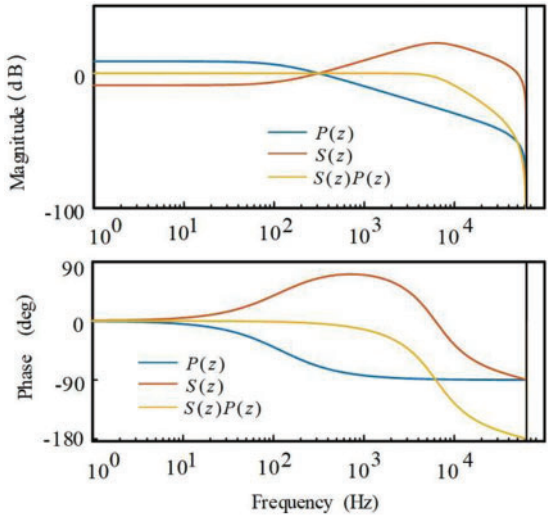


Figure 11: The compensation effect of $S(z)$

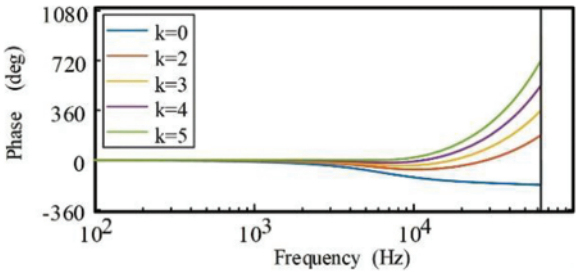


Figure 12: z^k compensation effect of different orders

Since N/6 is not an integer, when the FRC is realized by discrete digitization, the resonant frequency shifts to 298 Hz at 300 Hz and 896 Hz at 900 Hz. This effect is more obvious at higher frequencies, and the deviation of resonant frequency reaches 10 Hz, as shown in Figs. 13a–13c, respectively. After optimizing the sampling frequency of the system to 20.7 kHz, it can be seen that the FRC after optimizing the sampling frequency can achieve the effect of traditional RC, so as to ensure the accurate tracking of harmonics.

If the sampling frequency of the optimized system is 20.7 kHz, N/6 = 69. If the grid frequency does not shift, the control effect of FRC can be guaranteed. Assuming that the grid frequency offset is +0.6 Hz, the number of periodic delay points of FRC $N/6 = 20.7\,\mathrm{K}/50.6/6 \approx 68.2$, $N_i = 67$, d = 1.2. $z^{-\frac{N}{6}} \approx z^{-68.2} = z^{-67} * z^{-1.2}$.

If the sampling frequency of the optimized system is 20.7 kHz, N/6 = 69. If the grid frequency does not shift, the control effect of FRC can be guaranteed. Assuming that the grid frequency offset is +0.6 Hz, the number of periodic delay points of FRC.

When non-integer d is close to M/2, the interpolation effect is the best [17]. $d = 1.2$, closest to 1, so M/2 = 1, M = 2.

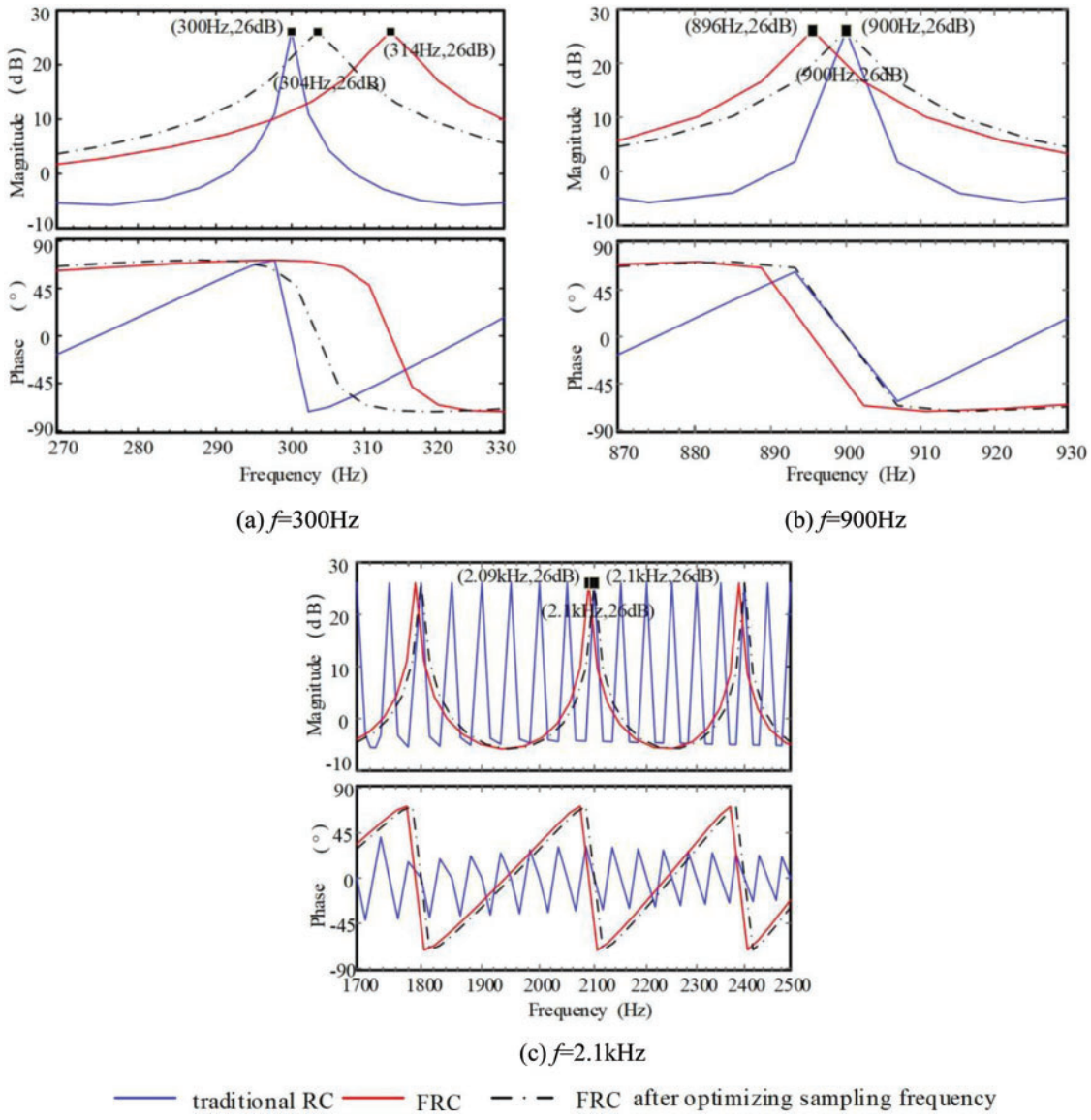


Figure 13: Comparison of Bode diagram of different repetitive control

According to the calculation formula when M = 2 in Table 1, bring in the value of d to calculate $h(0)$, $h(1)$ and $h(2)$. Fractional delay is obtained Eqs. (15) and (16):

$$z^{-d} : z^{-1.2} \approx -0.08 + 0.96z^{-1} + 0.12z^{-2} \tag{15}$$

$$z^{-68.2} \approx z^{-67} * z^{-1.2} = -0.08z^{-67} + 0.96z^{-68} + 0.12z^{-69} \tag{16}$$

Bode diagrams of traditional RC, FRC and FOFRC are shown in Fig. 14. After the grid frequency is offset, the actual frequency of 5th and 7th harmonics in *dq* coordinate system shall be $50.6 \times 6 = 303.6$ Hz. Because the traditional RC has no frequency adaptive ability, its fifth harmonic frequency is

still 300 Hz; FRC causes the resonant frequency to shift to 314 Hz due to approximate rounding; The FOFRC resonant frequency is finally fitted to 304 Hz. This difference in frequency tracking accuracy is more obvious at higher harmonics. As shown in Fig. 14b, the theoretical offset value of 17th and 19th harmonics in *dq* coordinate system is $0.6 \times 18 = 10.8$ Hz, the actual offset of FRC is 41 Hz, and the actual offset of FOFRC method is 11 Hz. The tracking effect of frequency offset is obviously better than FRC.

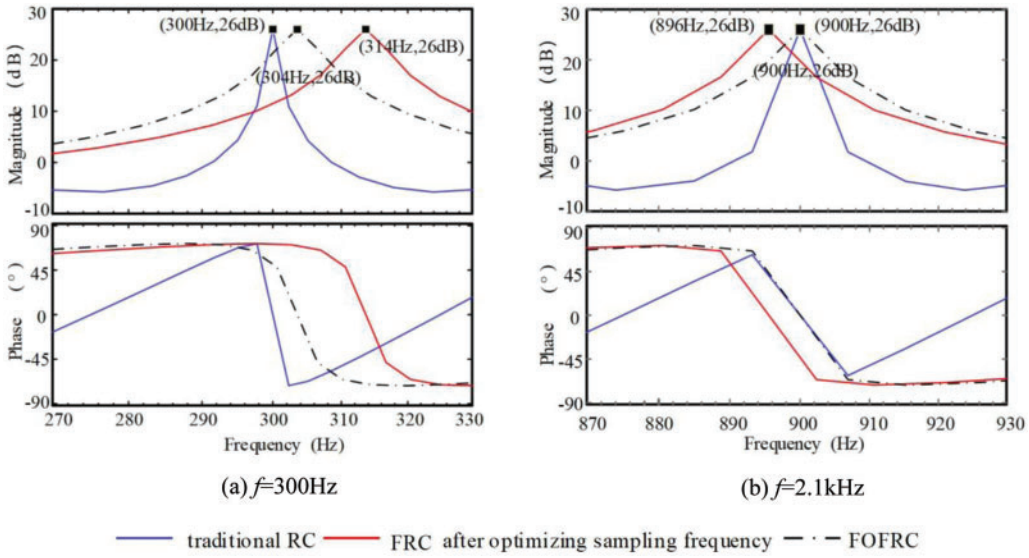


Figure 14: Comparison of Bode diagram of different repetitive control in power grid frequency offset

5 Simulation and Experimental Verification

In order to verify the effectiveness of the method proposed in this paper, the simulation model of the Vienna rectifier control system is built in MATLAB, and the simulation parameters are shown in Table 2.

Table 2: System parameter

Parameters	Value
Phase voltage(u_s)	220 V
AC voltage rated frequency(f_0)	50 Hz
AC side inductance(L)	3 mH
Equivalent impedance(R)	0.36 Ω
Switching frequency(f_s)	20 kHz
DC side voltage(u_{dc})	800 V
DC side capacitance(C_1, C_2)	1000 μF
DC side load(R_L)	50 Ω

5.1 Simulation Verification of Fractional Order Fast Repetitive Control Strategy

The simulation waveform diagrams in Fig. 15 are steady state AC current waveforms from traditional RC, FRC and FOFRC strategies. When the grid frequency offset is +0.6 Hz, because the traditional repetitive control has no frequency adaptive ability, the power grid current waveform distortion is serious, and the THD is as high as 8.19%. The FRC strategy has a certain frequency adaptive ability, and the THD is improved to 5.87%, but the discrete approximate rounding still leads to a large THD. The FOFRC strategy has good adaptability to frequency offset, the grid current waveform is significantly improved, the THD is further reduced to 1.84%, and high steady-state accuracy is realized.

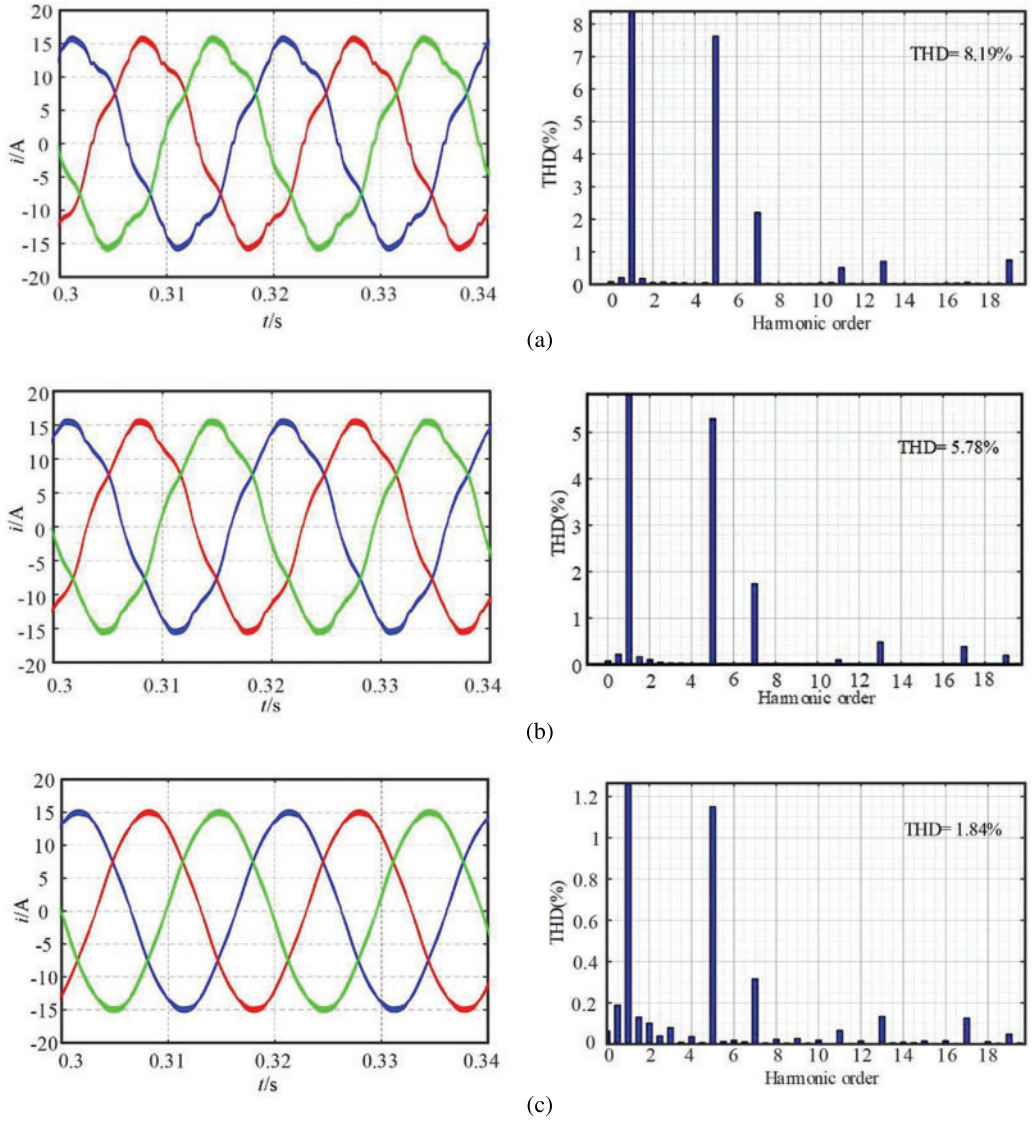


Figure 15: Steady state AC current waveforms with grid frequency offset of 0.6 Hz (a) traditional RC; (b) fast repetitive control; (c) FOFRC

In order to further compare and analyze the steady-state performance of rectifier, THD of steady-state input current and tracking error, the results are shown in Table 3. It can be seen from Table 3 that the fractional order fast repetitive control strategy proposed in this paper can greatly reduce the frequency tracking error, significantly reduce the current steady-state THD, and significantly improve the steady-state characteristics of the rectifier, so as to suppress the influence of harmonics on the current waveform distortion. The current waveform distortion can be observed in the simulation. The control method proposed in this paper has good waveform.

Table 3: Simulation results of steady-state performance of rectifier

	Harmonic frequency	Control strategy		
		Traditional RC	FRC	FOFRC
Current steady state THD		8.19%	5.78%	1.84%
Frequency tracking error	300 Hz	3.6 Hz	10.4 Hz	0.4 Hz
	900 Hz	10.8 Hz	41 Hz	11 Hz
	2.1 kHz	24 Hz	200 Hz	30 Hz

5.2 Experimental Verification of Fractional Order Fast Repetitive Control Strategy

According to the theoretical analysis and simulation above, an experimental prototype of Vienna rectifier based on TMS320F28335 is built as shown in Fig. 16. The experimental parameters are the same as those in Table 2. Tektronix P5200A different probe is used to measure the voltage signal, Tektronix TCPA300 probe is used to measure the current signal. The Tektronix MDO 3034 mixed domain oscilloscope is used to capture and analyze the signals. The total harmonic distortion is measured by Fluke 43B Power Quality Analyzer.

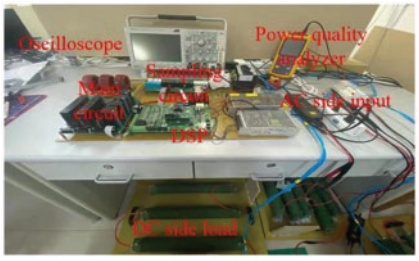


Figure 16: Experimental prototype

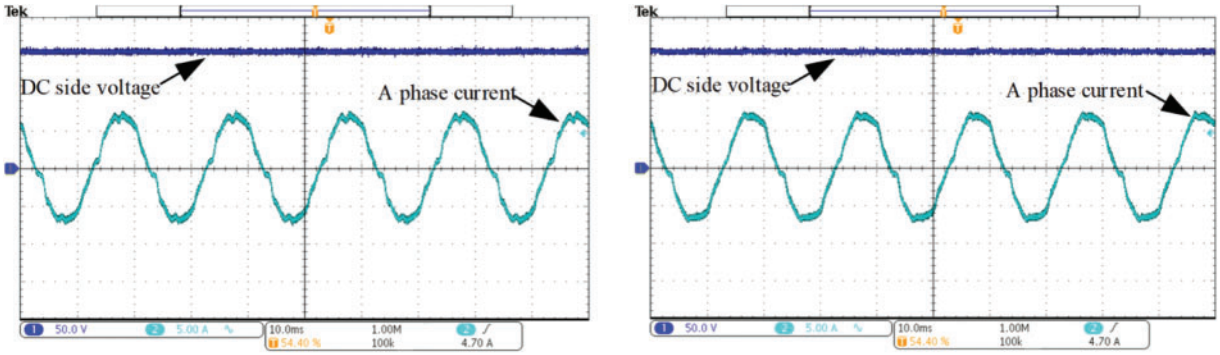
The grid frequency offset is 0.6 Hz, the THD diagrams of the traditional RC, FRC and FOFRC strategies captured by the Fluke 43B Power Quality Analyzer are shown in Fig. 17. The THD of 2.6% from the FOFRC strategy is obviously less than the THD of 6.8% from the FRC strategy and the THD of 8.5% from the traditional RC strategy. These results illustrate that the FOFRC strategy can track the expected value more accurately than the traditional RC and FRC strategies. The harmonic compensation performance of the system is improved and has better performance harmonic suppression capability.

(a) (b) (c)

Figure 17: THD diagrams with grid frequency offset of 0.6 Hz: (a) traditional RC; (b) fast repetitive control; (c) FOFRC

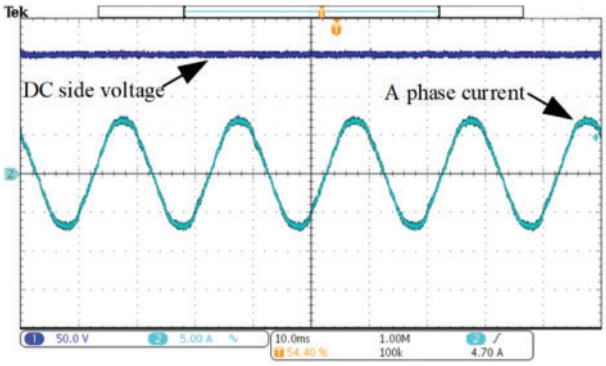
The grid frequency offset is 0.6 Hz, the steady-state AC current waveforms of traditional RC, FRC and FOFRC strategies are shown in Fig. 18. The AC current of power grid is seriously distorted in the waveform of traditional RC, the current waveform is improved in the waveform of FRC strategy, but some distortion can still be seen. The power grid current waveform is significantly improved in the waveform of FOFRC, and the current waveform is smoother and sinusoidal.

After the current THD data is derived by the power quality analyzer, the results are shown in Table 4. By observing the data in Table 4, the proposed strategy in this paper reduces the THD of current from 8.5% to 2.6%, which verifies the effectiveness of this method in improving the steady-state characteristics of rectifier. Due to the influence of noise and sensor accuracy in the hardware experiment, the THD of the experimental current waveform is higher than that of the simulated waveform current. However, compared with the THD under each control method in the experiment, the method proposed in this paper greatly reduces the current THD without obvious distortion.



(a) (b)

Figure 18: (Continued)



(c)

Figure 18: Steady state AC current waveforms with grid frequency offset of 0.6 Hz: (a) traditional RC; (b) fast repetitive control; (c) FOFRC

Table 4: Experimental results of steady-state performance of rectifier

Control strategy	Current steady state THD
Traditional RC	8.5%
FRC	6.8%
FOFRC	2.6%

6 Conclusion

Aiming at the widely concerned interaction technology between electric vehicle and power grid, this paper analyzes the typical topology Vienna rectifier suitable for electric vehicle DC charging pile. On this basis, considering the problem that the traditional repetitive control has poor steady-state accuracy and cannot accurately track the expected output in the case of power grid frequency offset, a fractional order fast repetitive control is proposed, the combination of fractional order fast repetitive control and proportional control is applied to the current inner loop.

Firstly, the reason why the repetitive control delay link in power grid frequency offset is non-integer is analyzed. Secondly, the non-integer delay link that cannot be realized by discrete system is approximated by Lagrange interpolation polynomial, and the fractional delay element is used to overcome the influence of non-integer periodic delay, which effectively improves the fitting accuracy. The simulation and experimental results show that the FOFRC controller effectively improves the frequency characteristics of repetitive control, ensures the steady-state accuracy of repetitive control in the case of grid frequency offset, and reduces the current THD of repetitive control in the case of grid frequency offset. Compared with traditional RC and FRC, the steady-state sinusoidal AC current under FOFRC is smoother, and the THD is only 2.6%. Therefore, Vienna rectifier with FOFRC has better steady-state performance and harmonic suppression ability.

However, the parallel combined control has coupling to the control effect. In the next step, the coupling analysis of the combined control to the control effect will be carried out. In addition, the engineering application and popularization of control strategy is also a problem worthy of discussion.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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