

A Time-Domain Comparator Based Skipping-Window SAR ADC

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Received: 10 March 2021; Accepted: 13 April 2021

Abstract: This paper presents an energy efficient successive-approximation register (SAR) analog-to-digital converter (ADC) for low-power applications. To improve the overall energy-efficiency, a skipping-window technique is used to bypass corresponding conversion steps when the input falls in a window indicated by a time-domain comparator, which can provide not only the polarity of the input, but also the amount information of the input. The time-domain comparator, which is based on the edge pursuing principle, consists of delay cells, two NAND gates, two D-flip-flop register-based phase detectors and a counter. The digital characteristic of the comparator makes the design more flexible, and the comparator can achieve noise and power optimization automatically by simply adjusting the delay cell number. An energy efficient digital-to-analog converter (DAC) control scheme suitable for the skipping window technique is also developed to reduce the switching energy during SAR conversion. Together with the skipping-window technique, the linearity and the power consumption of the SAR ADC are improved. The impact of different window sizes on comparison cycles, DAC switching energy and the overall energy efficiency is analyzed. Simulation results show that the proposed skipping-window technique can improve the overall energy-efficiency of the SAR ADC, as well as the linearity, and the optimized window size for the overall energy efficiency will vary with the DAC switching energy.

Keywords: Skipping-window technique; DAC switching scheme; time-domain comparator; low-power

1 Introduction

Internet of Things (IoTs) can connect many devices together to formulate a smart network, which can be used in smart home, intelligent transportation, smart grid, wise medical, smart agriculture and smart cities [1–3]. Such a huge devices put a stringent power budget on the system, and low power is usually the basic requirement. For this reason, IoT devices with low power ADC are highly attractive. In terms of energy-efficiency, successive-approximation register (SAR) analog-to-digital converter (ADC) is a good candidate due to its low power, medium resolution



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and medium speed. Moreover, SAR ADC mainly consists of digital circuits, which can scale with the technology friendly.

To improve the energy efficiency and resolution of SAR ADC, researches focused on digital-to-analog converter (DAC) switching scheme and comparator have been developed [4–14]. Many energy-efficient DAC switching schemes have been developed to reduce the switching energy during SAR conversion [4,14–17]. Monotonic switching scheme in [4] reduces the switching energy by 81% compared to conventional SAR scheme, with the disadvantage of common mode voltage variation. In order to further improve the energy efficiency of the DAC switching scheme, a third voltage reference is introduced. Merged capacitor switching scheme [14], Tri-level [15], Vcm-based monotonic scheme [16] reduced the switching energy by 87%, 96.9%, 97.7%, respectively. However, the DAC switching energy only occupies for only about 30% of power consumption in modern CMOS technology [17].

Comparator performance is another challenge in SAR ADC design, especially for high resolution ADC, where the noise performance is of great importance. For traditional voltage-domain comparator, every 1-bit resolution improvement in signal-to-noise ratio (SNR) requires four times power consumption of the comparator, which results in less energy-efficient. To improve the energy-efficiency, time-domain comparators are developed [18–20]. The edge-pursuit comparator proposed in [18] achieves good energy-efficiency as well as design flexibilities in terms of the input referred noise and offset. The VCO-based comparator in [19,20] employs the information provided by the comparator to achieve the meta-stability or adaptive bypassing window to improve the overall power-efficiency of SAR ADC.

To further improve the overall power-efficiency, different window techniques for SAR ADC are proposed [21–23]. The bypass window technique can reduce the overall power consumption and improve the differential non-linearity (DNL) and integral non-linearity (INL) performance for some output codes, but two comparators are needed to improve the window technique, which complicates the ADC design [21]. The window techniques in [22,23] predefined different windows to improve the DAC linearity or the energy-efficiency for signals with specific characteristic. However, the voltage-domain comparator will deteriorate the energy-efficiency, especially when the resolution increases.

In this paper, a SAR ADC model with skipping window is proposed. Its key feature is the utilization of a time-domain comparator information to implement the skipping window technique to improve the energy efficiency. The rest of this paper is organized as follows. Section 2 describes the structure of the proposed SAR ADC. The analysis of the skipping window is given in Section 3. Simulation results are given in Section 4. Section 5 concludes this paper.

2 Proposed Skipping-Window SAR ADC Structure

The proposed SAR ADC architecture with skipping-window is shown in Fig. 1, which consists of a capacitive DAC (CDAC), a SAR control logic and a time-domain comparator. The CDAC achieves sampling and the corresponding voltage change under the control of the SAR control logic, and the output voltage of the CDAC is feed to the input of the time-domain comparator. The time-domain comparator will provide both the polarity information and the amount information of the CDAC output voltage to the SAR control logic to finish the conversion process.

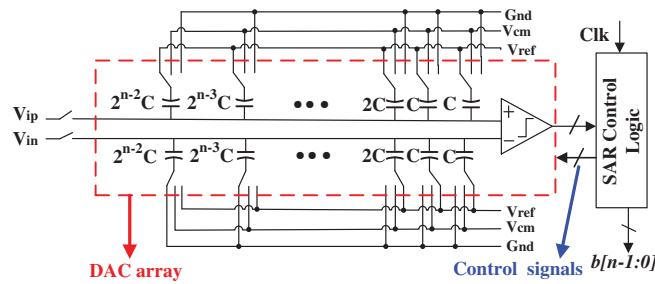


Figure 1: The proposed n-bit SAR ADC architecture

2.1 Analysis of the Proposed Time-Domain Comparator

The proposed time-domain comparator is illustrated in Fig. 2, which is composed of delay cells, two NAND gates, two D-flip-flop register based phase detector and a counter. The operation principle is based on the edge pursuing of two edges originating from two NAND gates similar to [18]. Two flip-flop based register based phase detectors are employed here to judge the polarity of the input. The counter is used to obtain the amount information of the input, which will be used to indicate whether the input is in the predefined window.

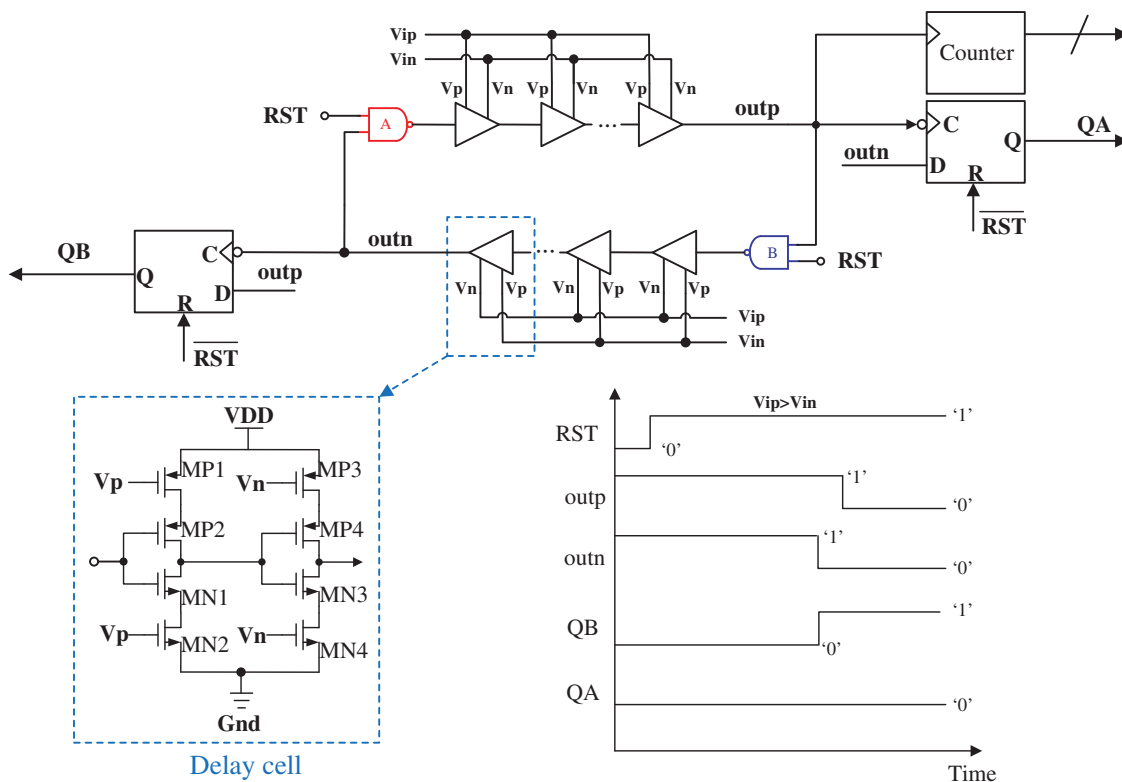


Figure 2: The schematic of the proposed time-domain comparator

Fig. 3 shows the operation principle of the comparator. When RST signal is logic low, the comparator is in reset state. Once RST changes from logic low to logic high, two propagating edges are injected into the oscillator, and travel through the delay cells. The oscillation will stop when one edge overtakes the other one. Fig. 3 illustrates the cases when V_{ip} is larger than V_{in} but with different amounts. When the voltage difference is small, the two propagating edges have a similar travel speed, and the cycles needed to arrive a decision automatically increase as Fig. 3 shows. On the other hand, if the voltage difference is large, the oscillation will stop very quickly, which inherently reduce the dynamic power consumption. In both cases, $outp$ will settle to 1 ($outn$ will settle to 0 in these cases), which indicates V_{ip} is larger than V_{in} . Moreover, the oscillation cycles, which is recorded by the counter, can be further utilized to detect the input voltage difference, which facilitates the SAR control logic to improve the whole energy-efficiency of the SAR ADC.

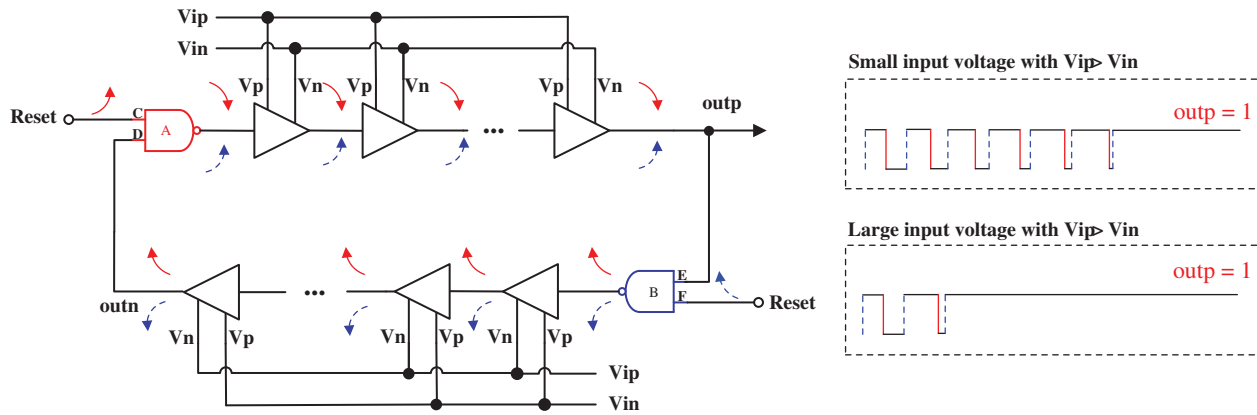


Figure 3: Operation principle of the proposed comparator

The noise root mean square (rms) level σ_v of the input-referred voltage and the input-referred offset voltage V_{OS_N} of the comparator can be expressed as [18]:

$$\sigma_v = \frac{\pi}{\sqrt{3}} f_0 \frac{kT}{I} \left(\frac{2}{V_{OV}} (\gamma_N + \gamma_P) + \frac{2}{V_{DD}} \right) V_{OV}, \quad (1)$$

$$V_{OS_N} = \frac{1}{\sqrt{N}} \cdot V_{OS}, \quad (2)$$

where f_0 is the oscillation frequency, k is the Boltzmann constant, T is the absolute temperature, I is the current-limiting current, V_{OV} is the overdrive voltage of the current-limiting transistors, V_{DD} is the power supply, V_{OS} is the input-referred offset voltage for one delay cell, γ_N and γ_P is the body-effect coefficients of NMOS and PMOS transistors respectively, and N is the number of the delay cell. From Eq. (1), the input-referred noise of the comparator is proportional to f_0/I , which is inversely proportional to the capacitor load of the oscillator. Thus, the input-referred noise can be easily tuned by adjust the MOS transistor size or the stages of the delay cell.

2.2 Working Principle of the Skipping-Window

Fig. 4 illustrates the working principle window of the skipping-window. When the SAR ADC powers on, the top plates and the bottom plates of the DAC array are all connected to V_{cm} . Then the control logic changes the connections of the bottom plates in order to generate the window voltage V_{win} . After the DAC settles, the comparator starts to work and the counter number N_{win} under V_{win} will be recorded. N_{win} will be utilized to indicate whether the input voltage falls into the skipping window during the SAR conversion. A SAR conversion will start after the V_{win} is set. After the sampling process, the SAR control logic set the current conversion cycle $i = 1$ and the time-domain comparator compares the DAC output voltages. If the voltage difference is larger than the window voltage V_{win} , the SAR control logic will perform the normal SAR conversion cycle by cycle; otherwise, the control logic will judge whether the current conversion cycle i is less than the skipping window cycle P_{win} ; if $i < P_{win}$, the control logic sets $i = P_{win}$, and perform the rest conversion cycles. Once $i \geq P_{win}$, the control logic will perform the normal conversion.

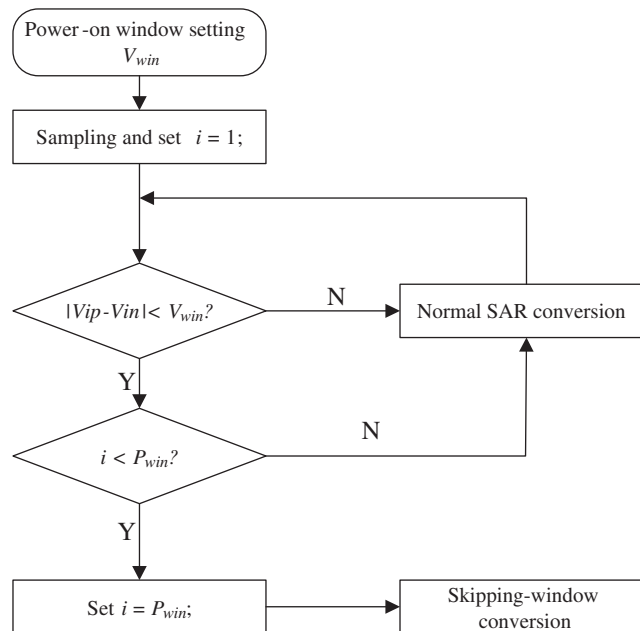


Figure 4: Illustration of the proposed skipping window

Fig. 5 shows the conversion process of a 10-bit SAR ADC model with $V_{win} = 64$ LSBs. The most significant bit (MSB) cycle is denoted as phase 9, and the least significant bit (LSB) cycle is phase 0. Fig. 5a is a normal conversion process and Fig. 5b is a skipping window conversion process. In Fig. 5a, the input voltage difference is larger than V_{win} at phase 6, where phase 6 corresponds to the window of 64 LSBs. Thus, no window is skipped for this case. In Fig. 5b, the input falls into the window V_{win} at phase 8, the next conversion cycle will skip to phase 5 directly, and two comparison cycles are saved. Thus, when the skipping window triggers, the conversion cycles will reduce, which in turn helps to improve the energy efficiency of the SAR ADC as well as the conversion speed and linearity.

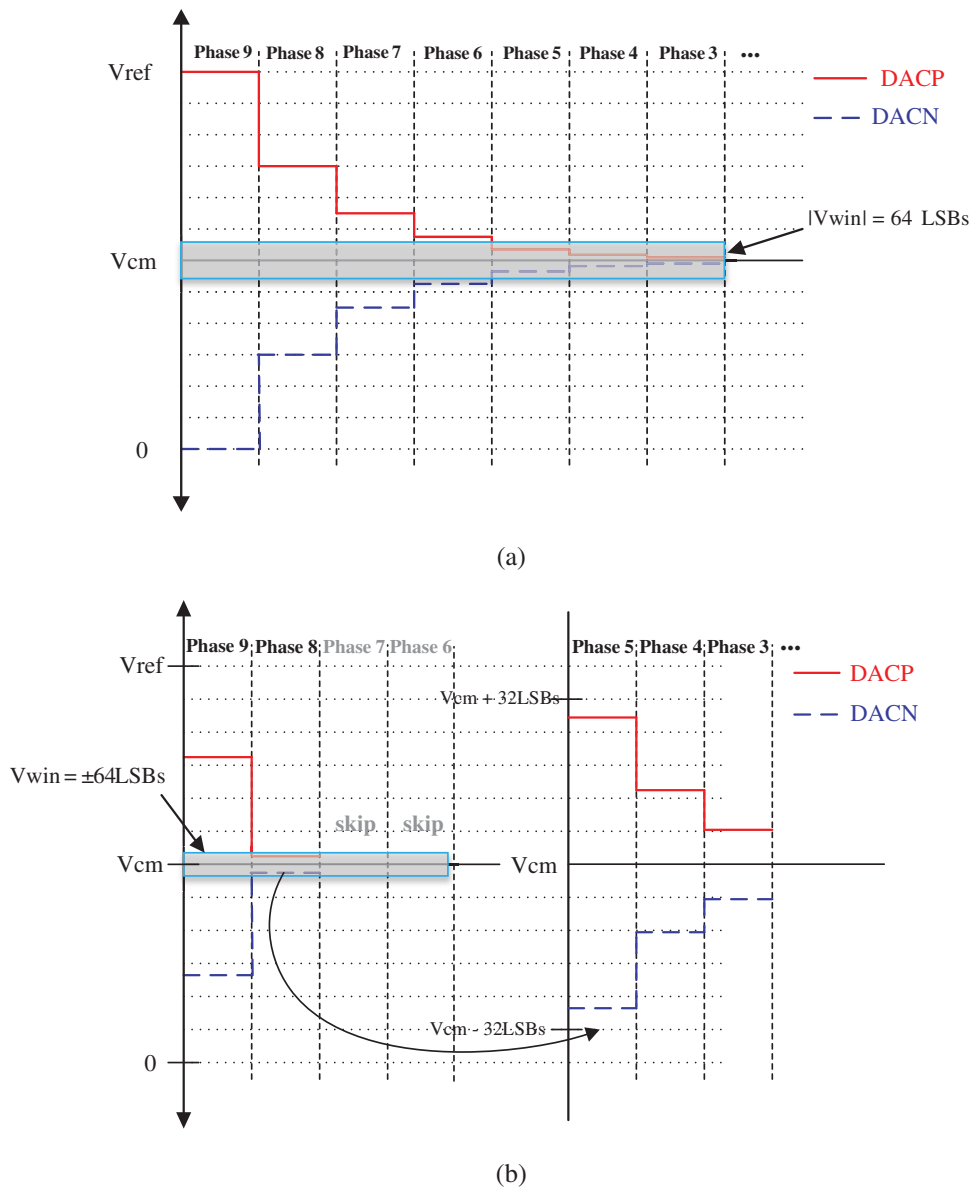


Figure 5: Illustration of the skipping-window scheme with $V_{win} = 64 \text{ LSBs}$ for a 10-bit SAR ADC. (a) Normal conversion. (b) Skipping window conversion

2.3 DAC Switching Procedure

The DAC switching scheme employed here is similar to that used in [14]. No additional switch or capacitor is needed. The skipping window technique is realized by the control logic according to the information provided by the comparator. Fig. 6 gives an example of the proposed skipping size with a window size of 64 LSBs. During the sampling phase, the input is connected to the top plates, and the bottom plates of the DAC array are all connected to the common-mode voltage V_{cm} , which is represented by '1/2' in Fig. 6. Once the sampling phase is finished, the sampling switches are turned off and the first comparison cycle is carried out directly. According to the comparison results, the control logic judges whether the input difference is less than V_{win} .

If $|V_{ip} - V_{in}| < V_{win}$, it means the input voltage is within the voltage window. Under this case, the skipping step is triggered. If $V_{ip} > V_{in}$, the bottom plates of C_5 in the DACp and DACn are connected to '0' and '1', respectively, where '0' represents GND and '1' stands for VDD, and three phases are skipped. If $V_{ip} < V_{in}$, the switching procedure is just opposite to that of $V_{ip} > V_{in}$ as the branch B shows in Fig. 6. However, if $|V_{ip} - V_{in}| > V_{win}$, the skipping procedure is not triggered, and normal conversion process is performed as branches C and D show. It should be noted that, whenever the input voltage is less than V_{win} before phase 6, the skipping procedure will be triggered, which is different from the incremental algorithm in [17].

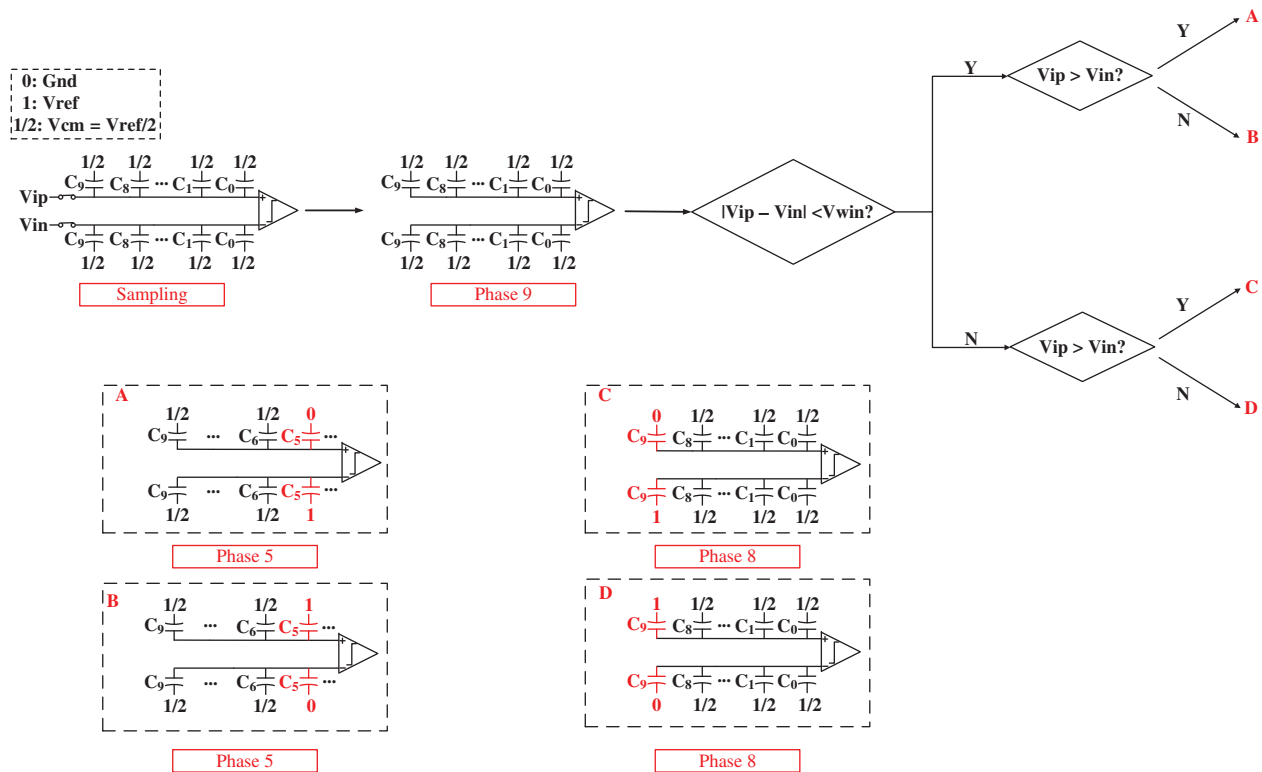


Figure 6: Switching procedure of the DAC with 64 LSBs judge window

3 Analysis of the Skipping Window

3.1 Conversion Cycle Saving for Different Window Size

To prove the efficiency of the proposed skipping window technique when the input falls in the predefined window voltage V_{win} , different window voltages are defined to verify the conversion cycle saving. During simulations, a 10-bit SAR ADC model is used. Fig. 7 shows the impact of skipping window size on the percentage of the triggered input. For normal SAR conversion with no skipping window size, all the input will carry out the full conversion cycles, and percentage of the triggered input is 0. When the skipping window size is set to 256 LSBs, the percentage of a full scale input fallen into the skipping window comes to 50%, which can improve the overall

energy efficiency of the SAR ADC significantly. When the skipping window size is reduced to 2 LSBs, the percentage is improved to about 99.61%.

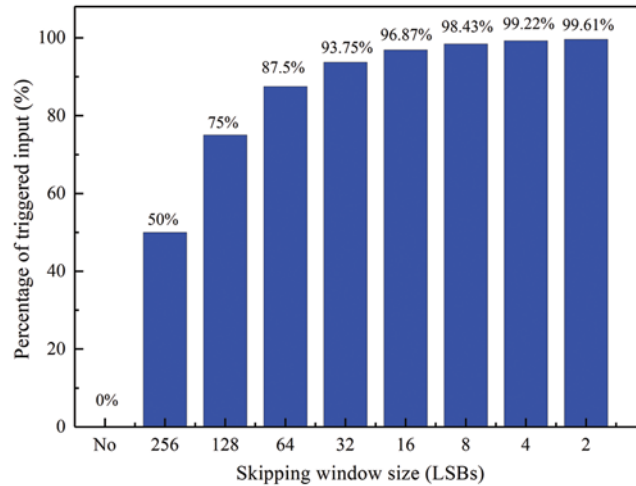


Figure 7: The impact of skipping window size on the percentage of triggered input

3.2 DAC Switching Energy Under Different Window Size

As described in Section 2.2, a large voltage range of the full scale input can fall in the skipping window zone if V_{win} is small. However, when V_{win} is small, the first MSB cycles can be skipped is less, which results in less energy efficiency of DAC. In order to evaluate the effect of the skipping window size on the DAC switching energy, a 10-bit SAR ADC model with the merged capacitor switching (MCS) scheme in [14] is employed. Fig. 8 shows the DAC switching energy under different skipping window size. It is clearly that when the skipping window size is large, the DAC consumes less switching energy than those with small skipping window sizes. This is because when the window size is large, most MSB cycles can be skipped. As the first few MSB conversion cycles occupies a large amount of the overall DAC switching energy, when the window size is large, the probability of the first few MSB conversion cycles will be skipped is high.

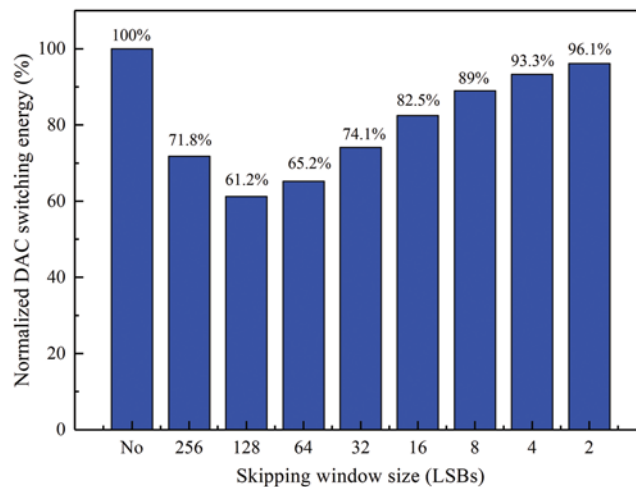


Figure 8: The impact of skipping window size on DAC switching energy

3.3 Overall Power Saving for Different Window Size

In SAR ADC, most of the power is consumed by three main building blocks, including comparator, DAC capacitor arrays and control logic. Since the DAC switching energy is not the same for different cycles during a conversion, the energy saving with different window size can be evaluated by supposing that each output code has the same probability, and the average DAC switching energy is denoted as E_{DAC} . For simplicity, we assume that the power consumption for the comparator E_{comp} and the control logic E_{dig} do not change for each bit-cycle.

For a normal conversion cycle, the power consumption for the comparator and the control logic are $n \cdot E_{comp}$ and $n \cdot E_{dig}$ for a n -bit SAR ADC, respectively. Assuming that the k -th cycle corresponds to the skipping window, and the corresponding size can be expressed as 2^{n-k} LSBs. According to the skipping window working principle in Section 2.3, if the current conversion cycle i is less than k and the input voltage is small than the window voltage V_{win} , the cycles between i and k will be skipped. In this circumstance, the power consumed by comparator and control logic can be expressed as

$$E_{comp,win} = (n - k + i) \cdot E_{comp} \quad (3)$$

$$E_{dig,win} = (n - k + i) \cdot E_{dig} \quad (4)$$

where $E_{comp,win}$ and $E_{dig,win}$ are the total power consumption of comparator and the control logic respectively when the skipping step is triggered. For the DAC power consumption, it is very complex to give an exact equation, and the simulation is used to evaluate the power saving of the skipping window as Fig. 8 shows. Fig. 9 shows the bit-cycles against output code under different window size for a 10-bit SAR ADC. The bit-cycle saving increases when the window size decreases, which can save the power consumption of the comparator and the control logic of the conversion cycle and accelerate the conversion speed. However, the DAC energy efficiency will reduce with the decreased window.

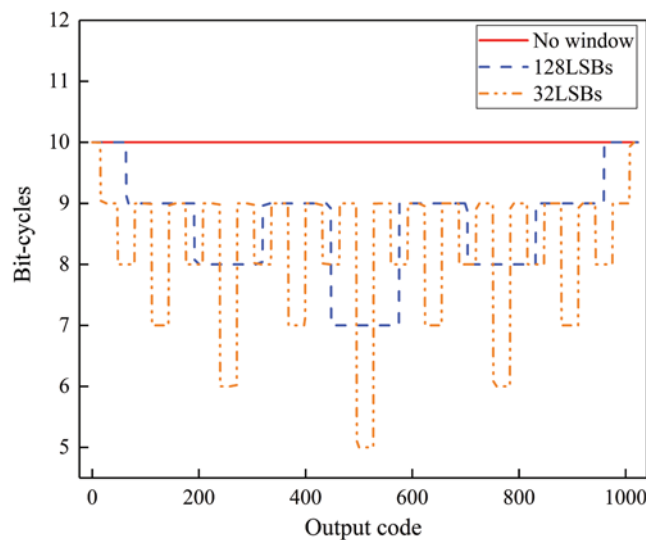


Figure 9: Bit-cycles against output code under different window size

4 Simulation Results

In order to evaluate the performance of the proposed skipping window technique, a 10-bit SAR ADC model is used. During simulations, the power consumption of the comparator and the control logic is assumed unchanged for each bit-cycle. Fig. 10 shows the switching energy against the output under different window size. The proposed skipping window technique can improve the DAC switching energy effectively. When the window size is 128 LSBs, the DAC energy saving is 38.8% compared to that of with no window.

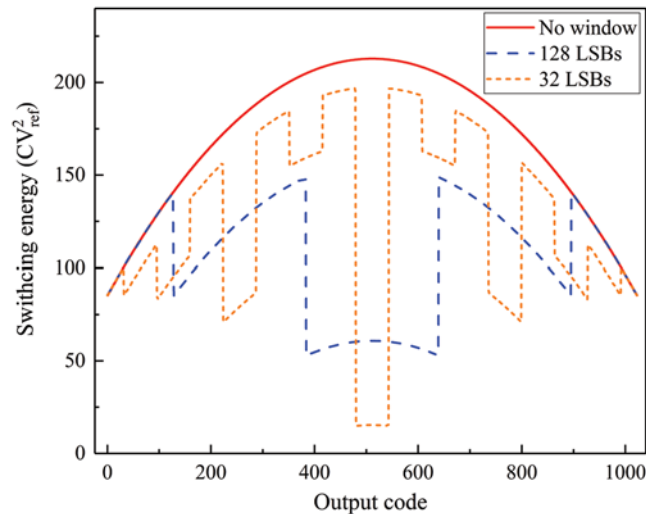


Figure 10: Switching energy against output code under different window size

Fig. 11 shows the static performance of the SAR ADC under different window size. The skipping-window technique can reduce the non-linearity of the DAC effectively, that is because the skipping process triggered by the window can reduce the accumulated error caused by the capacitor mismatch. Tab. 1 summarizes the power savings under different window size. Here, it is assumed that each output code has the same probability, the power consumption of the comparator and the control logic is 70% and the DAC occupies the rest 30% of the whole SAR ADC. For a 10-bit SAR ADC, there are 1024 output codes, and each code needs 10 bit-cycles for traditional SAR conversion, and 10240 bit-cycles are required in total. The bit-cycles saving is the saved bit-cycles over the total bit-cycles. Although a small window size can save more bit-cycles, the DAC energy saving is less, which results in less energy-efficient for the whole SAR ADC. For the DAC energy saving, 128 LSBs window size is the most energy-efficient one. When it comes to the overall power saving, the window size with 64 LSBs is the best choice. It should be noted that the MCS scheme in [14] is employed and 30% power consumption for the DAC is assumed during simulations. If the DAC switching scheme or the power consumption for the DAC varies, the optimized window size may be different.

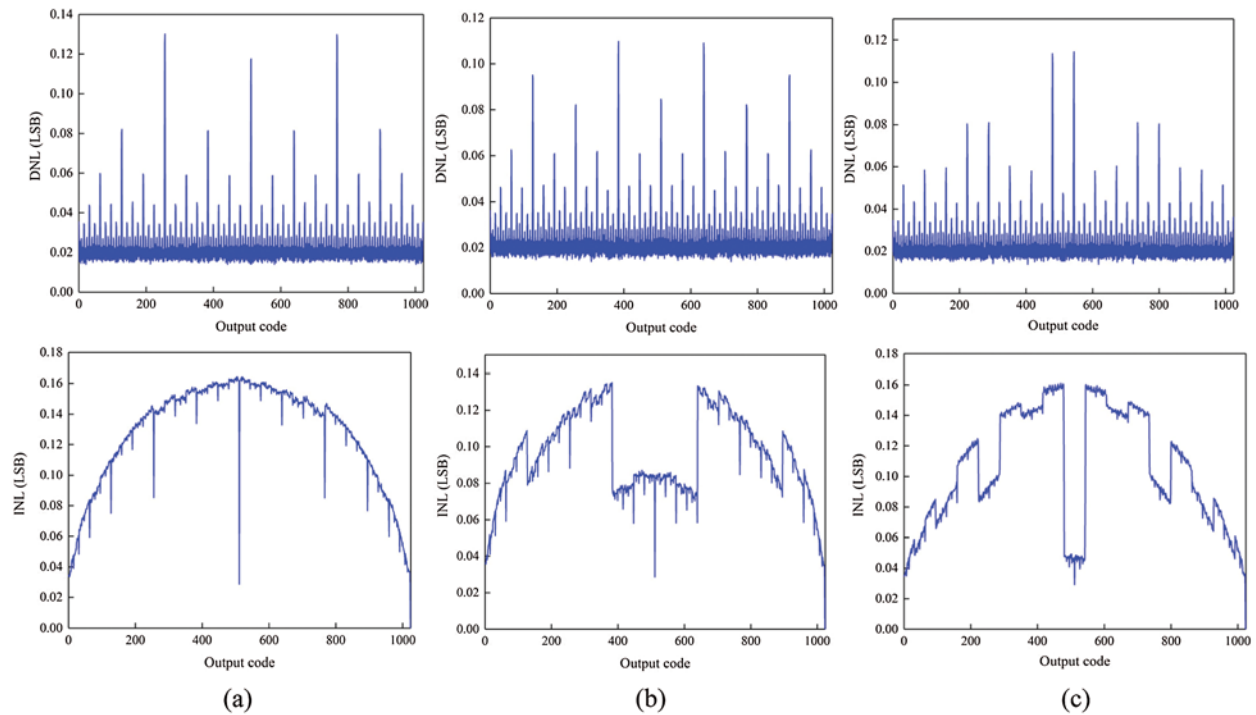


Figure 11: Static performance with different window size: (a) No window, (b) 128 LSBs, (c) 32 LSBs

Table 1: Power savings under different window size

	256 LSBs	128 LSBs	64 LSBs	32 LSBs	16 LSBs	8 LSBs	4 LSBs	2 LSBs
Bit-cycles saving (%)	5	10	13.75	16.25	17.81	18.75	19.3	19.6
DAC energy saving (%)	28.2	38.8	34.8	25.9	17.5	11	6.7	3.9
Overall power saving (%)	11.96	18.64	20.065	19.145	17.717	16.425	15.52	14.89

5 Conclusion

A SAR ADC with skipping window is presented. The proposed comparator provides not only the polarity information of the input, but also the amount of the input difference, which is employed to indicate the window voltage. The window voltage can be easily adjusted by connecting different DAC capacitors to corresponding reference voltages. The impacts on the DAC switching power and the conversion cycles are analyzed. Simulation results show that the proposed skipping window can effectively improve the overall energy-efficiency of SAR ADC.

Funding Statement: This work was supported partly by the National Natural Science Foundation of China under Grant No. 61704015, and the General program of Chongqing Natural Science Foundation (a special program for the fundamental and frontier research) under Grant No. cstc2019jcyj-msxmX0108.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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