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CNTFET Based Grounded Active Inductor for Broadband Applications

Muhammad I. Masud[1,2,*], Nasir Shaikh-Husin[2], Iqbal A. Khan[1] and Abu K. Bin A'Ain[2]

[1]Department of Electrical Engineering, Umm Al Qura University, Makkah, 21955, Saudi Arabia
[2]School of Electrical Engineering, Faculty of Engineering, Universiti Teknologi Malaysia, Johor Bahru, 81310, Johor, Malaysia
*Corresponding Author: Muhammad I. Masud. Email: mimasud@uqu.edu.sa
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Abstract: A new carbon nanotube field effect transistor (CNTFET) based grounded active inductor (GAI) circuit is presented in this work. The suggested GAI offers a tunable inductance with a very wide inductive bandwidth, high quality factor (QF) and low power dissipation. The tunability of the realized circuit is achieved through CNTFET based varactor. The proposed topology shows inductive behavior in the frequency range of 0.1–101 GHz and achieves to a maximum QF of 9125. The GAI operates at 0.7 V with 0.337 mW of power consumption. To demonstrate the performance of GAI, a broadband low noise amplifier (LNA) circuit is designed by utilizing the GAI based input matching-network. The realized LNA provides high frequency bandwidth (17.5–57 GHz), low noise figure (<3 dB) and occupies less space due to absence of any spiral inductor. Moreover, it exhibits a flat forward gain of 15.9 ± 0.9 dB, a reverse isolation less than −63 dB and input return loss less than −10 dB over the entire frequency bandwidth. The proposed CNTFET based GAI and LNA circuits are designed and verified by using HSPICE simulations with Stanford CNTFET model at 16 nm technology node.

Keywords: Active inductor; gyrator-C; CNTFET; quality factor; self-resonance frequency

1 Introduction

Inductors are crucial components of many high frequency analog signal processing (ASP) circuits. They are utilized in LNAs, voltage-controlled oscillators, filters, frequency dividers, impedance matching-networks and phase shifters to name a few [1]. However, their implementation in integrated circuits (ICs) is a challenging task. An on-chip spiral inductor dominates the die area of the IC, resulting in higher fabrication cost and also presents several disadvantages such as low QF, fixed inductance value and incompatibility with semiconductor fabrication process [2,3]. Limitations of spiral on-chip inductor motivates IC designers to opt for active-circuitry for synthesizing the integrated inductors. Comparatively to spiral inductor, an active inductor (AI) offers high tunable inductance, high QF and it requires smaller area [4]. However, AIs consume large power and introduce noise [5].

From technical literature, several GAI topologies have been reported by employing high performance active building blocks (ABBs) like extra-X current controlled current conveyor [6], differential difference current conveyor [7], current feedback operational amplifier [8], current differencing buffered amplifier [9], voltage differencing inverting buffered amplifier [10], inverting voltage buffer [11], dual-X current conveyor transconductance amplifier [12] and four terminal floating nullor transconductance amplifier [13]. However, high frequency performance of these GAI topologies is limited due to low self-resonance frequency (SRF), large number of active and passive devices, high power consumption and large chip area.

Several gyrator-C based compact GAI topologies, utilizing positive transconductance element (PTE) and negative transconductance element (NTE) as an ABB can be found in the technical literature [1–3,5,14–22]. However, each of these GAI topologies offers a few desirable specifications such as low power dissipation, wide inductance bandwidth, high QF, large tunable inductance, low noise and ability to work on low voltages. Although most AI circuit topologies presented to date are compact and achieve acceptably larger QF than its spiral counterpart, their application in low voltage, low power broadband ASP modules has been limited because of their narrow inductive bandwidth. As a result, to the best of authors knowledge, AI circuit topology has so far not been utilized in high frequency applications (>11 GHz) and wideband (>7 GHz bandwidth) ASP modules [3]. This comparatively limited inductive bandwidth ultimately reduced their feasibility for the design of broadband high frequency ASP modules.

It is to be noted that GAI topologies proposed in the technical literature [1–3,5–22] are based on bulk semiconductor technology. However, this technology faces numerous challenges below 22 nm technology node [23]. The issues include high field effects, short channel control, increased leakage, boron penetration, polysilicon depletion, direct gate tunneling current and lithographic limitations [24–27]. Therefore, it is extremely imperative for IC designers to explore new materials and devices for below 22 nm node, that equally works well to keep Moore's law alive [23].

To find replacements for CMOS technology, many devices and techniques are being introduced and evaluated by researchers such as double gate field effect transistors (FETs), single electron transistor, fin FETs and CNTFET [25]. Among these solutions, the CNTFET has tremendous potential to further continue the feature length down-scaling and extend Moore's law, due to its near ballistic transport of charge carriers, large thermal conductivity, higher cutoff frequency, smaller size, fast switching speed and low parasitic capacitances [26]. These excellent CNTFET features lead it as a suitable candidate for multi GHz frequency applications. Since CNTFET introduction as an alternative to MOSFET, limited studies on CNTFET based AI has been carried out [27]. However, the reported CNTFET based GAI topology utilizes large number of active and passive devices and suffers from low SRF, large chip area and high power dissipation.

In this work, a wide tunable CNTFET based GAI circuit is presented. The realized GAI circuit uses recently proposed PTE along with NTE as an ABB and one CNTFET varactor [28]. Tunability of GAI is achieved through the CNTFET varactor. The proposed GAI circuit enjoys higher tunable inductance magnitude over a very wide frequency band along with high QF, high SRF and low power dissipation. To evaluate the performance of the GAI topology, the proposed circuit is utilized in LNA. The GAI based LNA provides high frequency bandwidth, high gain, low noise figure (NF) and low power dissipation. The realized CNTFET based GAI has been studied in detail and the design is validated with HSPICE simulations by utilizing Stanford model [29].

Subsequent sections are organized as follows. Section 2 discusses CNTFET in detail. The GAI circuit description is given in Section 3. Simulation results of the realized CNTFET based GAI are

elaborated in Section 4. Comparison of the proposed GAI with other topologies is presented in Section 5. The application of GAI is demonstrated in Section 6. Lastly, the conclusion is provided in Section 7.

2 Carbon Nanotube Field Effect Transistor

Carbon nanotube (CNT), an allotrope of carbon, are graphite cylindrical sheets (GCS) which are rolled into cylindrical shape with diameter in the range of 1 to 50 nm and length of a few micrometers. CNTs are considered as the most attractive nanomaterial for future ASP applications due to its extraordinary electrical, chemical, mechanical, optoelectronics, and thermal properties [23]. CNTFET is an important application of CNT. It is realized by replacing the MOSFET conventional channel with an array of isolated and aligned single wall CNTs. The CNTs behave as the medium of conduction between the drain and source terminals as shown in Fig. 1. Like MOSFET, CNTFET also works as a voltage controlled active device. The CNTFET channel current is controlled through gate terminal voltage. CNTFET gate is coupled capacitively with the underneath channel that utilizes one or more CNTs [24]. In comparison to MOSFET, CNTFET enjoys numerous outstanding advantages like higher temperature resilience, larger transconductance, larger driving current, one-dimensional ballistic transport capability, near ideal subthreshold slope and lower value of intrinsic capacitances [25,26].

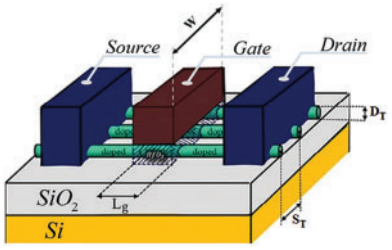


Figure 1: CNTFET 3D view

The geometric parameters S_T, D_T, N_T and W are the inter-CNT pitch, CNT diameter, number of channels and the transistor gate width respectively. These parameters are important for performance optimization of CNTFET. The parameter D_T and threshold voltage (V_{th}) of a single wall CNT are given by following equations [30].

$$D_T = \frac{a_c}{\pi}\sqrt{(n^2 + m^2 + nm} \tag{1}$$

$$V_{th} = \frac{E_g}{2q} = \frac{0.42}{D_T}(V) \tag{2}$$

where n and m are the chiral vectors, a_c is the graphene lattice constant, E_g is the band gap energy and q is the electron charge. The CNTFET gate width is given by following equation [24]:

$$W = D_T + S_T(N_T - 1) \tag{3}$$

Thus, the width of CNTFET can be adjusted by selecting S_T, D_T and N_T values to optimize the circuit performance.

3 GAI Circuit Description

The proposed GAI topology with its equivalent RLC circuit is shown in Fig. 2. It is based on gyrator-C topology. CNTFETs T_1 and T_4 form the NTE and CNTFETs T_2, T_3, T_5 and T_6 constitute the PTE [28]. The PTE utilizes CNTFETs T_2 and T_5 as an inverting voltage buffer (IVB) [24]. The varactor C_{var} utilized in Fig. 2 is based on a single CNTFET, as shown in Fig. 3 [25]. The CNTFET based varactor drain and source are tied together and then connected to control voltage V_{tune}. The varactor capacitance C_{var} can be controlled by varying V_{tune}. Fig. 4 demonstrate the small signal equivalent circuit of the GAI. In Fig. 4, each CNTFET is presented by g_{mi}, g_{dsi} and C_{gsi} which are the transconductance, output conductance and gate to source capacitance of the *i-th* transistor respectively. For simplicity, C_{gd} is neglected (since $C_{gd} << C_{gs}$).

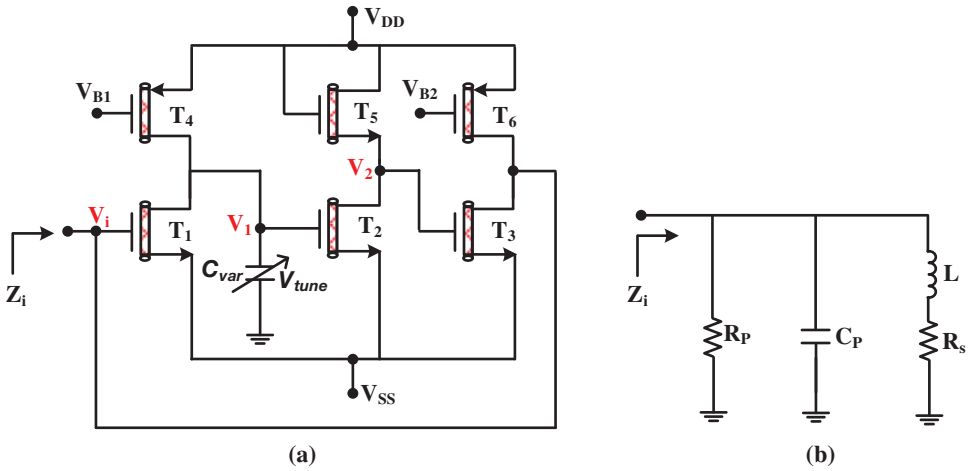


Figure 2: Active inductor (a) proposed circuit (b) equivalent RLC circuit

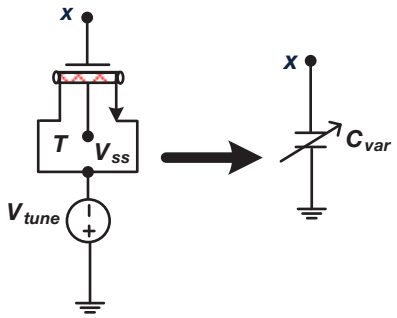


Figure 3: Varactor transistor level realization with its symbol

By using the small signal equivalent model of Fig. 4, the input admittance ($Y_i = 1/Zi = I_i/V_i$) can be found as.

$$Y_i(s) = G_p + sC_p + \frac{1}{(R_s + sL)} = (g_{ds3} + g_{ds6}) + sC_{gs1} + \left(\frac{1}{(\frac{\beta}{\alpha} - \frac{\omega^2 \rho}{\alpha}) + s\frac{(\gamma + \delta)}{\alpha}} \right) \tag{4}$$

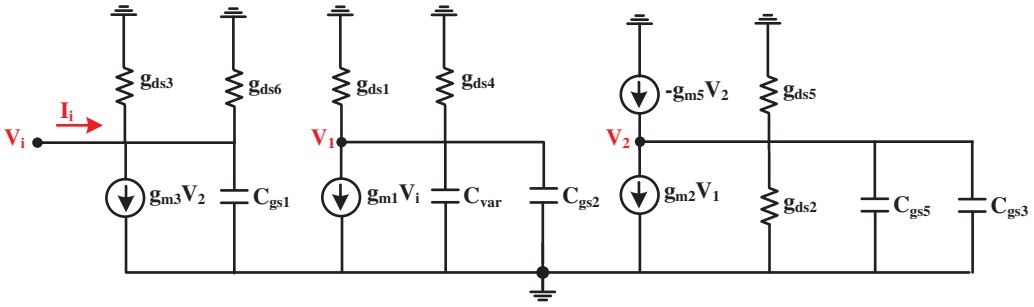


Figure 4: GAI small signal equivalent circuit

where the parameter α, β, γ, δ and ρ are given as follows:

$$\alpha = g_{m1}g_{m2}g_{m3} \tag{5}$$

$$\beta = (g_{m5} + g_{ds2} + g_{ds5}) * (g_{ds1} + g_{ds4}) \tag{6}$$

$$\gamma = (C_{gs3} + C_{gs5}) * (g_{ds1} + g_{ds4}) \tag{7}$$

$$\delta = (C_{\text{var}} + C_{gs2}) * (g_{m5} + g_{ds2} + g_{ds5}) \tag{8}$$

$$\rho = (C_{gs3} + C_{gs5}) * (C_{\text{var}} + C_{gs2}) \tag{9}$$

By considering $g_{m5} >> g_{ds2}$, $g_{m5} >> g_{ds5}$, $g_{m5} >> g_{ds1}$, $g_{m5} >> g_{ds4}$, $C_{var} >> C_{gs3}$, and $C_{var} >> C_{gs5}$, the equivalent RLC circuit model components of Fig. 2b can be derived as:

$$G_p = \frac{1}{R_p} = (g_{ds3} + g_{ds6}) \tag{10}$$

$$C_p = C_{gs1} \tag{11}$$

$$R_s \approx \frac{g_{m5}(g_{ds1} + g_{ds4})}{g_{m1}g_{m2}g_{m3}} - \frac{\omega^2(C_{gs3} + C_{gs5}) * C_{\text{var}}}{g_{m1}g_{m2}g_{m3}} \tag{12}$$

$$L \approx \frac{(C_{\text{var}} + C_{gs2}) * g_{m5}}{g_{m1}g_{m2}g_{m3}} \tag{13}$$

It can be seen from Eq. (13) that inductance of GAI can be controlled by adjusting the capacitance of CNTFET varactor. Thus, increasing the value of V_{tune} of CNTFET varactor, will increase the magnitude of inductance L. Moreover, the transconductance ratio of IVB (g_{m5}/g_{m2}), also plays a vital role in the improvement of inductance magnitude. The QF relation derived from the RLC equivalent circuit of Fig. 2 is given by:

$$QF = \left(\frac{\omega L}{R_s}\right) * \left(\frac{R_p}{R_s\left\{\left(\frac{\omega L}{R_s}\right)^2 + 1\right\} + R_p}\right) * \left(1 - \omega^2 LC_p - \frac{R_s{}^2 C_p}{L}\right) \tag{14}$$

The SRF of GAI which determine the circuit inductive behavior upper limit in frequency band can be written as:

$$SRF \approx \frac{1}{2\pi}\sqrt{\frac{g_{m1}g_{m2}g_{m3}}{C_{gs1} * (C_{\text{var}} + C_{gs2}) * g_{m5}}} \tag{15}$$

By analyzing Eqs. (13) and (15), it is seen that a tradeoff exists between the GAI inductance magnitude and SRF. With higher transconductance of CNTFET T_5, a significant increase in the inductance value can be achieved but the inductance bandwidth will shrink accordingly. The realized GAI utilizes few number of transistors in the main path of signal, which made it suitable for high frequency broadband applications. Moreover, the designed GAI is suitable for low voltage operation as it employs only two CNTFETs between its supply rails. In addition, it is suitable for integration due to absence of any external passive component.

4 GAI Design and Verification

The proposed GAI of Fig. 2 is designed and verified using HSPICE simulation tool with supply voltages $V_{DD} = 0.7$ V and $V_{SS} = -0.7$ V. All the transistors are modeled using Stanford CNTFET model with transistor parameters mentioned in Tab. 1. The diameter D_T is set to 3 nm for GAI design. Moreover, with constant pitch $S_T = 10$ nm, the major design factor of the CNTFET based GAI is the parameter N_T. In this regard, the transconductance ratio g_{m5}/g_{m2} is almost equal to N_{T5}/N_{T2}.

Table 1: The CNTFET parameters

Parameters	Description	Value
Fixed		
V	Supply voltage	±0.7 V
L_d/L_s	Doped CNTs source/drain side-length	16 nm
L_g	Physical length of channel	16 nm
High-K_{ox}	Dielectric material of top gate (Constant)	HfO_2 (16)
(n, m)	Chirality vector	(38, 0)
T_{ox}	Thickness of oxide	4 nm
L_{ceff}	The mean free path in intrinsic CNT	200 nm
L_{eff}	The mean free path in doped CNT	15 nm
E_{fo}	Fermi level of n^+ doped drain & source region	0.6 eV
S_T	Inter CNTs pitch	10 nm
K_{sub}	Bottom gate dielectric (constant)	SiO_2 (4)
Variable		
N_T	Number of CNT per CNTFET	-

The proposed topology is simulated using CNTFET parameters of Tab. 1 along with $N_{T1} = 5$, $N_{T2} = 5$, $N_{T3} = 5$, $N_{T4} = 5$, $N_{T5} = 30$, $N_{T6} = 5$ and $N_{T7} = 157$. Initially the varactor tuning voltage V_{tune} is set to −0.60 V. Figs. 5a and 5b show the magnitude and phase response of GAI input impedance. From Figs. 5a and 5b, a high SRF equivalent to 101 GHz is observed. Fig. 5c shows the GAI inductance plot. The inductance ranges from nearly 47.8 nH to 287.4 nH and can be adjusted to a set value for a specific frequency range. The AI circuit behavior is dominantly inductive in the frequency band, ranging from approximately 0.1 GHz to 101 GHz. The peak inductance value is found at 96.6 GHz. This wide inductive bandwidth makes the proposed GAI an attractive choice for broadband high

frequency applications. Fig. 5d shows the GAI QF plot. The maximum QF obtained is equivalent to 9125 at 16.6 GHz. This high QF is another advantage of the proposed work. The power dissipation is 0.337 mW. The realized GAI dissipates very small power, even at very high frequency of operation. The equivalent input referred noise for the circuit is 21.5 nV/$\sqrt{}$Hz, which is adequately a low value.

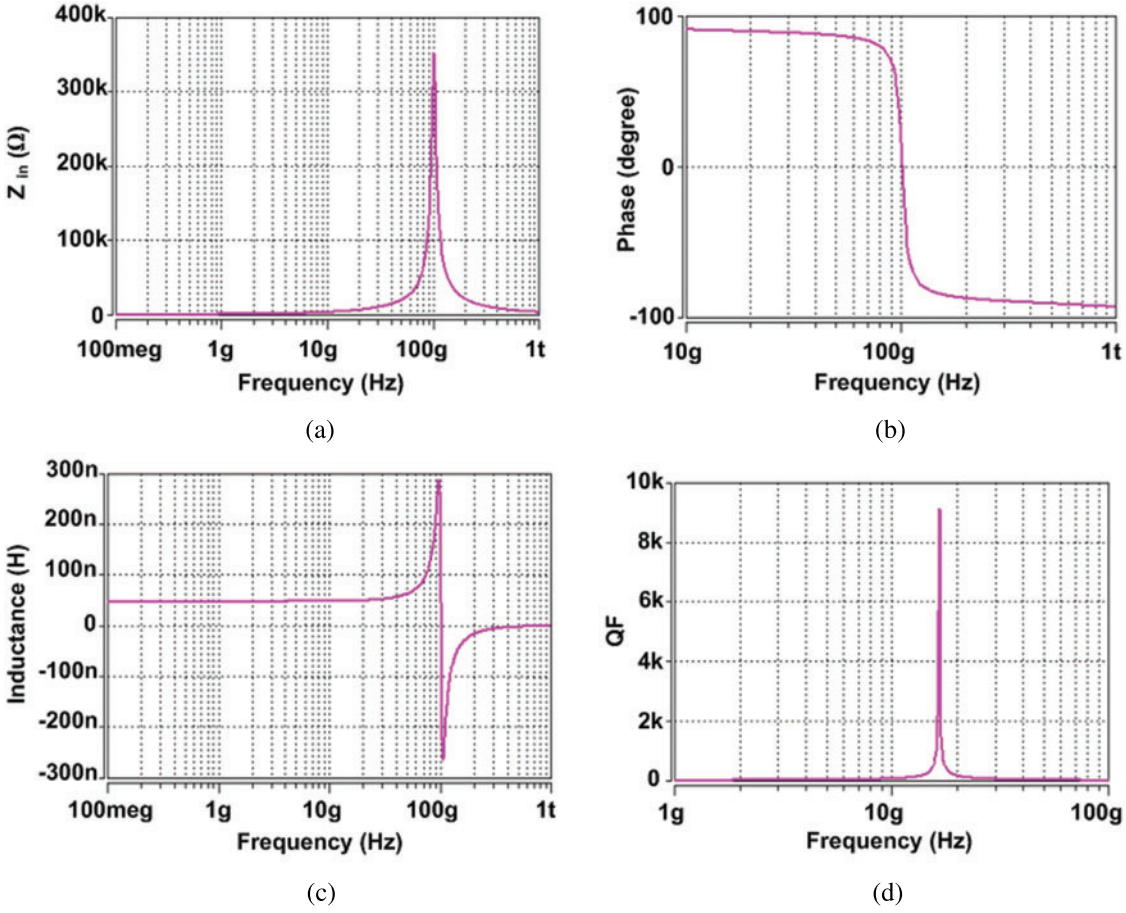


Figure 5: GAI frequency response (a) Z_{in} magnitude (b) Z_{in} phase (c) inductance (d) QF

The main criterion for selecting an AI for analog system design is its ability to tune to different resonant frequencies. As depicted by Eq. (13), the GAI inductance can be controlled by varying varactor capacitance C_{var}. To demonstrate the proposed GAI tunability feature, different tuning voltages V_{tune} are applied to the varactor. Fig. 6 shows the magnitude response of GAI input impedance, at different values of V_{tune}. It can be seen that the input impedance frequency band can be tuned to different frequencies by altering V_{tune}. The SRF are found as 101.2 GHz, 131.8 GHz, 160.3 GHz, 245.5 GHz, 319.9 GHz for V_{tune} equal to −0.60 V, −0.38 V, −0.35 V, −0.30 V, −0.15 V respectively. By varying the V_{tune} from −0.60 V to −0.15 V the GAI input impedance magnitude decreases from 351.7 kΩ to 34.4 kΩ. This tunable input impedance over a large frequency band makes the proposed work suitable for multi GHz ASP applications.

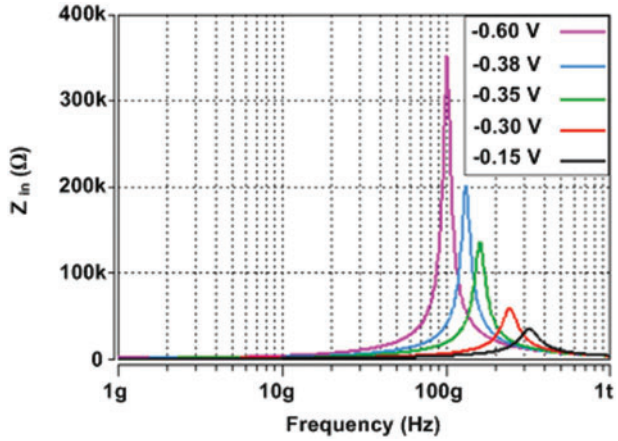


Figure 6: Frequency response of Z_{in} magnitude at different values of V_{tune}

Fig. 7 shows the frequency response of GAI inductance, at different values of V_{tune}. The maximum inductance is achieved at −0.60 V, where the inductance value varies in the range of 47.8 nH to 287.4 nH with a SRF of 101 GHz. The minimum inductance is achieved at −0.15 V, where the inductance value varies in the range of 4.4 nH to 9.6 nH with a SRF of 319.9 GHz. It can be seen that a tradeoff exists between the inductance magnitude and inductive bandwidth/SRF. Fig. 8a shows the variation of GAI inductance *vs.* varactor tuning voltage V_{tune} at a fixed frequency of 40 GHz. Fig. 8b demonstrates the variation of SRF versus V_{tune}. As discussed earlier, a trade-off exists between the inductive bandwidth/SRF and inductance magnitude, which is more obvious from Fig. 8.

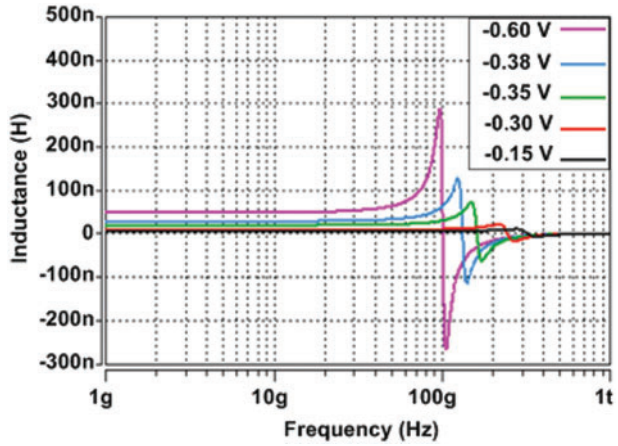
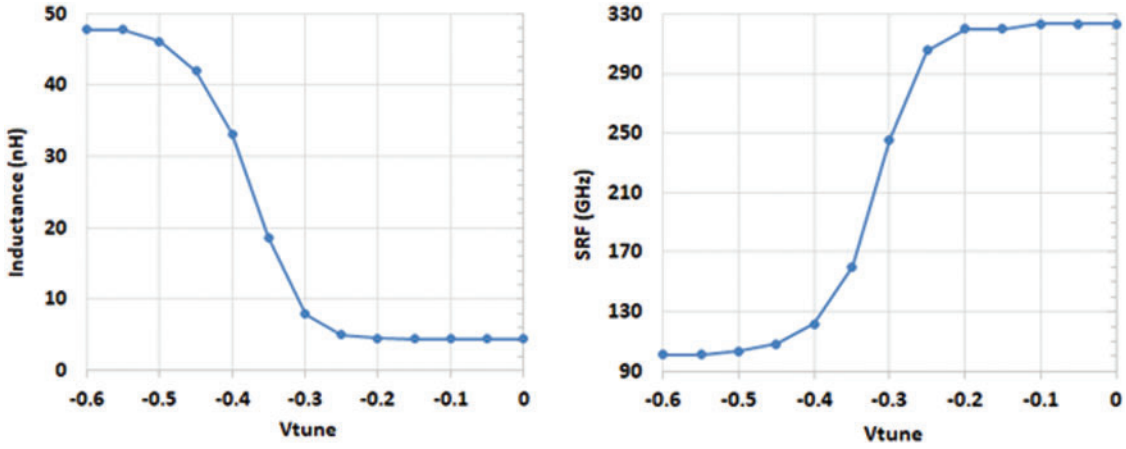


Figure 7: Frequency response of GAI inductance at different values of V_{tune}



(a) (b)

Figure 8: GAI (a) inductance versus V_{tune} (b) SRF versus V_{tune}

5 GAI Comparative Study

Tab. 2 summarizes a comparison of the realized GAI circuit with some other gyrator-C based AI topologies in the technical literature [1–2,5,14–22]. Except for the proposed topology, which is in CNTFET, the other GAI topologies are based on CMOS technology. For comparison, only GAI circuits suitable for multi-GHz ASP applications are included in Tab. 2. Limited works on CNTFET based GAI topology are available in the technical literature [27], however its frequency of operation is limited to MHz range. The GAI performance is compared for the characteristic's parameters inductive bandwidth, maximum inductance, maximum QF and power dissipation. Comparison results demonstrate that the realized GAI has maximum inductive bandwidth, highest QF, minimum power consumption, and large inductance. The inductive bandwidth of the proposed work is almost 9 times greater than [14]. The QF of the proposed work is almost 2 times greater than [22]. In comparison to [17], the proposed GAI shows 34% reduction in power dissipation.

Table 2: GAI performance comparison

Ref.	Inductive Bandwidth (GHz)	Inductance (nH)	QFmax @ Freq (GHZ)	Technology (nm)/ Voltage (V)	Inductance (nH)
[1]	0.3–7.32	38–144	3900@5.75	130/1.2	1
[2]	1–3.3	10–400	560@1.7	180/1.8	2.1
[5]	1.76–6.55	10.94–45	2581@2	130/1	1.32
[14]	0.3–11.3	216	2100@5.9	180/1.8	1
[15]	0.1–8.9	3–168	571@6.9	90/1	1.2
[16]	0.15–6.6	11–459	101	180/1.8	-
[17]	1.7–5.5	3.55–26	895@1.82	90/1	0.515
[18]	0.5–4	0.8–3.5	70@1.8	180/-	16
[19]	1.76–6.51	10.97–44	2565@2	130/1	1.32

(Continued)

Table 2: Continued

Ref.	Inductive Bandwidth (GHz)	Inductance (nH)	QFmax @ Freq (GHZ)	Technology (nm)/ Voltage (V)	Inductance (nH)
[20]	0.6–3.8	165	120@3	90/1.2	1.2
[21]	4	4–6	140	180/1	-
[22]	0–6.9	7.56	4406	180/1	2
This work	0.1–101	4.4–287.4	9125@16.6	16/0.7	0.337

Note: - Not available.

6 GAI Application

In this section, the application of the proposed CNTFET GAI is demonstrated. The proposed GAI is utilized in the dual negative feedback common gate (DNFCG) LNA topology [31]. For matching-network, LNA topologies usually utilize on chip passive spiral inductors. From Fig. 9a, it can be seen that spiral inductor L_{biase} is utilized by DNFCG LNA topology for matching. However, this inductor suffers from many drawbacks like low SRF, low QF, fixed and low inductance magnitude, larger chip area and incompatibility with standard CNTFET/CMOS technology. It is then most preferable to utilize AI instead of bulky spiral inductor, for reducing cost and size of LNAs.

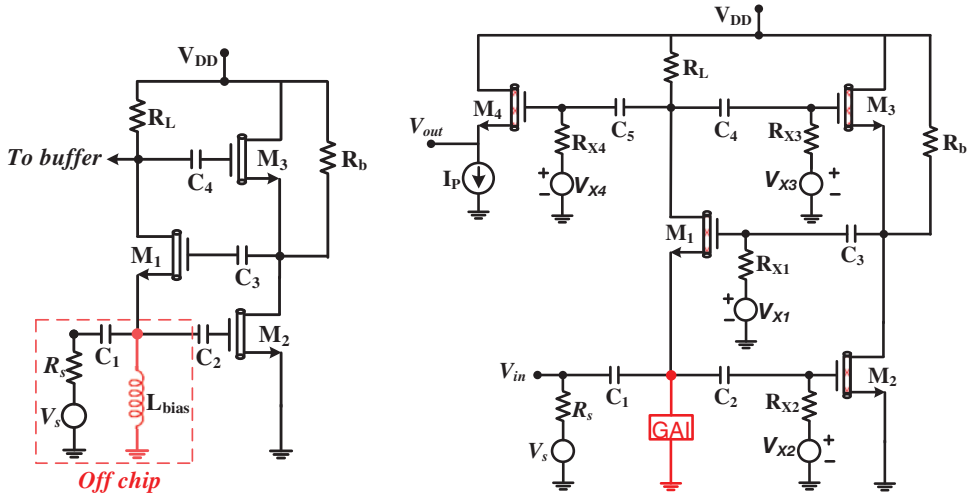


Figure 9: (a) DNFCG LNA [31] (b) GAI based DNFCG LNA

Fig. 9b shows the complete GAI based DNFCG LNA, where passive inductor L_{biase} of Fig. 9a is replaced with the proposed GAI circuit. The common gate impedance matching transistor M_1, amplifies the input and provides the main forward signal path. The common source transistor M_2 along with resistor R_b forms the inverting gain block between M_1 source and gate terminals and thus help in boosting the transconductance of M_1. Resistor R_b sets the loop gain and supplies the difference in bias current between the source follower transistor M_3 and M_2. The source follower transistor M_4 works as a buffer. The coupling capacitors C_1, C_2, C_3, C_4, C_5 and bias resistors R_{x1}, R_{x2}, R_{x3}, R_{x4} form the bias-network for the respective transistors. For proper operation of GAI based LNA, the zero

frequency-ωz and the pole frequency-ωp of the utilized GAI, should be equal to the lowest and highest operating frequency, respectively.

The input impedance of Fig. 9 can be derived as:

$$Z_{in} = \frac{1 + [g_{m3}R_b(g_{m1}R_L + 1)]}{g_{m1}(g_{m2}R_b + g_{m3}R_b + 1)} // sL // \frac{1}{sC_p} \tag{16}$$

where C_p is the total parasitic capacitance at the input due to transistor M_1 and M_2. The input matching-network is thus a parallel resonance, where GAI can be used to cancel the capacitive effects at the input-terminal. Thus, the parasitic C_p is absorbed into the LC-network and the imaginary part of Z_{in} is insignificant within the intended bandwidth [3,31]. The voltage gain A can be calculated as.

$$A = \frac{g_{m1}R_L}{2}\left(\frac{\frac{1}{R_b} + g_{m2} + g_{m3}}{\frac{1}{R_b} + g_{m1}g_{m3}R_L + g_{m3}}\right) \tag{17}$$

By assuming $g_{m3} << g_{m2}$ and $g_{m3}R_b(g_{m1}R_L + 1) << 1$, Eq. (17) can be reduced to:

$$A = \frac{g_{m1}R_L}{2}(1 + g_{m2}R_b) \tag{18}$$

The total NF is given by following relation.

$$NF = 1 + \frac{H_{m1}}{(1+A)} + \frac{H_{m2}A^2}{(1+A)^2 g_{m2}R_s} + \frac{H_{m3}A^2\left(\frac{g_{m3}}{g_{m2}}\right)}{(1+A)^2 g_{m2}R_s} + \frac{R_b}{(1+A)^2 R_s} + \frac{Rs}{R_L} \tag{19}$$

where H_{mi} are the CNTFET coefficients with magnitude less than one [30]. The LNA circuit with gain much greater than unity will reduce the noise impact of R_b and transistors M_1, M_2, M_3, M_4 on the NF. Tab. 3 shows the important design parameters for DNFCG LNA. It is to be noted that the N_{T2} of Common source transistor M_2 is set to sufficiently greater than N_{T3} to fulfill the primary assumptions $[g_{m3}R_b(g_{m1}R_L + 1)] << 1$ and $g_{m3} << g_{m2}$. For GAI the CNTFET parameters of Tab. 1 are used along with $N_{T7} = 157$, $N_{Ti} = 10$, where N_{T7} is the number of tubes of the CNTFET varactor T_7 and N_{Ti} is the number of tubes utilized by all other CNTFETs.

Table 3: Design parameters for DNFCG LNA

	CNTFET dimension			Vxi (V)	Cap (pF)	Resistance (Ω)
M_1	310	10	(38, 0)	$V_{X2} = 0.38$	$C_2 = 5$	$R_b = 40$
M_2	5000	10	(38, 0)	$V_{X3} = 0.57$	$C_3 = 5$	$R_{x1} = 15k$
M_3	20	10	(38, 0)	$V_{X4} = 0.37$	$C_4 = 5$	$R_{x2} = 15k$
M_4	90	10	(38, 0)		$C_5 = 5$	$R_{x3} = 15k$
						$R_{x4} = 15k$

Fig. 10 shows the forward-gain (S_{21}) and NF. It can be seen that the simulated gain is equivalent to 15.9 dB over the frequency range of 17.5 GHz to 57 GHz and drops by just 0.9 dB over the entire bandwidth. One of the important design considerations of broadband LNA is to keep the NF magnitude lower than 3 dB for frequency range of interest. It can be seen that over the entire bandwidth (17.5 GHz to 57 GHz), the NF magnitude is less than 3 db.

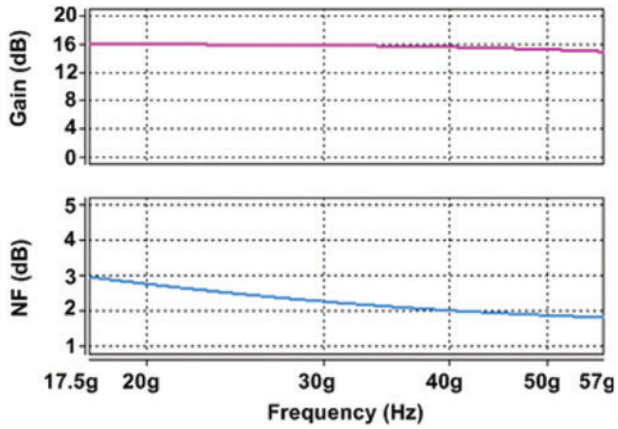


Figure 10: GAI based LNA gain and NF versus frequency

Fig. 11 demonstrates the S_{11}, S_{12} and S_{22} simulation results for the realized GAI based LNA. Magnitude of S_{11} ranges from −16.8 dB to −11.4 dB over the bandwidth (17.5 GHz to 57 GHz). The power dissipation of GAI based LNA is 6.961 mW. In summary, the realized GAI based LNA provides very high frequency bandwidth (17.5 GHz to 57 GHz), low NF (<3 dB), occupy less space due to absence of any spiral inductor and consumes only 6.961 mW.

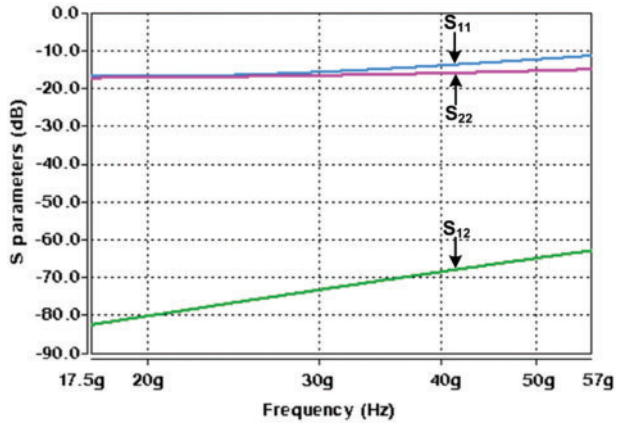


Figure 11: S_{11}, S_{12} and S_{22} versus frequency

Tab. 4 demonstrates the comparison of proposed CNTFET GAI based DNFCG LNA with other DNFCG LNA topologies. It can be seen that GAI based LNA design offers larger bandwidth and lower power dissipation. It is also important to mention that the tunability feature of GAI is useful for compensating the undesirable parameter effects due to process, voltage, temperature variations. Moreover, it can easily help to adopt specification of other broadband high frequency ASP applications. Due to wide inductive bandwidth, high QF, low power dissipation and large tunable inductance, the proposed GAI circuit can be utilized as a potential candidate for 5G/6G communication ASP modules.

Table 4: DNFCG LNA performance comparison

Reference	[30]	[31]	This work
Technology	32 nm CNTFET	180 nm CMOS	16 nm CNTFET
Voltage (V)	1 V	1.8 V	0.7 V
Bandwidth (GHz)	3–38	1.05–3.05	17.5–57
Power (mW)	16	12.6	6.961
Gain (dB)	14.7–13.7	16.9	15.9–15
NF (dB)	0.4–1.3	2.6–3.1	1.9–3
S_{11} (dB)	< -10	< -10	< -10

7 Conclusion

In this work, a CNTFET based GAI is presented. The proposed GAI circuit is free from external passive components and thus it is suitable for integrated circuit implementation. The realized AI is based on gyrator-C topology and employs only a few CNTFETs in the main path of signal which made it suitable for multi GHz broadband ASP applications. Simulation results demonstrate that the realized circuit consumes small power and provides high inductance, high QF, and large inductive bandwidth. These advantages make the proposed GAI an attractive candidate for low power, low voltage and high frequency broadband applications. Application of GAI is demonstrated in the design of broadband CNTFET based DNFCG LNA. Using the realized GAI in the input matching-network reduces the chip area. The realized GAI based LNA provides high gain, high frequency bandwidth, low NF and low power dissipation. The GAI and LNA circuit simulation outcomes based on CNTFET Stanford model using 16 nm technology node confirm the theoretical predictions.

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