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An Energy-Efficient 12b 2.56 MS/s SAR ADC Using Successive Scaling of Reference Voltages

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Abstract: This paper presents an energy efficient architecture for successive approximation register (SAR) analog to digital converter (ADC). SAR ADCs with a capacitor array structure have been widely used because of its simple architecture and relatively high speed. However, conventional SAR ADCs consume relatively high energy due to the large number of capacitors used in the capacitor array and their sizes scaled up along with the number of bits. The proposed architecture reduces the energy consumption as well as the capacitor size by employing a new array architecture that scales down the reference voltages instead of scaling up the capacitor sizes. The proposed 12-bit SAR ADC is implemented in Complementary Metal Oxide Semiconductor (CMOS) 0.13 um library using Cadence Virtuoso design tool. Simulation results and mathematical model demonstrate the overall energy savings of up to 97.3% compared with conventional SAR ADC, 67% compared with the SAR ADC with split capacitor, and 35% compared with the resistor and capacitor (R&C) Hybrid SAR ADC. The ADC achieves an effective number of bits (ENOB) of 11.27 bits and consumes 61.7 uW at sampling rate of 2.56 MS/s, offering an energy consumption of 9.8 fJ per conversion step. The proposed SAR ADC offers 95.5% reduction in chip core area compared to conventional architecture, while occupying an active area of 0.088 mm^2.

Keywords: Low voltage low power; successive approximation register; analog to digital converter; switching energy

1 Introduction

Wireless sensor networks and implantable biomedical devices has been gaining popularity in the recent years. These applications require low power consumption because of their limited power budget while achieving optimum performance. Also, it is required to include an analog to digital converter (ADC) for converting sensor data to digital. So, energy and area efficient ADCs plays a pivotal role.

For many ADC architectures, analog circuits are often employed such as operational amplifiers, which usually consume high energy. But the successive approximation register (SAR) ADCs, however, only need a simple analog circuit like a comparator since they carry out the rest of the operations using the digital circuits. SAR ADCs can, therefore, result in an improved performance and reduced power consumption. Despite these advantages, however, SAR ADCs are not selected for high resolution applications, because their capacitor array requires an excessively large capacitors for high resolution. Various techniques have been proposed to overcome this short coming of SAR ADC. The technique in [1] reduced the supply voltage to reduce the energy consumption, while [2] proposed the merged capacitor switching scheme, to reduce the switching power. In [3,4], a reduction in total capacitor size is realized by using the split capacitor scheme and the R&C Hybrid scheme.

Literature reveals several techniques to reduce the capacitor array size without digital calibration for fully differential architecture [5]. To reduce the capacitor array size by half a top plate sampling technique is used in [6], but at the expense of non-linearity and common mode input dependency. In [7] a digital to analog converter (DAC) configurable window switching technique to ensure reusing the capacitors in DAC is incorporated in SAR ADCs for overall smaller capacitances. However, the benefit of energy efficiency drops. In order to reduce the switching energy and improve the DAC linearity floating DAC switching technique is presented in [8].

In this paper, we propose a SAR ADC architecture based on successive scaling of the reference voltages instead of conventional scaling of capacitor size to reduce the switching energy consumption and chip area.

The rest of this paper is organized as follows: Section 2 describes the general architecture of SAR ADCs. Section 3 presents the proposed architecture and the analysis of its switching energy. Section 4 describes a 12-bit ADC implementation based on the proposed architecture. Section 5 analyzes the performance of the 12-bit ADC implementation followed by the conclusions in Section 6.

2 SAR ADC Algorithm

Fig. 1 shows a structure of a general SAR ADC, which consists of a DAC capacitor array, a comparator circuit, and a SAR control logic. The DAC capacitor array combines the functionality of digital to analog conversion and sample and hold to produce an approximated common mode voltage V_{cm}. The comparator determines whether the approximated voltage is greater than the predefined common mode voltage. If the voltage is greater, the SAR logic keeps the most significant bit (MSB) bit as one, or otherwise, it flips the MSB bit to zero. The above process is repeated with the next capacitor switched on and the new approximation value compared with the reference voltage. Each comparison result determines each bit of the digital output, where each bit successively improves the accuracy of the conversion. This process of successive comparison continues until the entire digital word is decoded. Fig. 2 shows the conventional DAC capacitor array [9]. The operation of the conventional SAR ADC is described below.

Initially, S_{sample} is high and the entire capacitor array stores the voltage $V_{cm} - V_{IN}$. Then, the MSB capacitor C_b, is connected to V_{ref} and the remaining capacitors are connected to ground, and so V_X is expressed by Eq. (1).

$$V_X = V_{cm} - V_{\epsilon} + \frac{V_{ref}}{2} \tag{1}$$

Then, the comparator output is given by Eq. (2).

$$V_{OUT} = \begin{cases} 1 & V_{IN} < V_{ref}/2 \\ 0 & V_{IN} > V_{ref}/2 \end{cases} \tag{2}$$

The comparator output determines the MSB bit of the digital output. If the output voltage V_{OUT} is low, the MSB is kept at one and so the voltage of C_b is kept. On the other hand, if V_{OUT} is high, the MSB is flipped to zero, and so the voltage of C_b is returned to ground. The next largest capacitor C_{b-1} in the capacitor array is then be connected to V_{ref}, increasing the output voltage at V_X.

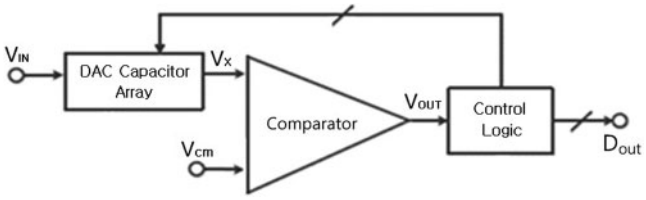

Figure 1: Block diagram of a general SAR ADC

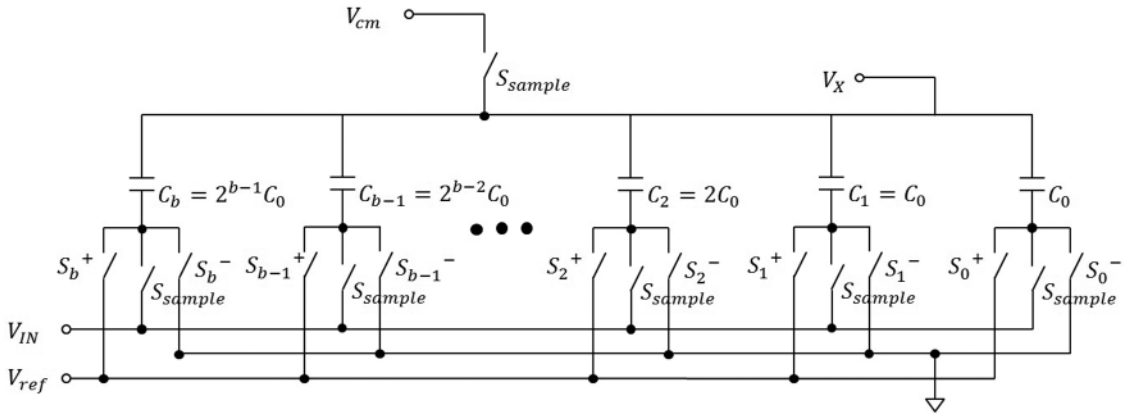

Figure 2: Conventional capacitor array of a b-bit SAR ADC

The above process is repeated for successive capacitors in the array. In each stage, the updated value of V_X is expressed by Eq. (3).

$$V_X = V_{cm} - V_{IN} + \frac{C_T}{C_T + C_B} \tag{3}$$

Here, C_T is the sum of all capacitors connected to the reference voltage, and C_B is the sum of all capacitors connected to ground terminal.

3 Proposed Architecture

During every bit cycle, the connections of the capacitors are changed. This section analyzes the switching energy [10] of the conventional architecture and the proposed scheme. For simplicity of analysis, a 2-bit capacitor array is selected in this section. A conventional 2-bit capacitor array is first analyzed, which is illustrated in Fig. 3.

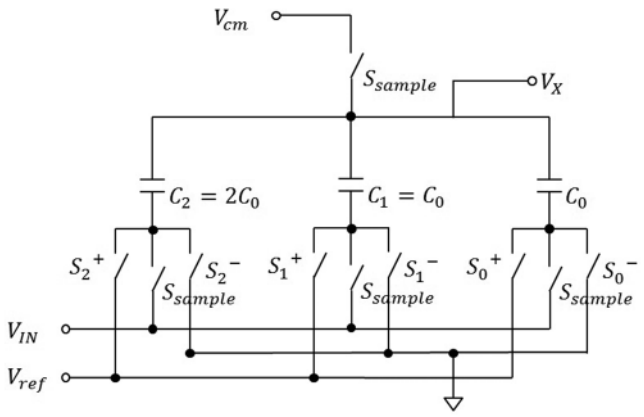

Figure 3: Capacitor array of a conventional 2-bit SAR ADC

At time 0^-, the input voltage is fully sampled by switch S_{sample} of the capacitor array, while all other switches are OFF. In the 1st iteration of the approximation process, at time 0, the bottom plate of the capacitor C_2 is connected to V_{ref}, while the other capacitors are connected to ground. Then V_X of the capacitor array is charged to the value expressed by Eq. (1). If the capacitor array settles in time T_P, the energy drawn by the capacitor array is given by Eq. (4).

$$E_{0\to1} = \int_0^{T_P} i_{ref}(t) V_{ref} dt = V_{ref} \int_0^{T_P} i_{ref}(t) dt \tag{4}$$

Since $i_{ref}(t) = -dQ_{C_2}/dt$, Eq. (4) can be simplified as Eq. (5).

$$\begin{aligned} E_{0\to1} &= -V_{ref} \int_0^{T_P} \frac{dQ_{C_2}}{dt} dt = -V_{ref} \int_{Q_{C_2}(0)}^{Q_{C_2}(T_P)} dQ_{C_2} \\ &= -V_{ref} Q_{C_2}(T_P) - Q_{C_2}(0) \\ &= -V_{ref}^2 C_0 \left(V_X[1] - V_{ref}\right) - V_X[0] \\ &= C_0 V_{ref}^2 \end{aligned} \tag{4}$$

Here $V_X[1] = V_{cm} - V_{IN} + V_{ref}/2$, while $V_X[0] = V_{cm} - V_{IN}$. For all the following calculations, T_P is assumed to be 1 for the sake of simplicity. At the end of each approximation iteration, the comparator in Fig. 1 compares V_X with V_{cm}, and produces V_{OUT}, which sets the corresponding digital bit to high value if $V_X < V_{cm}$.

In the 2nd iteration of the approximation process, C_1 in Fig. 3 is then connected to V_{ref}. Then the energy drawn by the capacitor array is computed by Eqs. (6) and (7). Here we assume that the MSB was determined as 1, and thus the capacitor ratio gives the output voltage ratio $(2C_0 + C_0)/4C_0 = 3/4$.

$$V_X[2] = V_{cm} - V_{IN} + \frac{3}{4} V_{ref} \tag{6}$$

$$E_{1\to2} = -V_{ref}[2C_0 \left(\left(V_X[2] - V_{ref}\right) - \left(V_X[1] - V_{ref}\right)\right) + C_0((V_X[2] - V_{ref}) - V_X[1])] = \frac{C_0 V_{ref}^2}{4} \tag{7}$$

Fig. 4 shows the proposed capacitor array architecture. The proposed architecture applies to each capacitor different reference voltage V_{ref} scaled down by the factor of 2_{m-i}, while keeping all the capacitor size as C_0. Here $V_{ref}{}^{i} = V_{ref}/2^{i}$ where i is the bit position with 0 indicating the MSB and so on. For the proposed architecture of Fig. 5, the energy drawn by the capacitor array for the 1st and the 2nd iterations of the approximation process are given by Eqs. (8)–(11), respectively.

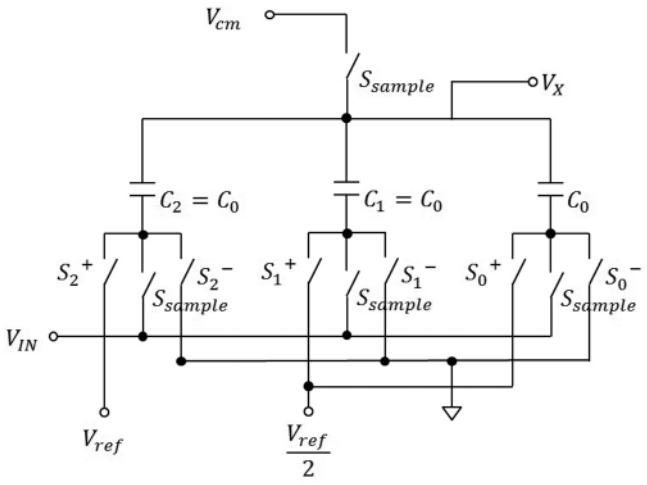

Figure 4: Capacitor array of a 2-bit SAR ADC based on scaled reference

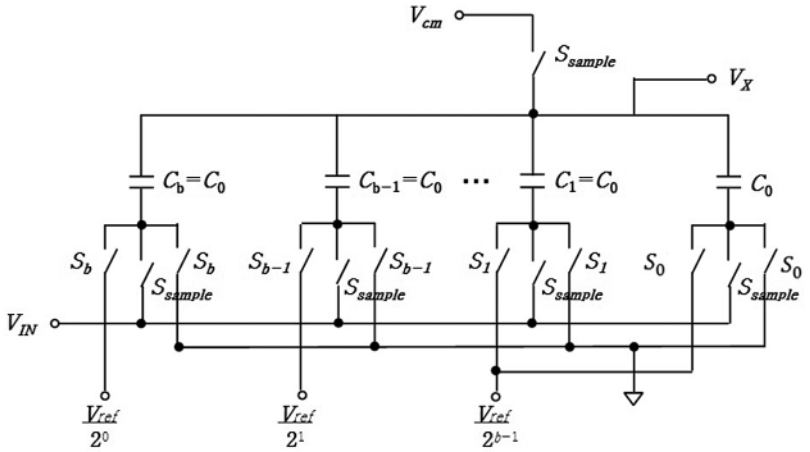

Figure 5: Capacitor array of a b-bit SAR ADC based on scaled reference

$$V_X[1] = V_{cm} - V_{IN} + \frac{1}{3}V_{ref} \tag{8}$$

$$E_{0\to1} = -V_{ref}C_0\left((V_X[1] - V_{ref}) - V_X[0]\right) = \frac{2C_0{V_{ref}}^2}{3} \tag{9}$$

$$V_X[2] = V_{cm} - V_{IN} + \frac{1}{2}V_{ref} \tag{10}$$

$$E_{1\to2} = -\frac{V_{ref}}{2}[C_0((V_X[2] - V_{ref}) - (V_X[1] - V_{ref})) + C_0((V_X[2] - \frac{V_{ref}}{2}) - V_X[1]) = \frac{C_0{V_{ref}}^2}{12} \tag{11}$$

It is evident from Eqs. (9) and (11) that the proposed SAR ADC architecture can substantially reduce the energy consumption as well as the size of capacitor array compared to the conventional architecture. For another example, Fig. 5 illustrates a b-bit SAR ADC based on the proposed scaled reference. Eqs. (12) and (13) compares the energy consumption of the capacitor array for the case of a conventional b-bit SAR ADC with the proposed one in Fig. 5.

By comparing Eqs. (12) and (13), it is observed that the energy reduction effect of the proposed SAR ADC is becoming drastically increasing. While the proposed architecture can substantially reduce the energy consumption and capacitor size, however, it has a restriction on the input dynamic range due to the reduced DAC maximum output voltage. This restriction can be acceptable for many ultra-low power and Internet of Things (IoT) application.

Conventional:

$$V_X[n] = \begin{cases} V_{cm} - V_{IN} + \frac{nV_{ref}}{2} & \cdots\cdots n < 2 \\ V_{cm} - V_{IN} + \frac{V_{ref}}{2^n} + \sum_{i=1}^{n-1} \frac{V_{ref}}{2^i} D_{b+1-i} & \cdots\cdots n \geq 2 \end{cases}$$

$$E_{n\to n+1} = -V_{ref}\left[\left(\sum_{i=0}^{n-1} 2^{b-1-i} D_{b-i} C_0 \left(-\left(V_X[n] - V_{ref}\right)\right)\right) + 2^{b-1-n} C_0 \left(\left(V_X[n+1] - V_{ref}\right) - V_X[n]\right)\right] \quad (12)$$

Proposed:

$$V_X[n] = \begin{cases} V_{cm} - V_{IN} + \frac{nV_{ref}}{b+1} & \cdots\cdots n < 2 \\ V_{cm} - V_{\epsilon} + \frac{V_{ref}}{2^{n-1}(b+1)} + \sum_{i=1}^{n-1} \frac{D_{b+1-i} V_{ref}}{2^{i-1}(b+1)} & \cdots \quad n \geq 2 \end{cases}$$

$$E_{n\to n+1} = -\frac{V_{ref}}{2^n} C_0 \left(\left(V_X[n+1] - \frac{V_{ref}}{2^n}\right) - V_X[n]\right) - \left[\sum_{i=0}^{n-1} \frac{V_{ref}}{2^i} C_0 D_{b-i} \left(\left(V_X[n+1] - \frac{V_{ref}}{2^i}\right) - \left(V_X[n] - \frac{V_{ref}}{2^i}\right)\right)\right] \quad (13)$$

4 Circuit Implementation

To evaluate the performance of the proposed architecture, a 12-bit SAR ADC is implemented based on the proposed successive reference scaling architecture, which is shown in Fig. 6. We implemented it in a fully differential structure to suppress the common mode noise. It also helps to inhibit even harmonic noise, thus improving the dynamic performance of ADC. The key building blocks of the implementation consists of bootstrapped switches, a dynamic comparator, a SAR control logic, and capacitor array DACs including the scaled reference voltages. The following sections describe the design considerations of the building blocks.

4.1 Bootstrapped Switch

An input sampling switch often has large impact on the performance of ADC circuits. To improve the linearity of the switch's transfer function, bootstrapped switch circuits have been widely studied. In this paper, thick gate oxide nMOS transistors are used to minimize the leakage current. To turn on the transistors, series cascaded bootstrap circuits [11] are used. It can generate twice the supply voltage as a gate-source voltage.

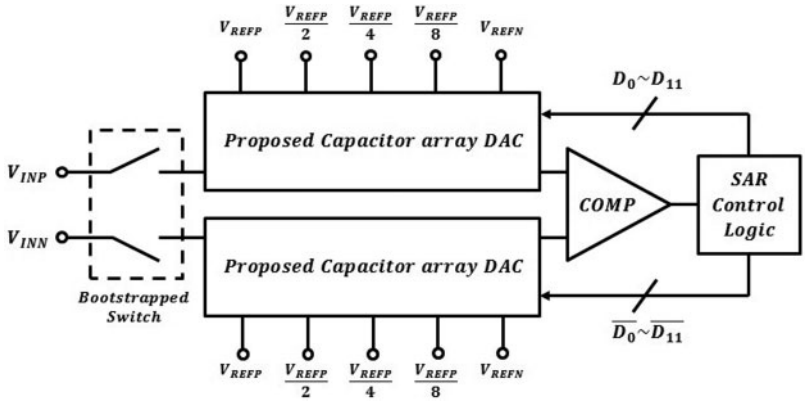

Figure 6: Block diagram of a proposed 12-bit SAR ADC

Fig. 7 explains the simplified operation of the cascaded bootstrapped switch circuit. Input clock is only a single-phase clock φ. When φ is low, the bootstrapping circuit is in the Hold mode. During the Hold mode, the voltage differences between the top plate and the bottom plate of both C1 and C2 are charged to VDD by S1, S2 and S5, S7, respectively. And V_g is discharged to ground by S8 to turn off the switch transistor MN_{sw}.

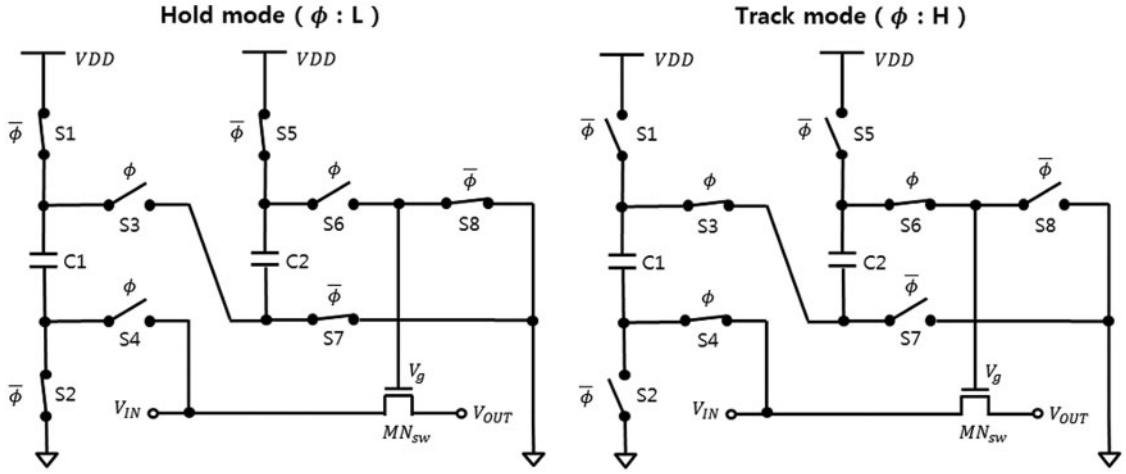

Figure 7: The operation of the bootstrapped switch

When φ goes high, the bootstrapping circuit moves to Sample mode. Then the series cascaded C1 and C2 provide 2XVDD as the gate-source voltage to MN_{sw}, by turning S3, S4, and S6 on. Therefore, the bootstrapped switch circuits achieve low on-resistance and high linearity by applying twice the supply voltage to the transistor gate. This results in V_{OUT} becoming almost equal to V_{IN}, and so the sampling operation can be conducted with high linearity regardless of input signal level.

4.2 Hybrid Structure of Capacitor Array

While the proposed architecture can substantially reduce the switching energy of the capacitor array, it has some limitations. The input dynamic range is reduced by the reduced reference voltage. Generating different reference voltages can be challenging if it requires a large number of reference

voltages. To alleviate this challenge, we propose a hybrid structure of capacitor array, which combines the proposed reference-scaling array along with the conventional capacitor-scaling array. For example, Fig. 8 shows a 12-bit capacitor array using the hybrid architecture. It employs the reference-scaling architecture for a 4-bit segment (Bit8∼Bit5) and uses the capacitor-scaling architecture for the rest of the array (Bit11∼Bit9 and Bit4∼Bit0). We assume that these 4 reference voltages can be provided by a power management integrated circuit (PMIC) or internal voltage regulators.

Furthermore, the size of the capacitor array can be further reduced by using a split capacitor. The split capacitor is used to split the array into a least significant bit (LSB) array and a MSB array. Fig. 8 shows a split capacitor of size $(32/31)C_0$ inserted between the capacitors for Bit5 an Bit4. The capacitance value of a split capacitor is calculated by Eq. (14).

$$C_{LSB\ array} = Sum\ of\ the\ LSB\ array\ capacitors$$

$$C_0 = C_{split}/C_{LSB\ array} = C_{split}/32C_0$$

$$C_{split} = \frac{32}{31}C_0 \tag{14}$$

In the example of Fig. 8, the proposed hybrid array architecture reduces the overall capacitor size by 98.8% compared to the conventional capacitor-scaling array. The reduced input dynamic range is only 15.8%, which is considered very small cost given the size reduction is significant.

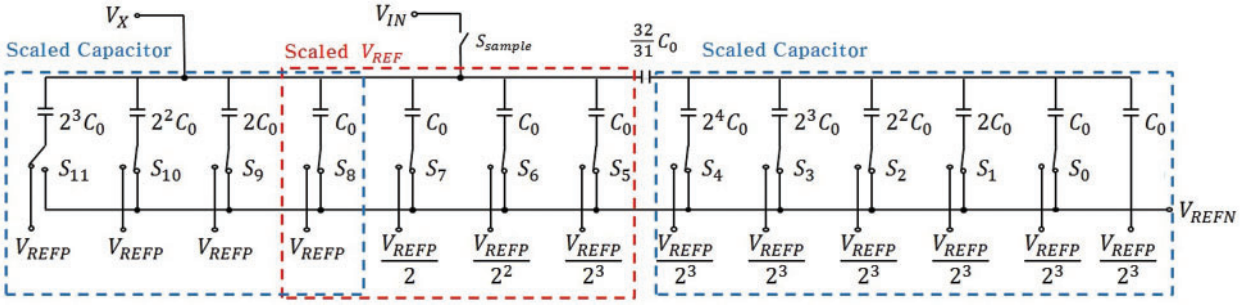

Figure 8: Architecture of proposed 12-bit capacitor array DAC

In addition, the proposed architecture eliminates the needs for an extra reference voltage V_{cm}, which was used by the conventional architecture shown in Fig. 3. The conventional architecture samples the input voltage using the bottom-plate of the capacitor array while connecting the top-plate to the reference voltage (V_{cm}). The proposed architecture illustrated in Fig. 8, however, samples the input voltage using the top plate of the capacitors, and thus does not need V_{cm}. During the input sampling, the MSB is preset to achieve a full-range sampling, which also eliminates an extra reset cycle. As shown in Fig. 9, the differential inputs are initially connected to the top plates of the capacitor array, and simultaneously the MSB is set to high (connecting S11 to V_{REFP}) and all other bits are set to low (connecting S_i to V_{REFP}). Next, the top-plate sampling switch S_{sample} is open and the sampled input voltage is kept in the capacitor array. A similar approach has also been reported in [12].

4.3 Dynamic Comparator

In SAR ADCs, the comparator also considerably contributes to the power consumption. We employ a two-stage dynamic circuit design similar to [13]. The comparator is shown in Fig. 10. The first stage is a voltage amplification stage. The second stage is a latch structure with cross-coupled

inverters acting as a positive-feedback amplifier. It obtains the rail-to-rail digital output (SP and SN). Prior to the comparison, the nodes FN and FP are discharged by a high value of the clock.

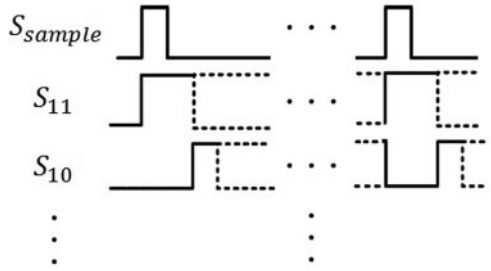

Figure 9: Timing diagram of capacitor array

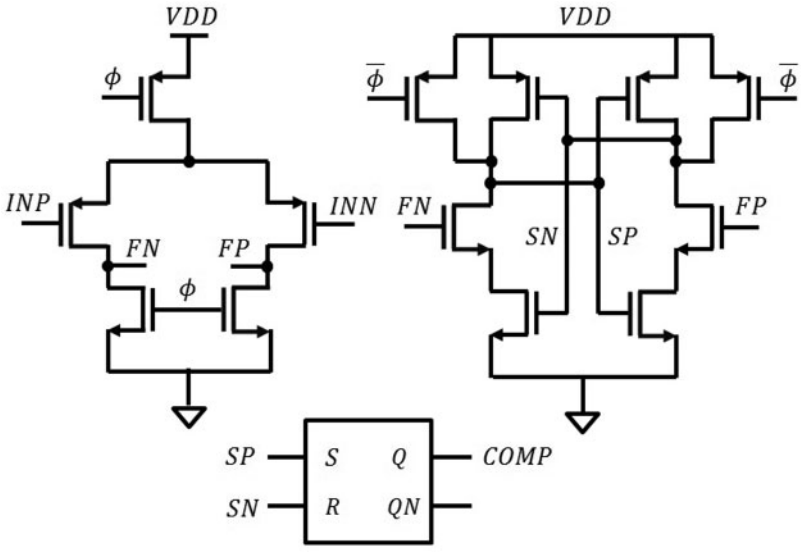

Figure 10: Architecture of dynamic comparator

4.4 SAR Control Logic

For SAR control logic, asynchronous control circuits have been often used to achieve high speed [14]. The circulation behavior of the asynchronous circuits, however, can incur serious stability problems, when the asynchronous circuits experience variations in the process, voltage, and temperature. To avoid such risk, therefore, we employ synchronous control circuit based on a ring counter structure. Fig. 11 shows the SAR control circuit used by the proposed SAR ADC.

The operation of the control circuit is summarized below. For each conversion, in the first cycle, the End of Conversion (EOC) signal is set to high, and all D-type flip flop (DFFs) are reset, and for rest of the cycles EOC is kept low until the final cycle. In the next cycle the most significant DFF is set to one which corresponds to MSB of the digital word of the ADC. Then the counter shifts '1' through the DFF from MSB to LSB.

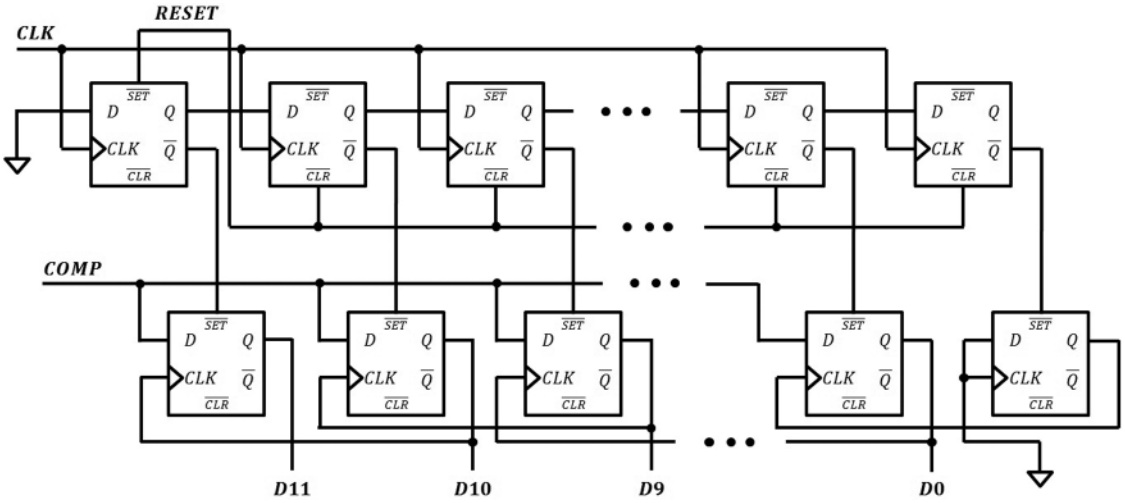

Figure 11: Architecture of SAR control logic

In each clock cycle, one of the outputs in the ring counter sets a DFF in the code register. The output of this DFF which is set by the ring counter is used as the clock signal for the previous DFF. At the rising edge of the clock, this DFF loads the result from the comparator. At the end of the conversion, EOC signal turns to high. This SAR control circuit produces very few signal transitions leading to low power consumption.

5 Simulation Results

The proposed SAR ADC was implemented and fabricated using a 0.13 um CMOS process. Fig. 12 shows the layout result of the chip, where the chip area is 262 um × 335 um, occupying an active area of 0.088 mm^2 Based on the process design rule, we used the minimum metal–insulation- metal (MIM) capacitor of size 67.35 fF as the unit capacitor (C_0) for the proposed capacitor array.

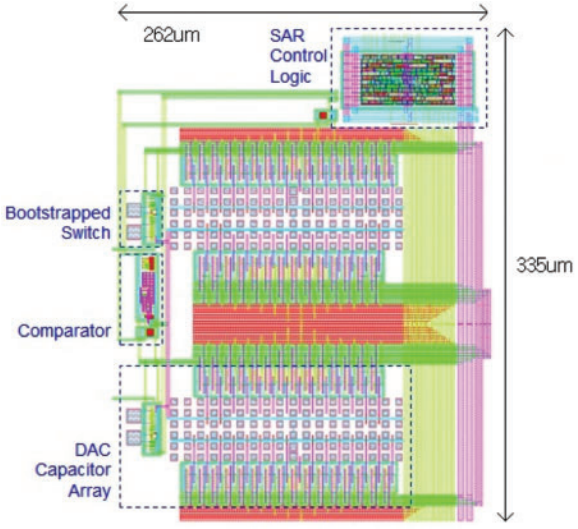

Figure 12: Layout view of proposed 12-bit SAR ADC

Fig. 13 compares the energy consumption of the proposed SAR ADC with various previous SAR ADCs: conventional, split capacitor, and R&C Hybrid SAR ADC. For fair comparison of various capacitor array architectures, the same dynamic comparator and SAR control circuit are used in all ADCs architectures compared above. The proposed SAR ADC provides the lowest energy consumption throughout all range of input voltages (X-axis indicates the corresponding digital output code).

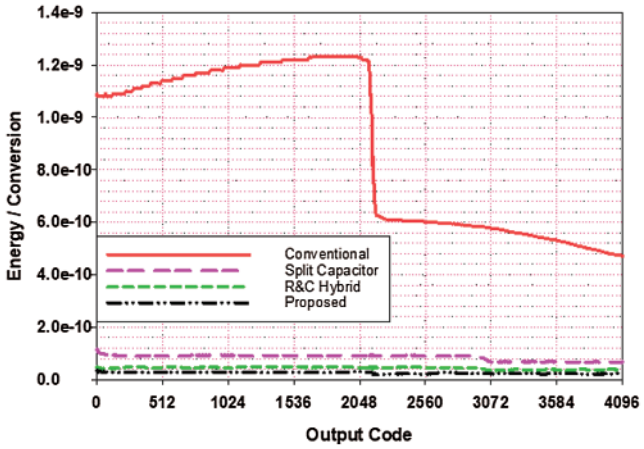

Figure 13: Comparison results of the energy consumption

Fig. 14 shows spectral analysis for the output of the proposed SAR ADC. Under a supply voltage of 1.5 V and a sampling frequency of 2.56 MS/s, the proposed ADC provides an SNDR of 69.63 dB, which is equivalent to 11.27 ENOB.

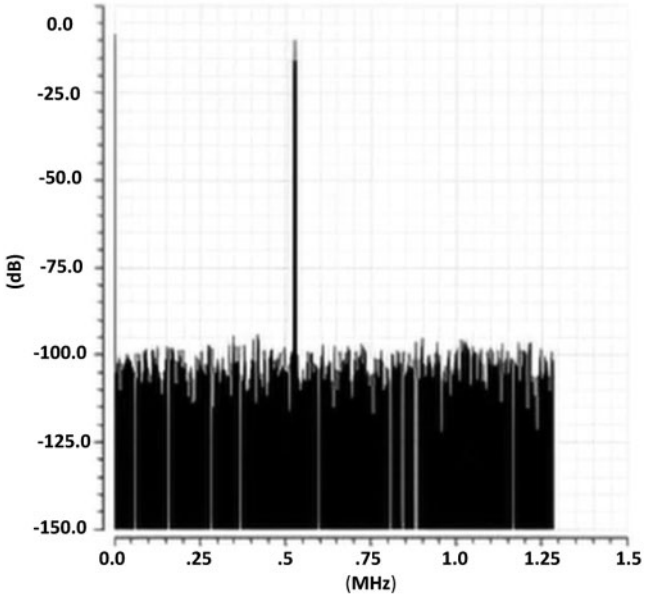

Figure 14: Output spectrum operating at 2.56 MS/s

Under the same operating conditions, we conducted detailed comparison between the proposed SAR ADC and the previous SAR ADCs. Tab. 1 demonstrates that the proposed SAR ADC achieves the lowest power consumption. It reduces the power consumption by 35% compared with the R&C Hybrid ADC, 67% compared with the ADC with split capacitor, and 97.3% compared with the conventional SAR ADC. In addition, the proposed SAR ADC reduces the chip area by 95.5% compared with the conventional SAR ADC.

Table 1: Performance comparison

	Conventional [12]	Split capacitor [3]	R&C hybrid [4]	Proposed
Technology [nm]	130			
Supply Voltage [V]	1.5			
Sampling Rate [S/s]	2.56 M			
Resolution [Bit]	12			
SNDR [dB]	71.17	70.76	70.33	69.63
ENOB [Bit]	11.53	11.46	11.39	11.27
Power [uW]	2294.6	202.7	102.8	61.7
FoM [fJ/conv.-step]	303.1	28.1	14.9	9.8

6 Conclusion

This paper proposed an energy-efficient architecture of successive approximation register (SAR) analog to digital converter (ADC) based on successive scaling of reference voltage. The proposed architecture incorporates a hybrid array architecture that scales down the reference voltages instead of scaling up the capacitor sizes. To illustrate the concept, a 12-bit SAR ADC is implemented in Complementary Metal Oxide Semiconductor (CMOS) 0.13um library using Cadence Virtuoso design suite and compared with conventional SAR ADC, SAR ADC with split capacitor, and Resistor & capacitor (R&C) Hybrid SAR ADC. Simulation results demonstrates an overall energy saving of 97.3%, 67%, and 35% respectively compared to conventional, with split capacitor, and R&C Hybrid SAR ADCs. The ADC achieves an effective number of bits (ENOB) of 11.27 bits and consumes 61.7 uW at sampling rate of 2.56MS/s, offering an energy efficiency of 9.8fJ per conversion step. The proposed architecture reduces the capacitor array size by 98.8% and offers 95.5% reduction in the overall chip core area, while occupying an active area of 0.088 mm^2.

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Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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