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Thermally-induced Warpage Measurement and Applications in Electronic Packaging using Shadow MoirAC

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Summary

Recently a number of changes have occurred in electronic packaging, such as increased contact density in both packages and substrates, high reflow temperature due to Pb-free conversion, new materials, new package configurations and new fabrication processes. All these trends demand tighter mechanical tolerances and increase the challenges in modern electronic assembly. Consequently surface flatness plays a more important role in the design and manufacturing process. Warpage introduced by dissimilar CTE (Coefficient of Thermal Expansion) can cause die cracking, solder joint opens, and solder joint cracking. Characterization of the thermally-induced warpage is proving to have significant value in improving manufacturing yield and reliability.

Shadow moirAC is a well-established optical technique for non-contact and full-field surface measurement. It has the advantages of high speed, high resolution, robustness, and adaptability with a thermal environment when compared to other techniques. In this paper, we integrate the shadow moirAC technique with a thermal environment to measure the thermally-induced warpage. Three typical applications in the electronic packaging industry: solder joint studies, thermal cycling tests, and computer modeling validation, are presented. It is concluded that advanced characterization of thermally-induced warpage can be an important means for reducing interconnect defects in the lifetime of an electronic product from design, manufacturing process, to reliability phases.