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Multi-Objective Optimization Method for Insulation Coordination of Offshore VSC-HVDC Converter Stations Considering Surge Arrester Parameter Selection

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ABSTRACT: Reasonable insulation coordination design balancing economic cost and operational safety of equipment is particularly critical for VSC-HVDC converter stations subject to lightweight and high-integration requirements. To address the excessive margins of surge arrester parameter selection and insulation coordination in conventional engineering schemes, this paper proposes a systematic collaborative optimization method of surge arrester parameters and equipment insulation levels for offshore VSC-HVDC converter stations. Based on a typical ± 400 kV offshore wind VSC-HVDC system, the surge arrester arrangement and insulation margins of the offshore VSC-HVDC converter station are presented and discussed according to the principles insulation coordination. Accordingly, a multi-objective coordinate optimization model for surge arrester parameters and equipment insulation levels is proposed, considering both life-cycle cost objective and technical objective, in which a novel transient stress index-based equivalent safety margin is introduced as the technical optimization objective. Meanwhile, an electromagnetic-transient-simulation-driven discrete multi-objective optimization solution method is adopted to obtain the optimal design scheme. Finally, a case study is carried out to verify the feasibility and effectiveness of the proposed systematic insulation coordination design methodology. Simulation results reveal that, compared with the direct-margin reference, the proposed recommended scheme improves the system-level equivalent safety margin by 7.40% and reduces the total life-cycle cost by 3.42%.

KEYWORDS: Offshore VSC-HVDC converter station; insulation coordination; surge arrester; equivalent safety margin; multi-objective optimization

1 Introduction

With the global transition toward low-carbon energy and the increasing scale of far-offshore wind power, offshore wind development is shifting from nearshore, small-capacity, and single-station projects toward long-distance, large-capacity, and clustered transmission. Voltage-source-converter-based high-voltage direct current (VSC-HVDC) transmission enables independent active and reactive power control, adapts well to weak AC (alternating current) systems, and avoids the severe charging-power limitation of long-distance DC (direct current) submarine cables. Therefore, it has become an important technical route for large-scale offshore wind power integration [1,2]. Meanwhile, offshore converter platforms are strongly constrained by space, weight, marine environment, and operation and maintenance conditions, making lightweight and compact platform design an important direction in engineering practice [3]. In this context,

the layout of primary equipment and overvoltage-protection apparatus, along with the insulation design in converter stations affect not only system operational safety, but also platform volume, equipment cost, and life-cycle economy [4,5]. Insulation coordination refers to determining the voltages that equipment may experience under overvoltage protection measures, and subsequently selecting the equipment's insulation strength based on safe operation and techno-economic rationality [6].

In offshore converter station design, the two most critical aspects of insulation coordination are the determination of the arrester configuration scheme and the determination of equipment insulation levels. The former determines whether overvoltages in different protection zones can be effectively limited, while the latter determines whether the protected equipment has sufficient withstand capability under representative overvoltages. Generally, the arrester configuration scheme should be based on the system structure and typical switching-overvoltage conditions. Electromagnetic transient simulations are usually conducted for AC- and DC-side faults, switching operations, blocking, restart, and line faults to identify the decisive overvoltage conditions at key nodes, according to which the arrester placement scheme is established. For offshore wind VSC-HVDC systems, Reference [7] has specified the protection zones of typical arresters. Recent studies on arrester placement also indicate that a greater number of surge arresters does not necessarily yield better performance. Instead, the optimal scheme with superior overall performance should be determined by jointly considering protection effectiveness, insulation risk, and installation economy [8,9]. The insulation level of key equipment is determined by combining system topology and fault simulation results. Since different fault types and observation nodes may correspond to different decisive conditions, arrester configuration must be based on protection-zone division and exhaustive simulation results [10,11].

As the basis of insulation coordination and system reliability analysis, arrester parameter design is closely related to the insulation level of the protected equipment [12,13]. Residual voltage and absorbed energy are important indicators for evaluating the overvoltage suppression performance of arresters, while arrester energy stress is also a key constraint in configuration and parameter design [14–16]. For large-capacity, high-energy surge arrester applications, multi-column parallel structures are widely adopted to boost current and energy handling capacity. The number of parallel varistor columns directly affects per-column discharge current, energy absorption, and current-sharing reliability, and thus must be considered a core design variable rather than a fixed structural premise [17,18]. Consequently, arrester parameter configuration should be determined by system overvoltage calculation results. Optimal arrester selection and coordinated placement at key protection points effectively constrain transient overvoltage levels and elevate the overall protection performance of HVDC converter stations [19,20].

For determining equipment insulation levels, the core objective of VSC-HVDC insulation coordination is to strike a reasonable balance between the prospective system overvoltage level and the insulation withstand strength of primary equipment. At present, three typical insulation coordination methods are widely adopted in VSC-HVDC projects, including the statistical method, the simplified statistical method, and the deterministic method. Existing standards provide insulation coordination procedures for HVDC converter stations. Based on representative overvoltage, the withstand voltage levels of main equipment are determined by considering arrester protective level, insulation safety margin, and equipment type [6,21]. For important equipment such as transformers, insulation coordination studies also emphasize that the protection level should be matched with equipment insulation strength, rather than relying solely on increasing the insulation level [22]. Some studies combine Monte Carlo simulation, the Electromagnetic Transients Program (EMTP), and mean time between failures (MTBF) to select arresters and determine their corresponding insulation levels [23]. Since both the AC and DC sides of offshore stations commonly use

submarine cables, insulation coordination should mainly focus on switching overvoltages during faults and fault-clearing processes. The switching impulse withstand levels of equipment are then determined through multi-scenario fault scanning, arrester stress verification, and insulation margin calculation [24,25].

From the perspective of optimization research, existing studies on offshore wind HVDC systems have incorporated topology, control strategy, and insulation requirements into a unified optimization framework, together with operating cost, investment cost, and simulation-based design verification [26]. In transmission-line applications, cost-effective insulation coordination has been employed to reduce lightning back-flashover risk while accounting for protection investment [27]. In distribution-network lightning-protection studies, multi-objective optimization has also been adopted to balance the flashover risk, protection-device cost, and arrester placement [28].

In arrester-related optimization, differentiated arrester configuration, multi-objective optimization, and risk-aware arrester modeling have been applied to distribution-network lightning protection and arrester placement optimization [29,30]. In addition, optimization studies on arrester dynamic-model parameters show that the accuracy of residual-voltage prediction directly affects the reliability of overvoltage calculation, arrester configuration, and insulation coordination analysis [31]. Overall, existing studies have demonstrated the necessity of optimization from the perspectives of insulation cost, protection effectiveness, risk evaluation, and arrester parameter modeling. However, most studies still focus on transmission and distribution lines, conventional substations, or individual arrester models, and have not sufficiently addressed offshore wind VSC-HVDC converter stations. Although a relatively experience-driven engineering design has been employed successfully for insulation coordination in such stations, a systematic optimization method is still lacking.

This paper proposes a coordinated optimization method for arrester parameters and equipment insulation levels in offshore VSC-HVDC converter stations. Based on the existing insulation coordination procedure, the proposed method takes the representative overvoltage under typical switching-overvoltage conditions as the constraint basis, and treats the arrester protective level, parallel-column number, specified equipment withstand voltage, and actual insulation safety margin as coupled design variables. The transient stress index-based equivalent safety margin is introduced, along with a life-cycle cost model that comprises arrester cost, insulation cost, and fault risk cost. Furthermore, an electromagnetic-transient-simulation-driven discrete multi-objective optimization solution method is adopted to obtain a compromise scheme that balances insulation safety and engineering economy through Pareto non-dominated screening. The main contributions of this paper are as follows:

(1) A multi-objective coordinate optimization model for surge arrester parameters and equipment insulation levels is proposed, along with an electromagnetic-transient-simulation-driven discrete multi-objective optimization solution method, providing a systematic optimization procedure on insulation coordination for offshore VSC-HVDC converter station.

(2) A novel transient stress index based equivalent safety margin is proposed as the technical optimization objective for insulation coordination design, integrating peak overvoltage, wavefront steepness, duration-related stress intensity, and surge arrester energy absorption.

(3) Case study on systematic insulation coordination design for ± 400 kV offshore VSC-HVDC converter station is performed, demonstrating the technical and economic effectiveness of the proposed multi-objective coordinate optimization and the transient stress index based equivalent safety margin.

The remainder of this paper is organized as follows: Section 2 provides the basic topology and insulation coordination scheme for the offshore VSC-HVDC converter station. Section 3 proposes the multi-objective

optimization strategy of insulation coordination. Simulation results on a ± 400 kV offshore VSC-HVDC converter station are extensively analyzed in Section 4, and concluding remarks are summarized in Section 5.

2 Insulation Coordination Design of Offshore VSC-HVDC Converter Station

2.1 System Configuration of Offshore VSC-HVDC System

The topology of the offshore VSC-HVDC system investigated in this paper is illustrated in Fig. 1. The offshore VSC station and onshore VSC station are interconnected via a 99 km submarine DC cable and an 8-km land DC cable. The VSC-HVDC project adopts the modular multilevel converter (MMC) topology with a rated DC voltage of ± 400 kV and a rated capacity of 1100 MW [32]. The offshore wind farm steps up voltage to 220 kV via transformer T1 before connecting to the offshore converter station, while the onshore converter station is linked to the 400 kV onshore AC grid through transformer T2.

In steady-state operation, the offshore VSC station is normally operated under V/f control, and the onshore VSC station adopts constant DC voltage and constant reactive power control to deliver electrical power from the offshore wind farm to the onshore grid. In addition, the VSC-HVDC system can switch to STATCOM (Static Synchronous Compensator) mode with no active-power exchange inside the system, where the converter stations participate in voltage and reactive power regulation for the onshore grid.

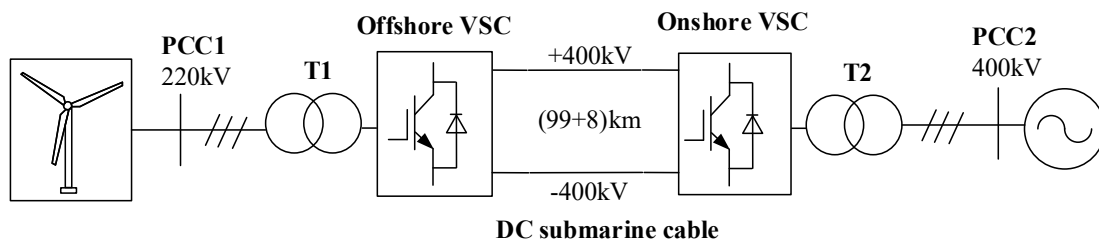


Figure 1: System topology of offshore VSC-HVDC system.

2.2 Principles and Design Scheme for Insulation Coordination

Overvoltages in offshore VSC-HVDC converter stations are mainly induced by system switching operations, grid faults, and lightning intrusion. Severe overvoltages may damage system equipment and even cause converter blocking. Therefore, it is essential to further investigate the insulation coordination principles and typical design schemes of VSC-HVDC converter stations to mitigate the overvoltage risk of offshore VSC-HVDC systems. The fundamental insulation coordination scheme is to optimization configuration and parameters of surge arresters.

The basic criterion for surge arrester layout is to ensure that all voltage levels and connected equipment are fully protected against overvoltages, while realizing an optimal matching among equipment insulation withstand capability, operational reliability, and construction cost. The layout principles of surge arresters for offshore VSC-HVDC converter stations, which are basically the same with convention power stations [33,34], can be summarized as follows:

- (1) Overvoltages generated on the DC side are mainly suppressed by DC-side surge arresters, including DC line surge arresters and converter bus surge arresters;
- (2) Overvoltages occurring on the AC side are primarily mitigated by AC bus surge arresters;
- (3) The internal overvoltage of electrical equipment inside the converter station is protected by the nearest surge arrester.

Based on the above layout principles, extensive electromagnetic transient simulations with different AC-side and DC-side faults, switching operations, blocking, restart, and line faults to identify the decisive

overvoltage conditions at key nodes of the offshore VSC-HVDC system were performed, yielding the optimized surge arrester configuration scheme [6] illustrated in Fig. 2. The installation positions and corresponding functions of each surge arrester in the configuration scheme are summarized in Table 1.

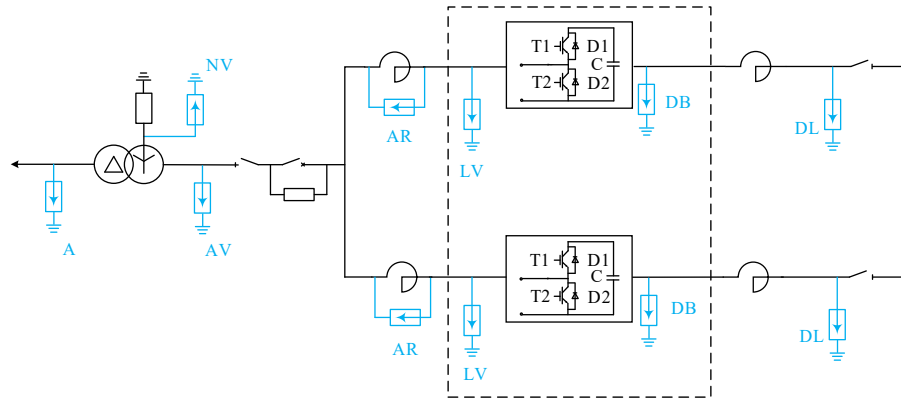


Figure 2: Arrangement scheme of surge arrester for offshore VSC-HVDC converter station.

Table 1: Location and function of surge arresters.

Symbol	Name	Function	Location
A	AC bus surge arrester	Protects the AC bus and incoming AC-side equipment.	AC bus or AC line entrance
AV	Transformer valve-side surge arrester	Limits overvoltage on the valve side of the converter transformer.	Valve-side terminal of the converter transformer
NV	Neutral-point surge arrester	Protects the transformer neutral point and grounding branch.	Neutral point of the converter transformer
AR	Arm-reactor surge arrester	Protects the arm reactor against switching overvoltage.	Across or near the arm reactor
LV	Valve-side arm-reactor surge arrester	Protects the converter valve and adjacent valve-side equipment.	Between the arm reactor and converter valve
DB	DC bus surge arrester	Limits overvoltage on the DC pole bus.	DC pole bus
DL	DC line surge arrester	Protects the DC line or cable terminal.	DC line/cable terminal

According to the existing industry standard [6], considering the insulation operating environment of grid-connected offshore VSC-HVDC converter stations, the differences in insulation requirements of various on-site equipment, and the improved protection performance of surge arresters, the minimum insulation safety margin of all equipment is specified to be no less than the values listed in Table 2. This paper focuses on switching overvoltage because offshore VSC-HVDC converter stations are usually connected with long submarine cables on the collection and transmission sides, making fault- and switching-related transients more critical for insulation coordination than direct lightning intrusion. In particular, switching overvoltages during fault occurrence and clearance are the primary factors determining arrester stress verification and equipment switching impulse withstand levels [25,35]. The values will be referred to technical objective in following optimization model.

Table 2: Minimum insulation margins for device.

Overvoltage Type	Oil Insulation (Line Side)	Oil Insulation (Valve Side)	Air Insulation
Steep-front overvoltage	1.25	1.25	1.25
Lightning overvoltage	1.25	1.20	1.20
Switching overvoltage	1.20	1.15	1.15

3 Multi-Objective Coordinated Optimization for Insulation Coordination

3.1 Optimization Variables Selection

The overvoltage level in each protection zone of a VSC-HVDC converter station is determined by both the voltage-clamping characteristic and the current- and energy-handling capability of the corresponding surge arrester. A lower protection level generally reduces the overvoltage stress imposed on protected equipment, but increases the discharge current, absorbed energy, and possibly the number of parallel varistor columns required. Conversely, a higher protection level reduces arrester-body stress and cost, but may increase the equipment withstand-voltage requirement. Therefore, a clear safety-economic trade-off exists among arrester parameters, equipment withstand voltage, and insulation safety margin, which yields the optimization variables selection as:

$$x = [\lambda_1, \lambda_2, \dots, \lambda_m, n_1, n_2, \dots, n_m, U_{\text{with},1}, U_{\text{with},2}, \dots, U_{\text{with},n}, K_1, K_2, \dots, K_n] \quad (1)$$

where λ_j is the voltage-coordinate scaling factor of the V-I characteristic of the j -th arrester, n_j is the number of parallel varistor columns in each arrester installed at a single protection point, $j \in \mathbf{A} = \{1, 2, \dots, m\}$; $U_{\text{with},i}$ is the specified withstand voltage of the i -th protected equipment or protection zone, and K_i is the actual insulation safety margin of the protection zone, $i \in \mathbf{I} = \{1, 2, \dots, n\}$.

$$\lambda_j \in \Lambda_j, n_j \in N_j, U_{\text{with},i} \in U_i \quad (2)$$

$$U_j(I_{\text{tot},j}, \lambda_j, n_j) = \lambda_j U_{j,0} \left(\frac{I_{\text{tot},j}}{n_j} \right) \quad (3)$$

$$I_{\text{col},j} = \frac{I_{\text{tot},j}}{n_j} \quad (4)$$

where $I_{\text{tot},j}$ and $I_{\text{col},j}$ are the total arrester current and the current per column, respectively, and $U_{j,0}()$ is the reference single-column V-I characteristic. Eqs. (3) and (4) give the system-level interpretation of the two arrester variables under ideal current sharing. λ_j changes the reference-voltage level of a physically admissible V-I curve family. n_j divides the total current and absorbed energy among columns. $\lambda_j < 1$ indicates a lower protective level, and $\lambda_j > 1$ indicates a higher protective level. Non-uniform current and energy sharing are subsequently represented by correction factors in the feasibility constraints.

$$U_{\text{rp},i}(\lambda, n) = \max_{s \in \mathbf{S}} U_{\text{max},i,s}(\lambda, n) \quad (5)$$

$$K_i(\lambda, n, U_{\text{with},i}) = \frac{U_{\text{with},i}}{U_{\text{rp},i}(\lambda, n)} \quad (6)$$

where $U_{\text{rp},i}$ is the representative overvoltage of the i -th protected zone is defined as the maximum overvoltage governing insulation coordination among the considered verification conditions, and $U_{\text{max},i,s}$ denotes the simulated peak overvoltage of zone i under fault condition s , $s \in \mathbf{S} = \{1, 2, \dots, r\}$.

It can be seen from Eq. (6) that the safety margin is not predetermined solely by an empirical coefficient; instead, it is jointly determined by the arrester protection effect and equipment withstand level. This paper establishes the mapping relationship through electromagnetic transient simulation, thereby converting adjustable arrester parameters into insulation coordination evaluation indicators.

3.2 Transient Stress Index Based Equivalent Safety Margin

Evaluating insulation safety only by the overvoltage peak has certain limitations. The fault transient process of VSC-HVDC converter stations usually has steep wavefronts and short durations. If two schemes have similar overvoltage peaks but different wavefront steepness or duration effects, their overall impact on equipment insulation and protection devices may not be the same. Therefore, this paper introduces a comprehensive transient stress index (TSI) on the basis of the conventional safety margin K .

For each protection zone i and verification condition s , $U_{pk,i,s}$ denotes the peak representative overvoltage, $D_{i,s}$ denotes the maximum wavefront steepness, and $A_{i,s}$ denotes the duration-related voltage stress. These terms are normalized by their corresponding baseline values before weighting.

$$U_{pk,i,s}(x) = \max_t |u_{i,s}(t; x)| \quad (7)$$

$$D_{i,s}(x) = \max_t \left| \frac{du_{i,s}(t; x)}{dt} \right| \quad (8)$$

$$A_{i,s}(x) = \int \left[|u_{i,s}(t)| - \sqrt{\frac{1}{\Delta t} \int_t^{t+\Delta t} u_{i,s}^2(t) dt} \right]_+ dt \quad (9)$$

$$TSI_i(x) = w_U \max_{s \in S} \frac{U_{pk,i,s}}{U_{pk,i,s0}} + w_D \max_{s \in S} \frac{D_{i,s}}{D_{i,s0}} + w_A \max_{s \in S} \frac{A_{i,s}}{A_{i,s0}} \quad (10)$$

where quantities with subscript 0 denote the reference arrester parameters under the same fault condition. The coefficients w_U , w_D and w_A are non-negative weighting coefficients for peak value, front steepness and duration stress, respectively, satisfying $w_U + w_D + w_A = 1$.

In multi-criteria evaluation and optimization, weighting methods generally include subjective, objective, and combined approaches. Since the relative importance of the components in this study is mainly governed by the engineering mechanism of insulation coordination, the Full Consistency Method (FUCOM) is adopted to determine the component weights, which is a subjective weighting method based on expert reference [36]. A smaller TSI indicates lower comprehensive voltage stress on the protected insulation relative to the same-fault reference. The safety index and system-level margin are calculated by:

$$K_{eq,i} = \frac{K_i}{(TSI_i)^\omega} \quad (11)$$

$$K_{eq,sys} = \min_{i \in I} K_{eq,i} \quad (12)$$

where ω is the transient-stress correction exponent. When $\omega = 0$ the equivalent safety margin degenerates into the conventional safety margin. When $TSI_i < 1$, the scheme reduces the comprehensive transient stress relative to the baseline scheme, which can indicate better comprehensive safety even if the peak-value margin changes only slightly. Accordingly, $K_{eq,i}$ is used as the safety index of a single protection zone, while the system-level margin $K_{eq,sys}$ is obtained by taking the most conservative value among all protection zones.

3.3 Multi-Objective Coordinated Optimization Model

3.3.1 Multi-Objective Optimization Function

This paper takes the minimization of life-cycle cost and equivalent safety-risk indicator as optimization objectives. Unlike directly using a fixed margin as the only criterion, this paper allows the actual safety margin K to vary within a reasonable engineering search range, and uses K_{eq} to combine equipment withstand capability and transient stress into a safety evaluation quantity. To reflect the uncertainty associated with publicly available equipment prices and engineering estimates, the economic objective value derived from low, middle, and high cost estimates.

$$\min f_1(x) = C_{total}(x) \quad (13)$$

$$\min f_2(x) = \frac{1}{K_{eq,sys}(x)} \quad (14)$$

where f_1 denotes the economic objective, and f_2 denotes the technical objective expressed by the reciprocal of the equivalent safety margin. A smaller f_2 indicates a higher equivalent safety margin of the system.

To compare the economy of different combinations of surge arrester protective level, parallel-column number, and equipment withstand voltage, this paper establishes a life-cycle equivalent cost model to characterize the relative variation of arrester investment, equipment insulation cost, and fault risk cost under different schemes. For each cost component, $\xi \in \{L, M, U\}$ denotes the low, middle, and high calibration levels. The baseline scheme refers to the original deterministic insulation coordination scheme used as the reference for cost and safety-margin normalization.

The cost of the j -th arrester is jointly affected by its protective level, parallel-column number, derived energy class, and topology-determined installation quantity, and it can be expressed as:

$$C_{MOA,j}^{\xi} = num_j C_{MOA,j,0}^{\xi} \frac{n_j}{n_{j,0}} \left(\frac{\lambda_{j0}}{\lambda_j} \right)^{\eta_j} \left(\frac{E_{r,j}}{E_{r,j0}} \right)^{\delta_j} \left(\frac{I_{r,j}}{I_{r,j0}} \right)^{\mu_j}, \xi \in \{L, M, U\} \quad (15)$$

where $C_{MOA,j}^{\xi}$ is the total cost of all installed type-(j) arresters under cost level ξ , num_j is the number of identical arresters required by the converter topology, while n_j is the parallel-column number within each arrester. $C_{MOA,j,0}^{\xi}$ is the calibrated reference cost at cost level ξ . η_j is the sensitivity coefficient of the increase in arrester cost caused by residual-voltage reduction. δ_j is the energy-class cost sensitivity coefficient, μ_j is the discharge-current capability cost sensitivity coefficient. $E_{r,j}$ and $E_{r,j0}$ are the selected and reference rated energy-absorption capabilities of one column; and $I_{r,j}$ and $I_{r,j0}$ are the corresponding rated discharge-current capabilities. The rated absorption capability of the arrester is determined according to the maximum absorbed energy obtained from fault simulation with an additional margin:

$$\begin{cases} E_j^{worst} = \max_{s \in S} E_{j,s} \\ E_j^{req,col} = k_E \gamma_{E,j} \frac{E_j^{worst}}{n_j} \\ E_{r,j} = \min \left\{ E \in \mathcal{E}_j : E \geq E_j^{req,col} \right\} \end{cases}, \frac{E_j^{req,col}}{E_{r,j}} \leq 1 \quad (16)$$

where $E_{j,s}$ is the absorbed energy under scenario s , E_j^{worst} is its maximum over the scenario set S , $E_j^{req,col}$ is the required energy capability per column, k_E and $\gamma_{E,j}$ are the energy safety and sharing factors, respectively.

In the insulation coordination design of VSC-HVDC converter stations, the arrester absorbed energy is typically required to incorporate the calculation values obtained from system simulation studies.

The insulation cost of the i -th protected equipment or protection zone is expressed as:

$$C_{\text{ins},i}^{\xi}(U_{\text{with},i}) = C_{\text{fix},i}^{\xi} + C_{\text{sen},i}^{\xi} \left(\frac{U_{\text{with},i}}{U_{\text{with},i,0}} \right)^{\gamma_i}, \xi \in \{L, M, U\} \quad (17)$$

where $C_{\text{fix},i}^{\xi}$ is the fixed cost weakly related to the insulation level, mainly including the equipment body, supporting structure, measurement devices, and switching devices; $C_{\text{sen},i}^{\xi}$ is the insulation-sensitive cost under the baseline insulation level; and γ_i is the exponent describing the increase in equipment size, air clearance, support insulation, and structural cost caused by increased insulation level. The candidate withstand levels are discrete engineering values rather than continuous variables.

In addition to initial investment, a reduced insulation margin may increase the expected loss associated with insulation damage or fault outage. Therefore, this paper further introduces the fault risk cost. The risk cost of the i -th protection zone is defined as:

$$C_{\text{risk},i}^{\xi}(x) = T \nu_i C_{\text{loss},i}^{\xi} P_{0,i} \exp[-\beta_i (\frac{K_{\text{eq},i}}{K_{\text{eq},i,0}} - 1)] \quad (18)$$

where T is the life-cycle evaluation period. ν_i is the annual equivalent frequency of severe representative overvoltage events in the i -th protection zone. $C_{\text{loss},i}^{\xi}$ is the the corresponding low, middle, or high loss estimate caused by a severe insulation fault or equipment damage. $P_{0,i}$ is the conditional probability that a severe event causes insulation damage or outage under the baseline scheme. β_i is the sensitivity coefficient of risk to the equivalent safety-margin variation, and $K_{\text{eq},i,0}$ is the equivalent safety margin under the baseline scheme.

When the equivalent safety margin of an optimized scheme is higher than that of the baseline scheme, the fault risk cost decreases; when the equivalent safety margin is lower than that of the baseline scheme, the fault risk cost increases.

The loss of a single severe fault can be further decomposed as:

$$C_{\text{loss},i} = C_{\text{rep},i} + C_{\text{out},i} + C_{\text{repair},i} \quad (19)$$

$$C_{\text{out},i} = P_{\text{out},i} t_{\text{out},i} c_e \quad (20)$$

where $C_{\text{rep},i}$ is the replacement or repair cost of damaged equipment within the protection zone. $C_{\text{out},i}$ is the outage energy loss. $P_{\text{out},i}$ is the equivalent outage power. $t_{\text{out},i}$ is the equivalent outage duration. c_e is the converted price of unit energy loss, and $C_{\text{repair},i}$ is the cost of maintenance, testing, restart, and labor.

The total life-cycle cost is represented by a low-to-high interval, and a representative value is obtained by combining the middle estimate with an upper-side uncertainty weighting factor ρ :

$$[C_{\text{total}}^L, C_{\text{total}}^U] = \sum_{j \in A} [C_{\text{MOA},j}^L, C_{\text{MOA},j}^U] + \sum_{i \in I} ([C_{\text{ins},i}^L, C_{\text{ins},i}^U] + [C_{\text{risk},i}^L, C_{\text{risk},i}^U]) \quad (21)$$

$$C_{\text{total}} = C_{\text{total}}^M + \rho(C_{\text{total}}^U - C_{\text{total}}^M), 0 \leq \rho \leq 1 \quad (22)$$

In the optimization model, this total cost is used as the economic objective f_1 .

3.3.2 Constraints

To ensure the engineering feasibility of the optimization results, the following constraints are imposed. The constraints encompass the discrete, physically admissible ranges of λ_j , n_j , and $U_{\text{with},i}$; minimum conventional insulation margin and minimum system-level equivalent margin; quantified steady-state conduction criteria; per-column peak current and energy capability; and, when product data are available, temporary-overvoltage (TOV) withstand verification. An artificial upper bound on the actual insulation margin is unnecessary, as excessive insulation is naturally penalized by the economic objective.

$$K_i = \frac{U_{\text{with},i}}{U_{\text{rp},i}} \geq K_{\min,i} \quad (23)$$

$$K_{\text{eq},\text{sys}} = \min_{i \in I} K_{\text{eq},i} \geq K_{\text{eq},\min} \quad (24)$$

where $K_{\min,i}$ is selected according to the insulation type, overvoltage category, and applicable engineering standard [6].

$$I_{\text{leak},j}^{\text{rms}} \leq n_j I_{\text{leak},\text{lim}}^{\text{rms}} \quad (25)$$

$$I_{\text{leak},j}^{\text{pk}} \leq n_j I_{\text{leak},\text{lim}}^{\text{pk}} \quad (26)$$

$$I_{\text{cap},\text{col},j} \geq \gamma_{i,j} \frac{I_{j,\text{pk}}^{\text{max}}}{n_j} \quad (27)$$

where $I_{\text{leak},j}^{\text{rms}}$ and $I_{\text{leak},j}^{\text{pk}}$ are, respectively, the RMS and peak values of the total leakage or conduction current of the j -th arrester assembly under normal operating voltage after the V–I characteristic is scaled; $I_{\text{leak},\text{lim}}^{\text{rms}}$ and $I_{\text{leak},\text{lim}}^{\text{pk}}$ are their per-column limits; $I_{j,\text{pk}}^{\text{max}}$ is the maximum total peak discharge current obtained over all evaluated fault scenarios; $I_{\text{cap},\text{col},j}$ is the per-column current capability; and $\gamma_{i,j}$ is the current-sharing factor. The first two inequalities prevent sustained conduction under normal operation, whereas the third prevents individual-column overloading during fault discharge.

The absorbed-energy constraints are expressed as:

$$\Delta E_j \leq \max(10^{-3} \text{kJ}, 10^{-3} E_{j,\text{fault}}^{\text{max}}) \quad (28)$$

$$E_{\text{cap},\text{col},j} \geq k_E \gamma_{E,j} \frac{E_{j,\text{eq}}^{\text{max}}}{n_j} \quad (29)$$

$$(U_{\text{TOV},j}, t_{\text{TOV},j}) \in \Omega_{\text{TOV},j} \quad (30)$$

where ΔE_j is the steady-state energy increment, $E_{j,\text{fault}}^{\text{max}}$ is the maximum fault-energy increment. The first inequality limits steady-state energy accumulation by combining an absolute tolerance with a relative tolerance referenced to the fault energy. $E_{j,\text{eq}}^{\text{max}}$ is the equivalent energy demand. $U_{\text{TOV},j}$, $t_{\text{TOV},j}$, and $\Omega_{\text{TOV},j}$ denote the TOV magnitude, duration, and allowable magnitude–duration region, respectively, ensuring that the arrester remains within its temporary-overvoltage withstand capability.

3.4 Solution Method

Since the change in arrester protective level requires electromagnetic transient simulation to obtain the corresponding overvoltage, current, and absorbed energy, directly calling PSCAD/EMTDC with a continuous intelligent optimization algorithm would lead to high computational cost. Considering that the objective of this paper is to establish a reproducible coordinated optimization procedure for arresters and insulation levels, an electromagnetic-transient-simulation-driven discrete multi-objective optimization method is adopted. The detailed procedure is as follows.

(1) Determine the arrester set A participating in the optimization, the protected equipment or protection-zone set I , and the fault verification condition set S according to the converter topology, protection-zone division, and insulation-coordination procedure. Establish the baseline arrester V-I curve and topology-determined installation quantity.

(2) Set the physically admissible candidate sets Λ_j and N_j for the arrester protective-level coefficient and parallel-column number. For each (λ_j, n_j) combination, adjust the corresponding arrester characteristics in PSCAD/EMTDC and conduct start-up and normal-operation verification. Candidates violating the quantified rms-current, peak-current, or steady-state energy-increment criteria are eliminated before fault evaluation.

(3) Conduct simulations under all fault conditions for λ combinations that pass the normal-operation verification, and extract overvoltage peak, wavefront steepness, duration effect, maximum arrester absorbed energy, maximum current, and other indicators.

(4) Set the candidate withstand-voltage set of each protected equipment in MATLAB, and combine each group of PSCAD results with the candidate withstand-voltage combinations to form a candidate solution set.

(5) For every complete combination of λ , n , and U_{with} , calculate K , TSI, K_{eq} , arrester cost, equipment insulation cost, fault risk cost, and total cost for each candidate solution. At this stage, every combination of λ and U_{with} is converted into a complete candidate scheme with both technical and economic attributes.

(6) Eliminate all candidates that violate the conventional or equivalent insulation-margin requirements, steady-state conduction criteria, per-column peak-current capability, or per-column energy capability. Only feasible complete insulation-coordination designs enter the objective-space comparison.

(7) Perform Pareto non-dominated screening using C_{total} and $1/K_{\text{eq,sys}}$ as the objectives. Where $K_{\text{eq,sys}}$ denotes the system-level equivalent safety margin and is conservatively taken as the minimum $K_{\text{eq},i}$ among all protected zones. If scheme a satisfies $C_{\text{total}}(a) \leq C_{\text{total}}(b)$ and $1/K_{\text{eq,sys}}(a) \leq 1/K_{\text{eq,sys}}(b)$, and at least one inequality is strict, then scheme a dominates scheme b. All feasible schemes not dominated by any other scheme constitute the Pareto optimal solution set.

(8) Select a compromise scheme from the Pareto optimal solution set. In this paper, the normalized distance method can be used to calculate the distance from each Pareto scheme to the ideal point, and the scheme with the minimum distance is selected as the recommended scheme.

$$d_q = \sqrt{((C_{\text{total},q} - C_{\text{total,min}})/(C_{\text{total,max}} - C_{\text{total,min}}))^2 + ((f_{2,q} - f_{2,min})/(f_{2,max} - f_{2,min}))^2} \quad (31)$$

where d_q is the normalized distance of the q -th Pareto solution, $C_{\text{total},q}$ and $K_{\text{eq,sys},q}$ are the normalized objective values. The ideal point is composed of the minimum normalized cost and the minimum normalized reciprocal safety-margin objective in the Pareto set, and the selected solution represents the closest safety-economic compromise to this ideal point.

4 Case Study

4.1 Parameter Settings

Based on the system topology shown in Figs. 1 and 2, the PSCAD/EMTDC simulation model of the offshore wind VSC-HVDC system is established. To verify the reliability of the proposed optimization model and method, three representative arrester protection zones are selected: the converter-transformer valve-side AC zone protected by AV arresters, the MMC valve-side arm-reactor zone protected by LV arresters, and the DC pole-bus zone protected by DB arresters. These three zones cover the main AC-side, valve-side, and DC-side insulation stresses of the offshore converter station and are also the positions where switching overvoltages, arrester current, and absorbed energy are most directly affected by arrester parameter selection. The main simulation parameters are listed in Table 3.

Table 3: Simulation parameters in the case study.

Parameters	Value	Description
Rated HVDC parameters	1100 MW, ± 400 kV, 50 Hz	Rated power, DC voltage, and system frequency of the offshore VSC-HVDC system.
AC bus voltage	220 kV (offshore), 400 kV (onshore)	Grid-side AC voltage levels of the offshore and onshore converter stations.
DC cable	99 km submarine cable + 8 km land cable, frequency-dependent phase-domain model	DC transmission cable length and model used in PSCAD/EMTDC.
AC-side cable model	Distributed-parameter/Bergeron model, two 5 km sections	AC-side cable representation in the simulation model.
Converter topology	Half-bridge MMC, 76 submodules per arm, arm reactor 50 mH, switching frequency 1650 Hz	MMC topology and main converter-side parameters retained in all simulations.
Converter control	PI parameters of V/f controller: $k_{p1} = 0.35$, $k_{i1} = 0.10$, PI parameters of constant DC voltage controller: $k_{p2} = 0.65$, $k_{i2} = 0.025$	V/f control (VSC offshore), Constant DC-voltage and reactive-power control (onshore VSC).
Fault resistance	0.01 Ω	Low-impedance grounding/short-circuit resistance kept identical for candidate comparison under the same fault category.
Fault time and duration	Inception time 1.5 s, duration 0.1 s	Faults are applied at 1.5 s and cleared after 0.1 s.
Breaker operation	/	When grid fault occurs, DC or AC breakers can interrupt the fault current within milliseconds.
Converter blocking logic	No extra manual blocking during the fault, built-in Dblk and DC-voltage limiter retained, $V_{dc,max} = 1.1$ p.u., $K_{VdcLim} = 5.0$, $T_{VdcLim} = 0.05$ s	Blocking and limiting logic is unchanged among all candidate simulations.
Numerical settings	Simulation duration 2.0 s, time step 50 μ s, output sampling interval 1 ms	Numerical settings for EMT simulation and waveform export.

Before the coordinated optimization, representative no-arrester fault simulations, including AC-side single-phase grounding, two-phase short circuit, three-phase short circuit, DC pole-to-ground fault, pole-to-pole short circuit, and valve-side grounding faults, were carried out to identify the most severe overvoltage condition of each protection zone. The maximum overvoltage at the DB surge arrester measurement point

is approximately $U_{\max, \text{noDB}} = 938.560$ kV, while the long-term steady-state DC bus-to-ground voltage is approximately $U_{\text{normal}} = 414.514$ kV. Therefore, the V-I characteristic of the baseline DB surge arrester should satisfy two requirements: first, it should not conduct significantly near the normal operating voltage; second, it should effectively clamp the voltage under fault overvoltage conditions. Based on these principles, the baseline V-I characteristic curve of the DB surge arrester is constructed, with a 1 kA protective level of 760 kV, as shown in Fig. 3.

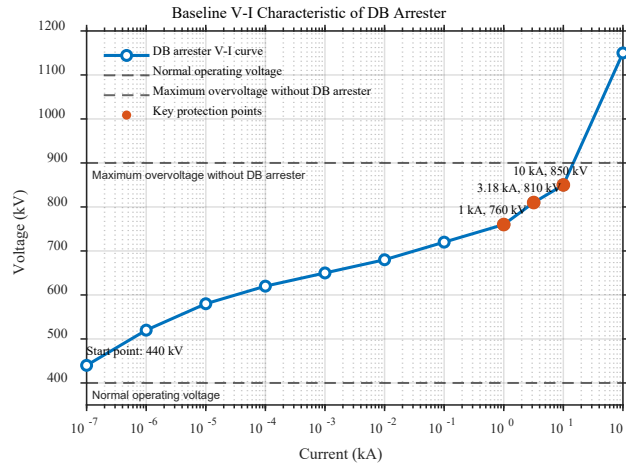


Figure 3: Baseline V-I characteristic of the DB arrester.

Under the baseline scheme, the maximum representative overvoltage corresponding to the DC bus pole-to-ground fault is $U_{\max, 0} = 822.890$ kV, and the maximum absorbed energy is $E_{\text{arr}, 0} = 12.005$ MJ. The corresponding voltage waveform and energy absorption results are shown in Fig. 4.

Based on the same rule, the AV and LV baseline voltage ratings are set to 700 and 750 kV, respectively. The resulting characteristic points are listed in Table 4. These baseline curves are used as the reference for V-I curve scaling and for the reference parameter set.

Table 4: Baseline arrester characteristic points.

Types	Voltage Rating/kV	Low Current Reference Voltage/kV	1 kA Residual Voltage/kV	3.18 kA Residual Voltage/kV	10 kA Residual Voltage/kV
AV	700	513.31	886.69	945.00	991.69
LV	750	549.98	950.03	1012.50	1062.53
DB	600	439.98	760.02	810.00	850.02

According to engineering design practice, the insulation level is rounded upward, with 50 kV used as the interval between candidate levels.

A full enumeration of all possible AV, LV, and DB parameter combinations would lead to a rapidly increasing number of EMT simulations. Therefore, a preliminary local screening is introduced only to reduce computational burden in this case study. As shown in Fig. 5, after the fault occurs, the voltage in the DB protection zone rises rapidly from its normal operating level and reaches the first overvoltage peak at around 1.50 s. Different λ values have a clear influence on the first peak amplitude and subsequent oscillation envelope. A larger λ leads to weaker arrester clamping and a higher first peak, while a smaller λ provides stronger voltage suppression but increases arrester current and energy absorption.

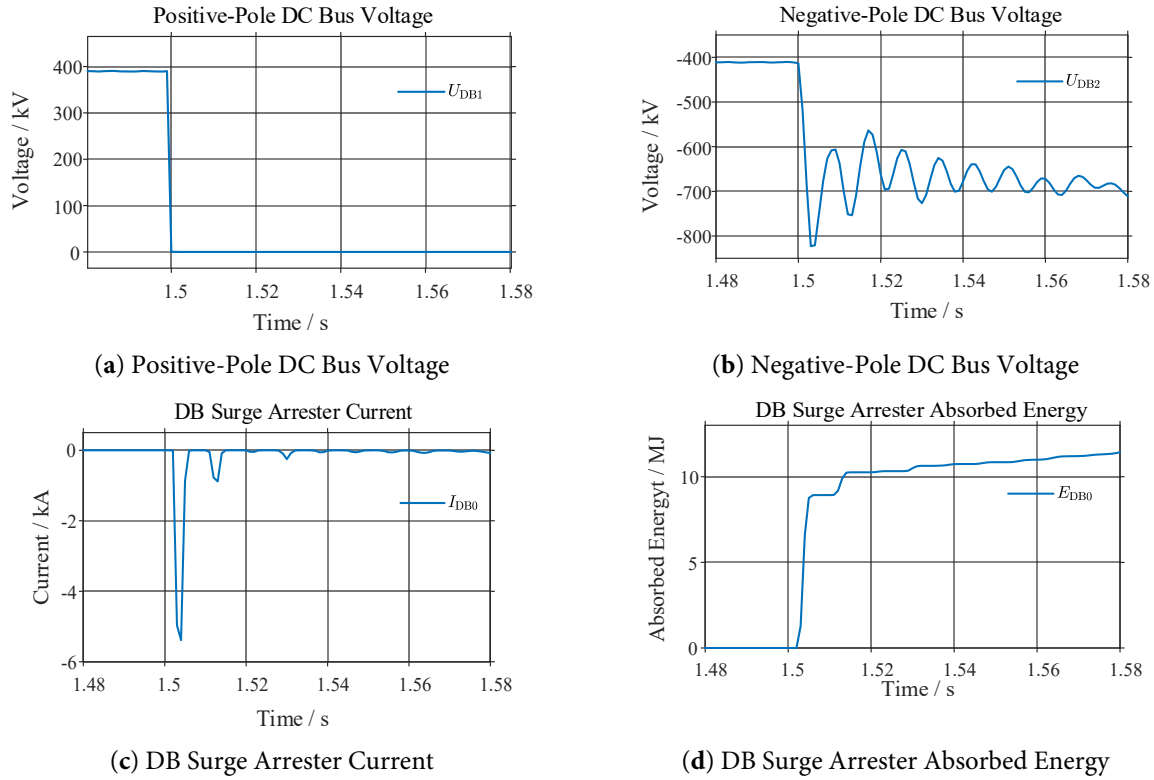


Figure 4: Waveforms under representative overvoltage with the baseline surge arrester configuration.

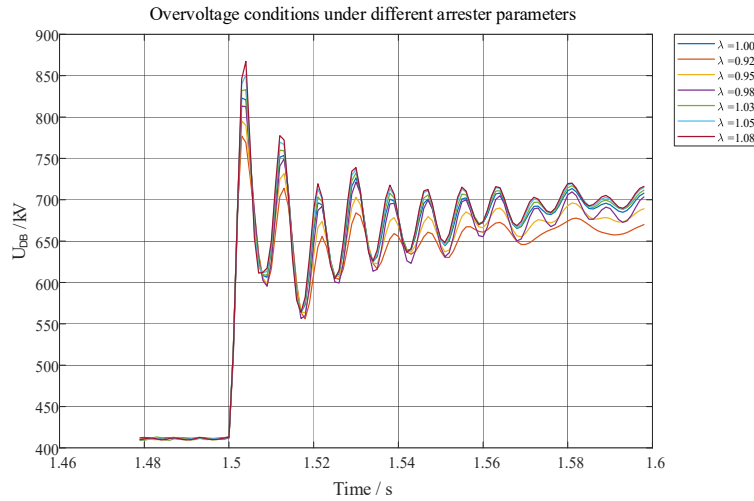


Figure 5: Overvoltage waveforms in the DB protection zone under different arrester parameters.

Specifically, when one arrester group is screened, the other two groups remain at their baseline settings, and two preferred settings are retained for each group. The retained settings are then recombined with the direct-margin reference of Q00 set to yield the nine parameter sets listed in Table 5. This screening is not an additional theoretical step of the proposed method. Rather, it is a practical simulation-saving measure for the case study.

For the final coordinated search, each of the nine parameter sets is simulated under the three zone-specific decisive faults. Thus, 27 simulations are used, and each simulation retains the AV three-phase,

LV six-arm, and DB two-pole voltage, current, and absorbed-energy records. This data set provides the representative overvoltage, TSI components, arrester current, and absorbed-energy inputs required by the model in Section 3. The main parameters required for the optimization calculation are listed in Table 6.

Table 5: Arrester parameter sets retained for coordinated optimization.

Set	λ_{AV}	n_{AV}	λ_{LV}	n_{LV}	λ_{DB}	n_{DB}
Q00	1.000	1	1.000	1	1.000	1
C01	0.950	1	0.950	2	0.975	2
C02	0.950	1	0.950	2	1.025	1
C03	0.950	1	0.950	1	0.975	2
C04	0.950	1	0.950	1	1.025	1
C05	1.050	1	0.950	2	0.975	2
C06	1.050	1	0.950	2	1.025	1
C07	1.050	1	0.950	1	0.975	2
C08	1.050	1	0.950	1	1.025	1

4.2 Optimization Results

Fig. 6 compares the peak voltages of the nine arrester parameter sets under the AV-, LV-, and DB-critical faults. The results confirm that each decisive fault primarily stresses its corresponding protection zone, but non-local interactions remain evident. Therefore, a design derived from a single common fault would not provide a sufficiently balanced basis for the coordinated AV–LV–DB insulation design.

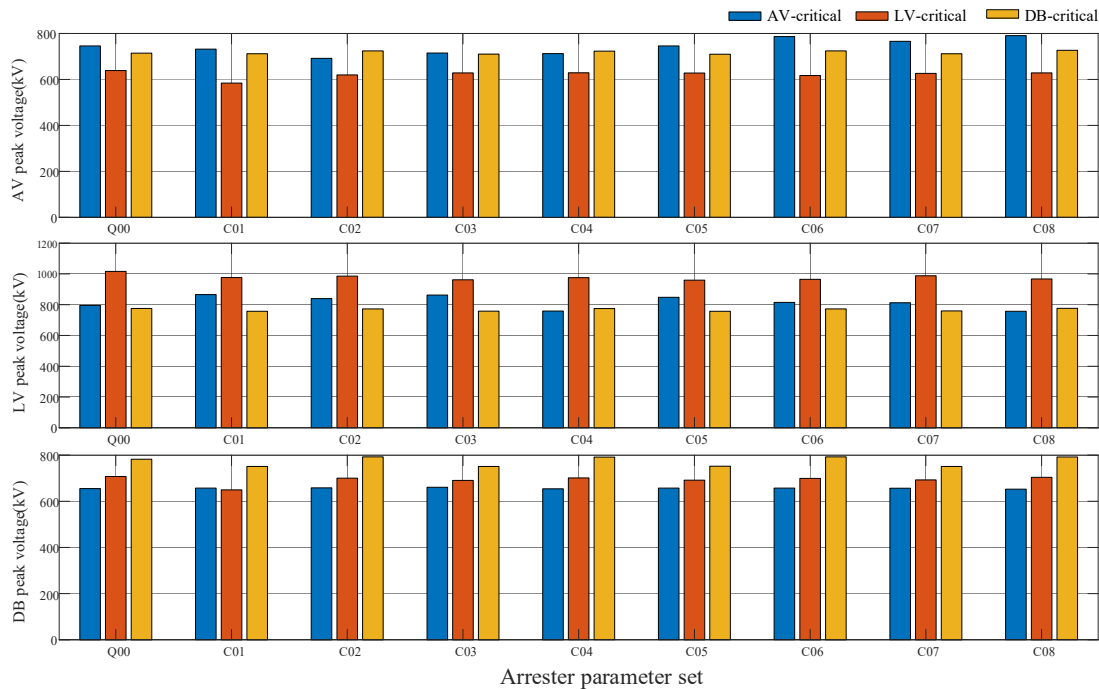


Figure 6: Peak overvoltages of nine arrester parameter sets under three decisive faults.

Table 7 further gives the cross-fault representative overvoltage and TSI envelopes. Among the nine parameter sets, C03 provides a balanced peak reduction: compared with Q00, the AV, LV, and DB representative peaks decrease from 745.8, 1016.6, and 782.5 kV to 714.8, 961.4, and 751.3 kV, respectively.

Table 6: Optimization parameters used in the coordinated insulation-design model.

Parameters	Value	Description
Installed quantities num_j	AV: 3, LV: 6, DB: 2	Topology-determined numbers of identical arrester assemblies.
Baseline voltage rating	AV: 700 kV, LV: 750 kV, DB: 600 kV	Baseline ratings used to construct the reference V-I curves.
Withstand-voltage catalogue	AV: 800–1100 kV, LV: 950–1400 kV, DB: 850–1200 kV, step = 50 kV	Discrete equipment withstand-voltage levels used in the complete design enumeration.
TSI weights	$\omega_U/\omega_D/\omega_A = 0.52/0.27/0.21$	TSI weights are obtained by FUCOM for peak voltage, wavefront steepness, and duration-related stress.
TSI correction exponent	$\omega = 0.40$	Exponent used to convert TSI into the equivalent safety margin K_{eq} .
Safety constraints	$K_{tar} = 1.15, 1.10 \leq K \leq 1.30, K_{eq,sys} \geq 1.15$	Direct-margin target and feasible insulation-margin constraints.
Arrester-body constraints	$k_E = 1.10, \gamma_I = 1.10, \gamma_E = 1.10$, leakage limits = 1 mA/column RMS and 10 mA/column peak	Energy, current, sharing, and normal-operation conduction constraints.
Cost levels and robust factor	$\xi \in \{L, M, U\}, \rho = 0.50$	Low, middle, and upper cost estimates. Total cost is formed from the middle estimate and upper-side uncertainty.
$C_{MOA,0}^\xi$	AV: 180/240/320, LV: 250/330/450, DB: 230/300/420 ($\times 10^4$ CNY)	Reference arrester costs at low/middle/upper levels.
C_{fix}^ξ	AV: 4800/6000/7200, LV: 6500/8000/10,000, DB: 2800/3500/4400 ($\times 10^4$ CNY)	Fixed equipment costs weakly related to insulation level.
C_{sen}^ξ	AV: 1350/1800/2400, LV: 6500/9000/12,000, DB: 900/1200/1680 ($\times 10^4$ CNY)	Insulation-sensitive costs at the baseline insulation level.
Reference risk cost	AV: 100/200/330, LV: 250/500/800, DB: 100/130/3200 ($\times 10^4$ CNY), $\nu_i = 0.05$ event/year	Baseline severe-event risk-cost calibration and annual severe-event frequency.
Cost sensitivity exponents	$\eta_{AV}/\eta_{LV}/\eta_{DB} = 1.20/1.20/1.50$, $\delta_{AV}/\delta_{LV}/\delta_{DB} = 0.40/0.45/0.60, \mu_j = 0.15$	Sensitivity coefficients for protective-level reduction, energy class and rated current capability.
Insulation and risk exponents	$\gamma_{AV}/\gamma_{LV}/\gamma_{DB} = 1.70/3.00/1.35$, $\beta_{AV}/\beta_{LV}/\beta_{DB} = 6/6/10$	Sensitivity coefficients of insulation cost and risk cost.

The TSI results shown in Fig. 7 supplies information not visible from peak values alone. For example, C03 reduces the LV representative peak, but its LV TSI is 1.0289 because the combined peak, steepness, and duration ratios under the controlling disturbance are slightly less favorable than those of Q00. Hence, the fault controlling U_{Tp} and fault controlling K_{eq} are reported separately in the following optimization tables.

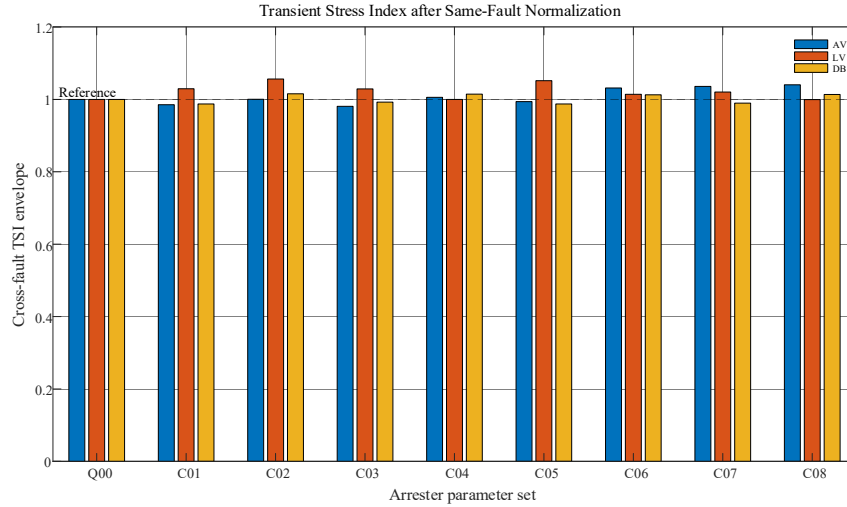


Figure 7: Cross-fault TSI envelopes after same-fault normalization.

Table 7: Cross-fault representative overvoltages and TSI envelopes.

Set	AV U_{rp}/kV	LV U_{rp}/kV	DB U_{rp}/kV	TSI _{AV}	TSI _{LV}	TSI _{DB}
Q00	745.8	1016.6	782.5	1.0000	1.0000	1.0000
C01	731.9	976.0	751.3	0.9853	1.0295	0.9874
C02	724.3	985.4	792.5	1.0005	1.0563	1.0155
C03	714.8	961.4	751.3	0.9810	1.0289	0.9925
C04	723.0	975.6	791.3	1.0058	1.0000	1.0145
C05	745.6	959.5	751.8	0.9940	1.0517	0.9875
C06	786.4	965.1	792.6	1.0316	1.0142	1.0127
C07	765.8	988.2	751.1	1.0360	1.0204	0.9897
C08	790.8	967.0	791.7	1.0403	0.9994	1.0136

The optimization variable is the complete insulation-coordination design, i.e., one arrester parameter set combined with the AV, LV, and DB withstand-voltage levels. The adopted catalogues generate 5040 combinations. After applying the conventional-margin limits, system-level equivalent-margin requirement, and arrester-body constraints, 134 designs remain feasible. Total life-cycle cost and $1/K_{eq,sys}$ are then used as the Pareto objectives.

As shown in Fig. 8 and Table 8, the Pareto front exhibits the expected safety-economy trade-off. Decreasing $1/K_{eq,sys}$ means improving the equivalent safety margin, but it usually requires a higher withstand level or a more expensive arrester arrangement. According to the normalized ideal-distance criterion, C03-U900-1150-950 is selected as the recommended coordinated design. Its arrester settings are $\lambda_{AV} = 0.95$ with one stack, $\lambda_{LV} = 0.95$ with one stack, and $\lambda_{DB} = 0.975$ with two parallel stacks. The selected equipment withstand levels are 900 kV for AV, 1150 kV for LV, and 950 kV for DB, giving $K_{eq,sys} = 1.2354$ and a total life-cycle cost of $35,759.7 \times 10^4$ CNY.

The Pareto set also provides engineering alternatives. C03-U850-1100-900 is the lowest-cost feasible boundary point, with $K_{eq,sys} = 1.1817$ and a total cost of $34,520.7 \times 10^4$ CNY, but it is located near the upper-left end of the front and is therefore overly economy-oriented. C03-U900-1200-950 offers a higher $K_{eq,sys}$ of 1.2762, but its total cost rises to $36,961.4 \times 10^4$ CNY. The selected C03-U900-1150-950 is closer to the engineering knee of the Pareto front, and it better demonstrates the coordinated optimization logic by improving safety over the Q00 direct-margin reference while still reducing total cost.

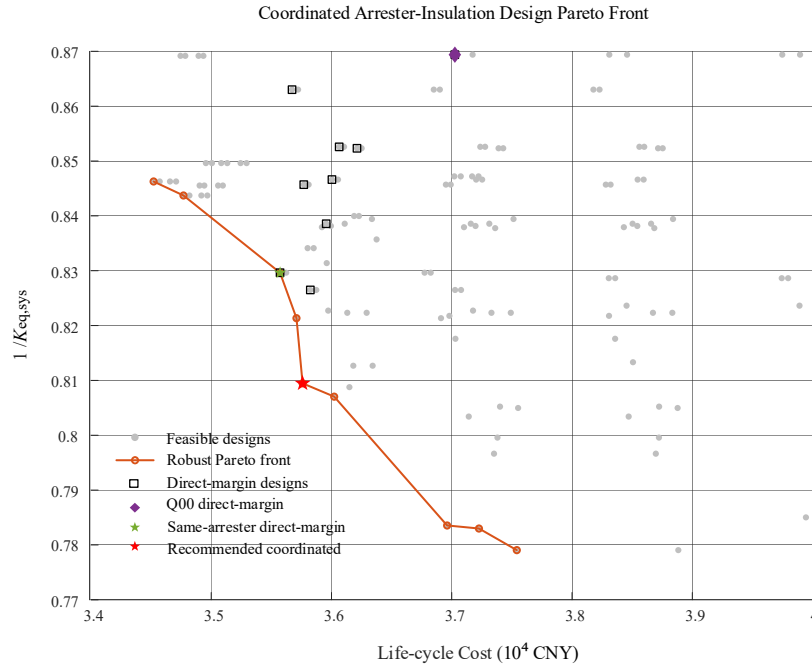


Figure 8: Robust Pareto front of the complete arrester–insulation design space.

Table 8: Robust Pareto-optimal complete insulation-coordination schemes.

Schemes	$U_{\text{with of}}$ AV/LV/DB/kV	$K_{\text{eq,sys}}$	$1/K_{\text{eq,sys}}$	Total Cost/ 10^4 CNY	Limiting Zone	Limiting Fault
C03-U850-1100-900	850/1100/900	1.1817	0.8463	34,520.7	LV	LV CRITICAL
C05-U900-1100-900	900/1100/900	1.1852	0.8437	34,769.3	LV	LV CRITICAL
C03-U850-1150-900	850/1150/900	1.2053	0.8296	35,572.6	AV	DB CRITICAL
C03-U900-1150-900	900/1150/900	1.2175	0.8213	35,708.9	DB	DB CRITICAL
C03-U900-1150-950	900/1150/950	1.2354	0.8095	35,759.7	LV	LV CRITICAL
C05-U950-1150-950	950/1150/950	1.2391	0.8070	36,022.4	LV	LV CRITICAL
C03-U900-1200-950	900/1200/950	1.2762	0.7835	36,961.4	AV	DB CRITICAL
C05-U950-1200-950	950/1200/950	1.2772	0.7830	37,226.1	AV	AV CRITICAL

4.3 Comparison between the Baseline Scheme and Recommended Scheme

To demonstrate the effectiveness of the proposed method, the direct-margin baseline scheme (Q00) is compared with the recommended scheme (C03-U900-1150-950) in Fig. 9, Q00 represents the conventional deterministic insulation-coordination reference with baseline arrester parameters and direct-margin withstand-level selection, whereas the recommended scheme jointly optimizes the arrester parameter set and zonal withstand levels under the same database and feasibility constraints.

As shown in Table 9, the recommended scheme uses the C03 arrester parameter set and the withstand-voltage combination of 900/1150/950 kV for AV/LV/DB. Compared with Q00, the representative overvoltages at AV, LV, and DB decrease from 745.8/1016.6/782.5 kV to 714.8/961.4/751.3 kV, respectively. Although the LV withstand level is reduced by one 50 kV catalogue step, the DB withstand level is increased by one step to maintain balanced protection on the DC side. Consequently, $K_{\text{eq,sys}}$ increases from 1.1502 to 1.2354, representing a 7.40% improvement.

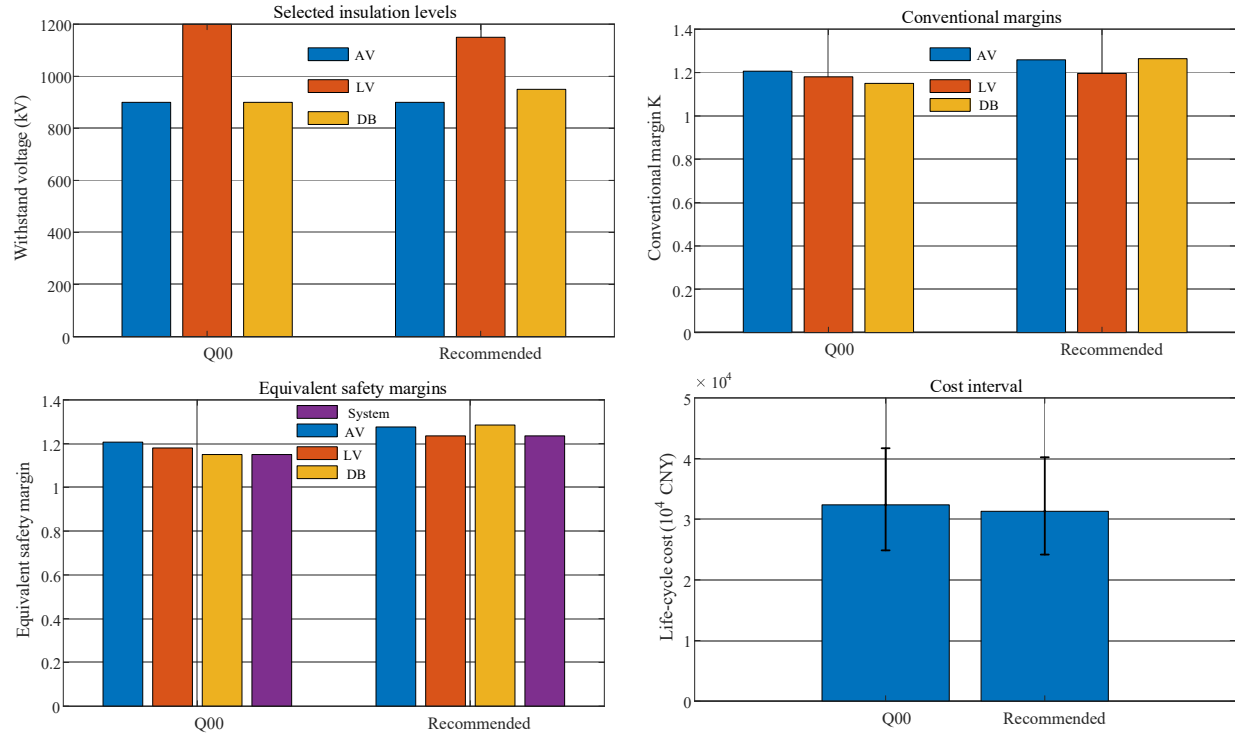


Figure 9: Recommended scheme versus the Baseline Scheme (Q00).

Table 9: System-level technical and economic comparison.

Schemes	U_{with} of AV/LV/DB (kV)	U_{rp} of AV/LV/DB (kV)	K_{eq} of AV/LV/DB	TSI of AV/LV/DB	Total Cost (10^4 CNY)
Q00	900/1200/900	745.8/1016.6/782.5	1.207/1.180/1.150	1.0/1.0/1.0	37,025.7
C03-U900-1150-950	900/1150/950	714.8/961.4/751.3	1.276/1.235/1.285	0.981/1.029/0.993	35,759.7

Table 10 further shows that the economic improvement is mainly contributed by the reduction in insulation-sensitive cost and risk cost. The recommended scheme increases arrester cost from 1112.4×10^4 CNY to 1443.3×10^4 CNY because of the stronger C03 arrester configuration, but the insulation cost decreases from $34,933.6 \times 10^4$ CNY to $33,738.1 \times 10^4$ CNY, and the risk cost decreases from 979.7×10^4 CNY to 578.4×10^4 CNY. As a result, the total life-cycle cost decreases from $37,025.7 \times 10^4$ CNY to $35,759.7 \times 10^4$ CNY, corresponding to a 3.42% cost reduction.

Table 10: Total life-cycle cost composition (10^4 CNY).

Scheme	Arrester	Insulation	Risk	Total
Q00 direct	1112.4	34,933.6	979.7	37,025.7
C03 coordinated	1443.3	33,738.1	578.4	35,759.7

The comparison results indicate that the proposed method enhances safety not by simply raising withstand levels, but by redistributing insulation withstand capabilities across protection zones based on actual arrester-clamped overvoltages and transient stresses. Therefore, the recommended scheme simultaneously improves the equivalent safety margin and reduces total life-cycle cost compared with

the Q00 direct-margin reference, demonstrating the effectiveness of coordinated arrester-parameter and insulation-level optimization.

5 Conclusion

To resolve the conflict between safety margin redundancy and high cost in the insulation coordination design of offshore VSC-HVDC converter station, this paper proposes a systematic coordinated optimization method. The main conclusions are as follows:

(1) The proposed multi-objective coordinated optimization method for surge arrester parameters and equipment insulation levels is feasible for the insulation coordination design of offshore VSC-HVDC converter station. Compared with the conventional experience-driven design methods, the systematic electromagnetic-transient-simulation-driven discrete multi-objective optimization method can facilitate the optimization procedure.

(2) The proposed novel transient stress index based equivalent safety margin considering peak over-voltage, and wavefront steepness can provide refined assessment of insulation safety margins to evolve from a single voltage amplitude to multiple transient stress factors. Absorbed energy and peak current are treated as independent arrester-body constraints to ensure the engineering feasibility of the selected scheme.

(3) Case study results for insulation coordination design of ± 400 kV offshore VSC-HVDC converter station demonstrate that the proposed systematic method achieves a better safety-economy balance than the direct-margin reference. The recommended scheme improves the system-level equivalent safety margin while reducing the total life-cycle cost, demonstrating that coordinated optimization of arrester parameters and equipment withstand levels can simultaneously enhance insulation safety and economic performance.

Future work will focus on developing key coefficient selection criteria and advanced algorithms for insulation coordination schemes across multiple VSC-HVDC converter stations, thereby extending the applicability of the proposed method to 500 kV and 800 kV VSC-HVDC systems. For practical engineering deployment, the final arrester selection should also be verified using manufacturer-specific V-I curves, TOV capability, rated energy, discharge-current capability, and current-sharing characteristics.

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Availability of Data and Materials: The data that support the findings of this study are available from the corresponding author upon reasonable request.

Ethics Approval: Not applicable.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations:

AC	Alternating current
DC	Direct Current
EMT	Electromagnetic transients
EMTP	Electromagnetic transients program
FUCOM	Full consistency method
HVDC	High-voltage direct current
MMC	Modular multilevel converter
MTBF	Mean time between failures
STATCOM	Static synchronous compensator
TOV	Temporary overvoltage
TSI	Transient stress index
VSC	Voltage-source-converter
VSC-HVDC	Voltage-source-converter-based high-voltage direct current

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