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Research on Excitation Power Supply Suitable for Total Harmonic Distortion Analysis (THDA) Detection of Hydrogen Production Equipment

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ABSTRACT: Total Harmonic Distortion Analysis (THDA) can precisely characterize internal performance degradation and fault evolution in electrolyzers, making it a key online condition-monitoring tool for improving overall energy efficiency and ensuring the extended lifespan of hydrogen production systems. THDA detection of hydrogen production equipment requires the injection of wideband perturbation signals across a wide frequency band (0.1 Hz–100 kHz) under a strong direct current (DC) bias. Traditional monolithic converters face significant challenges in balancing large-capacity DC output with wideband perturbation injection due to severe switching losses. To overcome this limitation, this paper proposes a broadband, high-dynamic-excitation power-supply solution based on a dual-power-supply parallel architecture with alternating current/direct current (AC/DC) impedance decoupling. At the hardware level, an improved bidirectional half-bridge topology with multi-level series matching inductors is proposed. Relying on the high-frequency passive low-pass filter network composed of a series inductor and an electrolyzer and the high-impedance isolation characteristics of the inductor current, this topology realizes the transient impedance decoupling of AC/DC parallel nodes while suppressing the chopping ripple of high-frequency switching, and blocks the current backflow caused by DC bus voltage disturbance. At the control level, a two-layer adaptive control strategy based on steady-state feature extraction is proposed for the characteristics of equivalent impedance drift of the electrolyzer under broadband sweep. This strategy relies on the discrete Fourier transform (DFT) to extract fundamental error features, introduces a nonlinear dead zone and anti-saturation mechanism, and realizes cross-decoupling and dynamic optimization of control parameters. Simulink simulation and STM32 hardware physical platform test results show that under conditions such as 0.1 Hz–100 kHz wideband steady-state scanning, cross-band stepping, and DC side disturbances, the system achieves millisecond-level dynamic response in the mid-to-high frequency band. In digital simulation, the full frequency band current Total Harmonic Distortion (THD) is strictly below 3%. In the hardware prototype tests, the fundamental amplitude steady-state tracking error is strictly controlled within 3%; The output current THD is below 2% within the core frequency band of 10 Hz–1 kHz, while in the edge frequency range (0.1 Hz–10 Hz and >1 kHz), due to hardware nonlinear constraints, it is as high as about 12%. This demonstrates the feasibility and effectiveness of the proposed research protocol.

KEYWORDS: Hydrogen production equipment; THDA detection; broadband excitation power supply; improved bidirectional half-bridge; steady-state feature extraction; adaptive control

1 Introduction

In the context of building new power systems, water electrolysis hydrogen production (such as Alkaline Water Electrolysis (AWE) and Proton Exchange Membrane (PEM)) is the core path to transition from

“green electricity” to “green hydrogen” [1–6]. However, megawatt-level hydrogen production equipment is prone to irreversible degradation such as plate corrosion or separator perforation under long-cycle fluctuating operating conditions [7]. Compared to conventional polarization curves and offline electrochemical impedance spectroscopy (EIS), Total Harmonic Distortion Analysis (THDA) detection technology overlays slight high-frequency AC sine perturbations on a DC baseline, effectively characterizing changes in the internal electrochemical reaction mechanisms of the equipment, making it an ideal means for online condition monitoring. The core prerequisite for implementing broadband (0.1 Hz–100 kHz) THDA detection is to build an excitation power supply capable of resisting strong DC bias and outputting high-precision sinusoidal perturbation signals.

In the fields of electrochemical impedance spectroscopy (EIS) and THDA online characterization of hydrogen production equipment, the technical routes for generating broadband perturbation signals mainly include the following categories, each with its own applicable boundaries and challenges when applying industrial-grade high DC bias:

Commercial EIS workstations and linear power amplifiers (PAs) are the standard tools for electrochemical impedance characterization in laboratory environments, offering extremely high control bandwidth and extremely low harmonic distortion. However, constrained by the operating principles of their linear amplification regions, the system’s energy conversion efficiency is relatively low, and thermal management costs are high when outputting large currents. Additionally, when directly undertaking the strong DC bias (e.g., tens to hundreds of amperes in industrial applications) of electrolyzers, hardware protection is quite challenging. Therefore, its scientific positioning mainly focuses on offline laboratory analysis or low-power testing.

To improve operational efficiency under heavy currents, a dual-power parallel architecture based on fully controlled switching devices with “AC/DC impedance decoupling” has emerged as a practical alternative for online impedance spectroscopy and THDA diagnostics [8,9]. Existing solutions typically rely on isolated transformers or passive filtering networks with fixed parameters (such as L or inductor-capacitor-inductor (LCL) filters). However, in such architectures, transformers are larger and struggle to transmit ultra-low frequency disturbances at 0.1 Hz; conversely, a single fixed passive filter network struggles to achieve optimal impedance matching across all frequency bands when facing ultra-wideband sweeps at 0.1 Hz–100 kHz. Additionally, when the low-impedance AC source is directly connected in parallel with a high-power DC bus, any transient voltage fluctuations on the main bus expose the system to severe DC backflow impacts [10–13]. Furthermore, without introducing advanced soft-switching topologies to mitigate high-frequency losses [14], the severe thermal stress under continuous high-frequency chopping becomes a major bottleneck for system reliability.

At the algorithmic level, dense frequency sweeping provokes wideband drift in the equivalent impedance of the electrolyzer, which severely limits the dynamic tracking capability of traditional fixed-parameter Proportional-Integral (PI) controllers. Conventional proportional-resonant (PR) controllers are also highly sensitive to system parameter jitter and frequency offsets, especially when operating under low carrier ratio conditions during wideband sweeps [15]. To overcome this, scholars have explored advanced strategies such as Repetitive Control (RC) and Model Predictive Control (MPC) [16]. The RC algorithm performs excellently in steady-state periodic signal tracking, but its internal delay mechanism during continuous frequency conversion scans leads to longer transient reconstruction times; MPC has fast dynamic response capabilities, but its control law relies heavily on precise high-frequency controlled mathematical models, while the polarization impedance of electrolyzers varies nonlinearly with operating conditions, increasing the difficulty of formulating an accurate predictive model.

To address technical bottlenecks in existing dual-power parallel solutions such as wide-band impedance mismatch, strong DC nonlinear backflow, and transient tracking hysteresis, this paper proposes a broadband high-dynamic excitation power supply system for THDA online testing. Compared with previous work, the main differences and innovations in this paper are: in terms of topological architecture, unlike traditional single passive filters, this paper proposes an improved bidirectional half-bridge topology with embedded multi-stage series matching inductors. This topology can solve full-frequency impedance decoupling and ripple suppression across 0.1 Hz–100 kHz through segmented matching, and effectively blocks energy backflow caused by transient disturbances in the main DC bus; In terms of control strategy, a dual-layer adaptive PI control strategy integrating discrete Fourier transform (DFT) steady-state feature extraction is proposed. By establishing nonlinear dead zone anti-oscillation and trapezoidal anti-saturation mechanisms, time-domain adaptive real-time optimization of control parameters under time-varying nonlinear loads is achieved. Finally, relying on Simulink's fully digital simulation and STM32-based physical prototype, this paper conducts in-depth benchmarking against the proposed solution and traditional architecture, verifying its superiority and robustness under wideband time-varying loads and strong DC side disturbance conditions. In summary, the main work of this paper is not to propose entirely new fundamental circuit topologies or control theories, but to explore a system-level integration solution combining hardware and software for testing the “high DC bias and wideband impedance drift” of hydrogen production equipment. On the hardware side, the combination design of multi-stage matching inductors and half-bridge topology balances the engineering needs of full-band perturbation transmission with suppressing transient backflow on the DC side; At the algorithm level, combining DFT steady-state feature extraction with conventional PI control reduces the controller's reliance on precise high-frequency nonlinear mathematical models of electrolyzers. This combined solution offers an engineering-feasible approach for inline THDA diagnostics of high-capacity hydrogen production systems, with relatively low computational costs and hardware complexity.

2 Materials and Methods

2.1 Topological Evolution and Parameter Design of Excitation Power Supply

In the dual-power supply parallel architecture with AC/DC impedance decoupling, the AC excitation power supply does not undertake the DC energy transmission task, and its core function is to inject disturbance signals across a wide frequency band. This chapter will delve into the impedance decoupling mechanism and hardware parameter boundaries of the main topology.

2.1.1 Failure Mechanism of the Traditional Bidirectional Half-Bridge in Parallel Systems

In applications that generate sinusoidal AC harmonics and require a bidirectional flow of energy, a bidirectional half-bridge DC-DC topology is a typical circuit structure. As shown in Fig. 1, the topology consists of a DC support capacitor and two fully controlled switches, i.e., Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), on the upper and lower bridge arms, with the midpoint directly connected to the load.

However, there are significant limitations when connecting the traditional bidirectional half-bridge directly to the THDA detection parallel system. On the one hand, under high-frequency Pulse Width Modulation (PWM), the output of the switching devices contains substantial high-frequency chopping ripple. If directly injected, this ripple not only interferes with the THDA spectrum analysis but also accelerates the degradation of the electrolyzer membrane modules. On the other hand, in a parallel architecture, if there is a lack of impedance buffer links, small voltage fluctuations or load transient sudden

changes on the main DC side will cause uncontrolled transient DC currents to surge into the AC power supply side, triggering thermal breakdown failures in the switching devices.

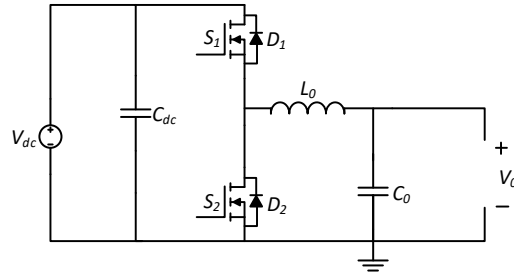


Figure 1: Traditional bidirectional half-bridge topology.

2.1.2 Decoupling Mechanism of Series Matching Inductor Improved Topology

In order to overcome the above problems, an improved excitation power supply topology is constructed: as shown in Fig. 2, the inductor L_0 is matched in series at the output load end of the traditional bidirectional half-bridge. The improved circuit is composed of DC side capacitor C_{dc} , upper bridge arm switch tube S_1 , lower bridge arm switch tube S_2 , and series output inductor L_0 , and the inductor end is connected to the parallel common node of the hydrogen production equipment and the main DC power supply.

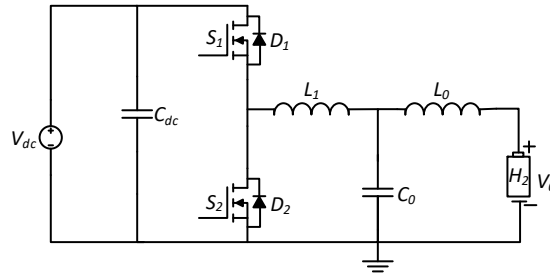


Figure 2: Improved bidirectional half-bridge topology.

In the improved topology, the series inductor L_0 and the load-side stray capacitor form a low-pass filter network on the one hand, which effectively attenuates the high-frequency current ripple caused by the switching chopper. On the other hand, according to the non-abrupt characteristics of the inductor current, L_0 significantly improves the transient impedance of the excitation power supply. This paper quantitatively evaluates the suppression ability of series inductors L_0 to suppress DC energy backflow by establishing a transient impedance model. Suppose a sudden voltage step disturbance ΔV_{dc} occurs on the main DC bus. Within the response delay time of the discrete control system Δt , the instantaneous voltage difference across the inductor is mainly dominated by this disturbance. According to the voltage-current differential relationship of the inductor, the rate of change of transient backflow current $di_{backflow}/dt$ can be expressed as:

$$\frac{di_{backflow}}{dt} = \frac{\Delta V_{dc}}{L_0} \quad (1)$$

By integrating the control delay time Δt , the maximum peak transient backflow current inflowing onto the AC inverter side is derived:

$$\Delta I_{\max} \approx \frac{\Delta V_{dc}}{L_0} \Delta t \quad (2)$$

In the control blind spot where the system control loop has not yet intervened, the peak inrush current $\Delta I_{\max}$ is inversely proportional to the matching inductance L_0 . Therefore, through a multi-level matching inductor network, the system improves transient impedance, effectively buffering voltage surges, thereby ensuring safe parallel operation of dual-power supply systems.

The improved half-bridge operates in continuous conduction mode (CCM) to track THDA commands. The switching period is set to T_s , and the circuit contains two core operating modes in a single cycle.

As shown in Fig. 3, in Mode 1, S_1 is on and S_2 is off.

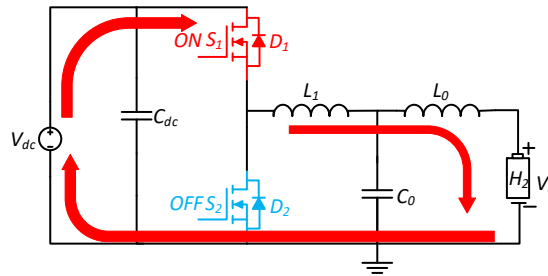


Figure 3: Improved bidirectional half-bridge topology working mode 1.

The DC bus voltage V_{dc} is applied to the series inductor and load, and according to Kirchhoff's Voltage Law (KVL), the circuit equation is:

$$V_{dc} - V_o(t) = L_o \frac{di_L}{dt} \quad (3)$$

where $V_o(t)$ is the load-side voltage at the parallel node. During this mode, the inductor current i_L exhibits a linear upward trend, and the system absorbs active power from the DC bus.

As shown in Fig. 4, in Mode 2, S_1 is off and S_2 is on.

The series inductor forms a freewheeling loop with the load, and the potential at the inductor end is lowered, and the equation evolves to:

$$-V_o(t) = L_o \frac{di_L}{dt} \quad (4)$$

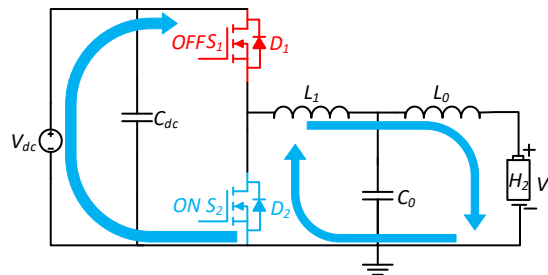


Figure 4: Improved bidirectional half-bridge topology working mode two.

The voltage polarity is reversed, and the current i_L shows a linear downward trend. By continuously adjusting the duty cycle d according to the sinusoidal law, the inductor current i_L can be controlled to track the THDA command on the macroscopic period.

2.1.3 Parameter Design of Multi-Level Matching Inductor Network

To establish a rigorous analytical transition from the switching model to the component selection rules, the physical roles of the inverter-side filter inductor (L_1) and the load-side matching inductor (L_0) must be clearly delineated. Specifically, L_1 serves as a static high-frequency carrier filter dedicated to locally smoothing the 1 MHz switching ripple. Conversely, L_0 functions as a dynamic impedance adapter and DC-blocking buffer. While the total high-frequency filtering capability is governed by their series combination, the dynamic impedance tracking for wideband perturbations is heavily dominated by L_0 . Therefore, to derive the strict boundary constraints for L_0 across different frequency bands, the following explicit engineering assumptions are established:

(1) Minimum inductance lower limit constraint based on high-frequency ripple suppression

In CCM, the peak-to-peak ripple of the inductor current during a switching cycle Δi_L is directly modulated by the duty cycle d . According to the inductance voltage equation of mode 1, we can obtain:

$$\Delta i_L = \frac{V_{dc} - V_o}{L_o} d T_s \quad (5)$$

Considering the ideal situation $V_o \approx dV_{dc}$, substituting the above equation gives:

$$\Delta i_L = \frac{V_{dc}}{L_o f_s} d(1 - d) \quad (6)$$

When the duty cycle $d = 0.5$, the maximum ripple amplitude is reached:

$$\Delta i_{L(\max)} = \frac{V_{dc}}{4 f_s L_o} \quad (7)$$

To prevent high-frequency chopping noise from obscuring weak electrochemical signatures during THDA spectrum analysis, the harmonic current ripple ratio—defined as the ratio of the maximum peak-to-peak ripple to the injected harmonic reference peak, I_m —must be restricted to below 5%. This threshold is governed by the Signal-to-Noise Ratio (SNR) requirements for feature extraction; in industrial electrolyzer applications, the most critical low-order harmonic responses (such as the 3rd harmonic) typically exhibit amplitudes of only 10%–15% relative to the fundamental perturbation. Clamping the high-frequency switching ripple strictly below 5% guarantees a theoretical SNR margin of at least +6 dB for the outer-loop DFT extraction algorithm. Consequently, the minimum inductance required to preserve spectral fidelity is derived as:

$$L_o \geq \frac{V_{dc}}{4 f_s \cdot \gamma I_m} \quad (8)$$

(2) The upper limit of the maximum inductance based on the dynamic climb of high frequency

In order to inject a high-frequency perturbation signal with an angular frequency ω_0 into the electrolyzer, the inverter power supply must have sufficient transient voltage output margin to overcome the dynamic inductance of the series inductor. In the worst case scenario where the output AC current reaches

its peak and the voltage of the system parallel node is at the highest potential (DC base bias voltage V_{load}), the half-bridge topology must be able to output a drive voltage higher than the back electromotive force (EMF). The inequality that satisfies it is:

$$\sqrt{V_{load}^2 + (\omega_0 L_0 I_m)^2} \leq V_{dc(max)} \cdot m_{max} \quad (9)$$

In the formula, m_{max} is the system's maximum linear modulation ratio (configured at 0.9 rather than the ideal saturation value of 1.0), intended to reserve a 10% unmodulated voltage buffer to compensate for: the forward on-state voltage drops of the power switches and isolating diodes; the DC equivalent copper resistance (RDCR) losses across inductors L_1 and L_0 ; and potential worst-case transient voltage sags on the DC bus V_{dc} . Additionally, setting 100 kHz as the maximum response frequency is governed by the sampling reconstruction limit of the digital control system. Under a 1 MHz carrier, a 100 kHz sinusoidal directive contains exactly 10 discrete sample updates per cycle. If the excitation frequency is pushed further, an excessively low carrier ratio will precipitate severe polygonal geometric distortion in the integrated waveform.

This inequality fundamentally bounds the dynamic tracking bandwidth in the high-frequency regime, from which the upper inductance constraint is derived as:

$$L_0 \leq \frac{m_{max} V_{dc(max)} - V_{load}}{\omega_0 I_m} \quad (10)$$

Based on the derived upper and lower boundary constraints, it is evident that a single fixed inductance cannot satisfy the filtering and dynamic requirements across the entire frequency spectrum simultaneously. Consequently, a multi-stage matching inductor cascade and an intelligent switching strategy must be implemented. However, the physical feasibility of this dynamic reconfiguration relies on a fundamental operational premise:

Quasi-Static Stepped-Sine Sweep: The safety of switching inductive branches via mechanical relays mid-operation assumes that the THDA diagnostic protocol executes a discrete stepped-sine sweep rather than a continuous wideband sweep. By injecting monochromatic frequencies sequentially, the master controller can execute relay state transitions strictly during zero-current crossing points or designated inter-frequency idle intervals, thereby completely avoiding inductive arc generation and transient bus shoot-through.

Governed by this operational assumption and the frequency characteristics of actual magnetic materials, the multi-stage inductor network is allocated into three distinct bands:

In the ultra-low and low-frequency band (0.1 Hz–2 kHz), the system operates at a low angular frequency ω . Here, the upper limit constraint is relatively loose, making switching ripple suppression the primary contradiction. Therefore, the system engages a large-capacity silicon steel core inductor network to strictly clamp the chopping ripple within 5%. In the mid-frequency band (2 kHz–20 kHz), dynamic inductive reactance becomes prominent. The system switches to amorphous nanocrystalline inductors to balance ripple suppression efficiency with the required dynamic current slew rate. Finally, in the high and ultra-high-frequency band (20 kHz–100 kHz), the upper limit constraint contracts sharply as ω surges exponentially. At this stage, the system bypasses the main networks and retains only a micro-Henry level high-frequency ferrite air-core coil, maximizing the transient voltage output margin and preventing high-frequency waveform collapse.

2.1.4 STM32 Hardware Implementation for Broadband Signals

The system uses STMicroelectronics' (ST) high-performance Cortex-M7 core microcontroller STM32H7-50V8T6 (clocked up to 480 MHz) as the underlying hardware computing and control core. Given the ultra-wideband perturbation requirement (0.1 Hz to 100 kHz), the system must execute the sliding discrete Fourier transform (SDFT) feature extraction and the complex floating-point calculations for the dual-layer adaptive PI in parallel within a short discrete control cycle. The chip's built-in hardware floating-point unit (FPU) and Digital Signal Processing (DSP) instruction set provide abundant underlying computing power support for real-time convergence of high-frequency control algorithms and high-precision refresh of duty cycles.

In the signal sensing link, the system needs to sample the transient features of the parallel nodes with high frequency and high precision. The AC inductor current (dynamic feedback amount of the inner loop) and the voltage at the load end (status monitoring and feedforward compensation parameters) are the core acquisition objects. The bottom layer uses a high-bandwidth Hall sensor to extract the original signal, and after accurate level translation, scaling, and low-pass anti-aliasing filtering conditioning through a differential operation amplification circuit with a high common-mode rejection ratio, it enters the 16-bit high-speed analog-to-digital converter (ADC) inside the microcontroller.

In order to avoid high-frequency noise interference caused by switching choppers, the microcontroller uses the trigger event mechanism of the advanced timer to realize the hardware synchronous trigger sampling of the ADC. The sampling point is configured in the middle of the PWM cycle with stable switch state and minimal electromagnetic interference to obtain clean and true average current and voltage values.

In the bidirectional half-bridge topology, the upper bridge arm switch tube (S_1) and the lower bridge arm switch tube (S_2) must be strictly mutually exclusive. If the two are turned on at the same time, it will cause a shoot-through short circuit on the DC bus, instantly burning the MOSFET device. Therefore, the STM32H750V8T6 needs to generate a set of complementary PWM-driven waveforms with dead zones. Complementary waveform generation utilizes an advanced control timer inside the microcontroller to configure it in center-aligned mode.

In the power-driven execution link, the system disables software delay, which is susceptible to interrupt jitter, in response to the risk of pass-through short-circuiting in the bidirectional half-bridge topology, and instead uses the hardware dead-time generator, specifically the Break and Dead-Time Register (BDTR), built into the STM32 Advanced Timer to accurately insert hundreds of nanoseconds of pass-through dead time at the edge of the generated logic-complementary PWM wave. The control signals are then level-shifted and amplified through an isolated gate driver, safely and efficiently driving the MOSFET to execute high-frequency switching.

Based on the STM32H750V8T6 digital signal acquisition and PWM complementary drive architecture shown in Fig. 5, the system establishes a closed-loop data link from "signal sensing" to "power execution" at the hardware level, laying a solid underlying hardware foundation for the subsequent implementation of complex frequency-domain adaptive PI control algorithms.

2.2 Adaptive PI Control Algorithm Based on AC Steady-State Feature Extraction

For broadband nonlinear loads, the traditional fixed-parameter PI controller exhibits severe amplitude attenuation and phase lag when tracking high-frequency sinusoidal references. Conventional proportional resonance (PR) controllers are more sensitive to system parameter jitter and frequency offset. In view of the severe drift of the equivalent impedance of hydrogen production equipment under parallel conditions, this paper reduces the dependence of the controlled object on the accurate high-frequency mathematical

impedance model, and proposes a double-layer adaptive PI control algorithm based on AC steady-state error feature extraction.

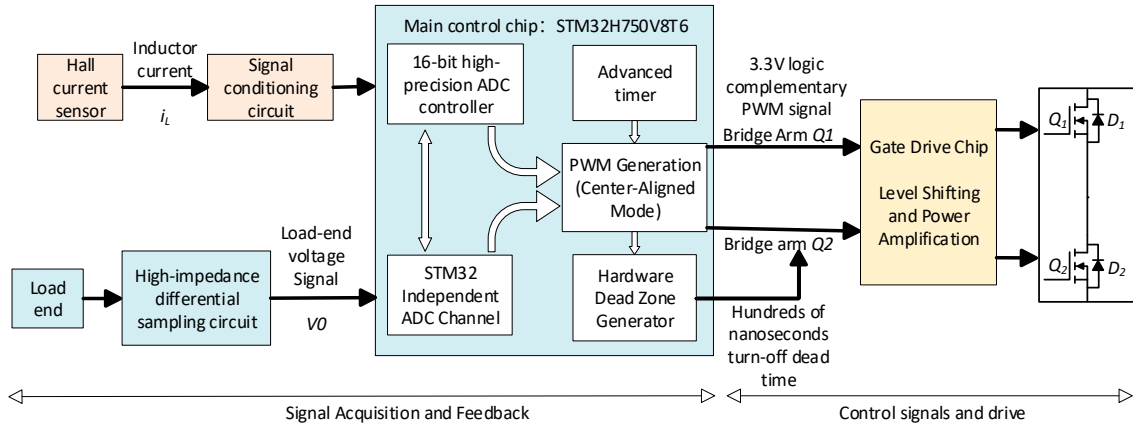


Figure 5: Structure diagram of wideband THDA excitation power control system based on STM32H750V8T6.

2.2.1 Challenges and Algorithm Architecture of Excitation Power Control

Ideally, the output AC current of a closed-loop control system should be strictly consistent with the THDA reference directive in amplitude and phase. However, in actual dual-supply parallel operation, the wide-frequency inductance of the series inductor and the nonlinear load characteristics of the main DC bus will introduce unknown phase hysteresis and gain attenuation to the system.

Therefore, a two-layer control architecture composed of “underlying fast transient PI tracking” and “outer steady-state feature adaptive compensation” is designed.

The block diagram of the structure of the closed-loop control system shown in the Fig. 6 shows the core logic of the architecture: fast transient closed-loop tracking of high-frequency waveforms is realized by using the underlying conventional PI control; At the same time, a DFT module is introduced in the outer ring to extract the fundamental amplitude and phase characteristics of the actual output current online, and the proportional gain (K_p) and integral gain (K_i) of the underlying PI controller are adaptively and dynamically tuned according to the real-time steady-state deviation.

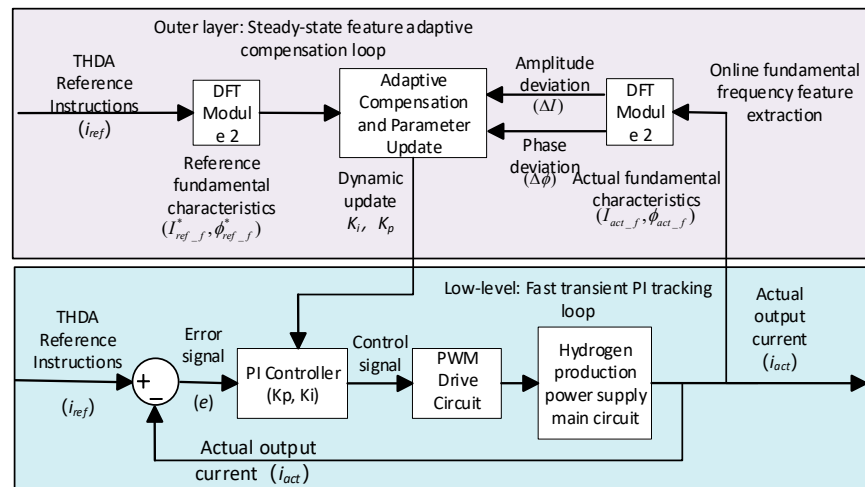


Figure 6: Dual-layer control architecture of excitation power supply for hydrogen production equipment.

2.2.2 Online Extraction and Preprocessing of AC Characteristic Signals

To obtain an accurate basis for adaptive adjustment, the microcontroller needs to acquire the steady-state characteristics of the output current in real time. The system utilizes high-speed ADC to sample the actual current $i_L(t)$, and extracts the AC features at the target frequency (f_0) in real time through SDFT: the true fundamental peak of the output sinusoidal current is obtained through amplitude extraction (A_{meas}); and the phase delay angle of the extracted output current relative to the reference command is obtained through phase extraction (ϕ_{meas}), using the zero-crossing point of the THDA reference command $i_{ref}^*(t)$ as the baseline.

In order to prevent high-frequency switching noise or DC-side bus step change from causing transient spike interference in feature extraction, which leads to severe oscillation of the adaptive parameters, the algorithm introduces a first-order low-pass filter smoothing mechanism for the extracted feature values:

$$I_{act_f}^{flt}(k) = \alpha I_{act_f}^{raw}(k) + (1 - \alpha) I_{act_f}^{flt}(k - 1) \quad (11)$$

where α is the filter weight coefficient, $I_{act_f}^{raw}(k)$ is the original feature extraction value of the current sampling period, $I_{act_f}^{flt}(k)$ is the final smoothed value after filtering, and k is the current discrete sampling period. This mechanism enhances the strength of the feedback signal while preserving the steady-state trend.

2.2.3 Design and Implementation of Adaptive PI Compensation Law

Based on the extracted smoothed feature values, the algorithm calculates the amplitude tracking error e_A and the phase tracking error e_ϕ under the current operating conditions. Since THDA detection requires tracking without phase shift, the target phase difference is $\phi_{ref} = 0$.

$$\begin{aligned} e_A &= A_{ref} - A_{filt}(k) \\ e_\phi &= \phi_{ref} - \phi_{filt}(k) \end{aligned} \quad (12)$$

In the dynamic mechanism of the PI controller tracking the AC signal, the proportional gain K_p dominates the system's response amplitude to transient deviations, which is directly related to the amplitude gain of the output AC waveform; while the integral gain K_i determines the system's ability to eliminate steady-state errors, directly affecting the phase lead/lag characteristics of the current waveform.

Accordingly, this paper designs the parameter adaptive update law of cross-decoupling, and the mathematics of its compensation mechanism are shown in the following Fig. 7:

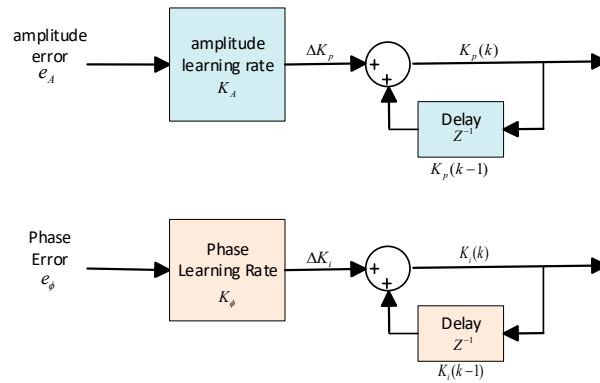


Figure 7: Adaptive update law of cross-decoupling parameters based on steady-state error.

As shown in the schematic, the controller's parameter update logic is:

$$\begin{aligned} K_p(k) &= K_p(k-1) + \Delta K_p \\ K_i(k) &= K_i(k-1) + \Delta K_i \end{aligned} \quad (13)$$

The step update amount is determined by the following formula:

$$\begin{aligned} \Delta K_p &= K_A \cdot e_A \\ \Delta K_i &= K_\phi \cdot e_\phi \end{aligned} \quad (14)$$

where K_A and K_ϕ are the adaptive adjustment learning rates for the amplitude and phase errors, respectively. When the output amplitude fails to meet the target, K_p is adaptively increased; when the output phase lags, K_i is adaptively increased to compensate for the phase angle.

In actual parallel electrolyzer networks, small quantization errors and sensing noise are inevitable. To translate the aforementioned theory into robust microcontroller execution code, a complete logic framework incorporating dead-zones and limits is designed. To prevent steady-state limit cycles caused by the frequent adjustment of the adaptive mechanism near the target value, a nonlinear dead-zone function is introduced into the error calculation link:

$$\begin{aligned} \Delta K_p &= \begin{cases} K_A \cdot e_A, & |e_A| > \varepsilon_A \\ 0, & |e_A| \leq \varepsilon_A \end{cases} \\ \Delta K_i &= \begin{cases} K_\phi \cdot e_\phi, & |e_\phi| > \varepsilon_\phi \\ 0, & |e_\phi| \leq \varepsilon_\phi \end{cases} \end{aligned} \quad (15)$$

(where ε_A , ε_ϕ are the set amplitude and phase tolerance dead-zone thresholds, respectively). The parameters are updated only when the steady-state error exceeds the dead-zone boundaries. Meanwhile, to ensure system stability under extreme disturbances, hard saturation limits $[K_{\min}, K_{\max}]$ are applied to the updated K_p and K_i to prevent excessive parameter drift.

After completing the parameter update, the underlying PI controller performs specific duty cycle operations. In order to improve the accuracy of high-frequency operations and eliminate the discretization error caused by conventional rectangular integration, the system adopts the trapezoidal integration rule:

$$Integral(k) = Integral(k-1) + \frac{[e(k) + e(k-1)] \cdot T_s}{2} \quad (16)$$

At the same time, in order to cope with the problem of deep saturation of the actuator (PWM duty cycle) caused by the rapid accumulation of integration terms at the moment of startup or when the system is disturbed by step, the algorithm embeds an anti-windup strategy. When the accumulated integral touches the set upper and lower limits, the growth of the integral term will be frozen immediately.

The final control output is:

$$u(k) = K_p(k) \cdot e(k) + K_i(k) \cdot Integral(k) \quad (17)$$

The algorithm combines classical frequency domain feature analysis with modern time-domain adaptive optimization, which reduces the dependence on accurate mathematical impedance models under parallel

hydrogen production conditions. It not only realizes broadband harmonic and low-latency tracking, but also provides fault tolerance and robustness for multi-device parallel connection in complex environments.

3 Results

In order to comprehensively evaluate the effectiveness of the proposed software-hardware collaborative topology and adaptive algorithm under harsh operating conditions, this chapter relies on the MATLAB/Simulink all-digital simulation platform and high-power physical prototypes to carry out tests, and compares them with the traditional fixed-parameter PI control strategy in depth.

3.1 Simulink Simulation System Modeling and Key Parameter Design

To ensure the authenticity and practical applicability of the simulation results, an accurate discrete control model is built in the Simulink environment. The parameter design of the simulation system strictly adheres to the boundary constraints and stability criteria established in Section 2.

3.1.1 Design of Power Main Circuit and Alkaline (ALK) Electrolyzer Impedance Parameters

The power main circuit uses an improved bidirectional half-bridge topology based on CCM. In order to ensure the smooth injection of high-frequency AC perturbation signals, a switching frequency of 1 MHz is selected for simulation to provide sufficient transient voltage climb margin for 100 kHz perturbation injection. The key simulation parameters of the main circuit and the controlled object are shown in Table 1.

Table 1: Excitation power main circuit and ALK load simulation parameter table.

Circuit Parameters	Simulation Setpoints
Main DC bus voltage V_{dc}	120 V
High frequency switching frequency f_s	1000 kHz
DC bus support capacitor C_{dc}	10 μ F
Inverter side filter inductor L_1	1E-5 H, 1E-4 H, 1E-3 H, 1E-2 H, 1E-1 H
AC filter capacitor C_0	1E-5 F, 1E-4 F, 1E-3 F
The load side is matched with inductor L_0	1E-7 H, 1E-5 H, 1E-4 H, 1E-3 H, 1E-2 H, 1E-1 H
AC perturbation amplitude I_{ref_m}	± 10 A
ALK ohmic internal resistance R_s	0.109 Ω
ALK charge transfer resistance R_{ct}	0.294 Ω
ALK electric double layer capacitor C_{dl}	0.01 F

3.1.2 Discrete Adaptive Controller Parameters and Solver Settings

In order to realistically simulate the digital computing environment of the STM32 microcontroller, the control loops in the simulation model are all built using discrete-time modules, and the underlying PI actuators with trapezoidal integration and anti-saturation logic are embedded. The sampling frequency of the outer DFT feature extraction algorithm is synchronized with the PWM carrier frequency.

The parameters of the traditional PI controller (K_{p_trad} , K_{i_trad}) are based on the impedance of the ALK electrolyzer in the middle and low frequency bands, and the optimal fixed gain obtained by the classical frequency response method is used, and it remains constant in all subsequent broadband sweep and step change tests.

At the same time, the adaptive PI controller proposed in this paper will use the nominal gain as the initial starting point for optimization ($K_{p0} = K_{p_trad}$, $K_{i0} = K_{i_trad}$), and dynamically update it in real time according to time-varying inductance and nonlinear perturbation during operation. The specific algorithm control and simulation solver parameter configuration of the system are shown in Table 2.

Table 2: Discrete controller comparison group and simulation solver key parameter table.

Parameter Name	Simulation Setpoints
Simulation solver step T_{step}	100 ns
Traditional PI ratio gain $K_{p,trad}$	0.5
Traditional PI integral gain $K_{i,trad}$	1.5
Adaptive PI initial proportional gain K_{p0}	0.5
Adaptive PI initial integral gain K_{i0}	1.5
Amplitude adaptive learning rate K_A	0.02
Phase adaptive learning rate K_φ	1.5
Nonlinear dead zone thresholds $\varepsilon_A, \varepsilon_\varphi$	0.15 A, 0.5°

3.1.3 Test Scenario Design

In order to comprehensively observe the dynamic characteristics of the controlled system under harsh working conditions, this paper designs three simulated operating scenarios for the actual operating mechanism of the ALK electrolyzer, which will be compared and verified one by one in the following subsections.

Case 1: The test command frequency is 0.1 Hz, 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz respectively to verify the steady-state characteristics of the power supply system at different frequencies.

Case 2: At $t = 0.05$ s, two sets of frequency steps of 1 kHz–100 Hz and 1 kHz–10 kHz are injected to comprehensively test the anti-collapse and dynamic reconstruction ability of the algorithm in response to the sudden increase of high-frequency induction resistance.

Case 3: In order to simulate the transient voltage of the hydrogen production bus precipitated by severe active power fluctuations from renewable energy sources in parallel operation, a high-power DC voltage source is used to directly apply step disturbances. When running to $t = 0.03$ s, two step disturbances were introduced, the bus voltage suddenly rose from 60 V to 65 V and from 60 V to 55 V. The dynamic anti-disturbance stiffness of the system and the robustness of the series inductor to block DC backflow are directly tested.

3.2 Simulink Comprehensive Dynamic Testing and Anti-Interference Verification

A fully digital simulation model of the dual-power parallel excitation system of hydrogen production equipment is built on the MATLAB/Simulink platform, and the main DC fundamental power supply, each gear contactor and corresponding inductor network, as well as the underlying high-frequency PWM driver and the outer DFT feature extraction algorithm are reproduced.

3.2.1 Comprehensive Evaluation of Wideband Steady-State Perturbation Generation

The excitation frequency required for THDA diagnosis in hydrogen production equipment spans several orders of magnitude. The simulation scenario is configured for a wideband sweep test, in which the amplitude of the target AC perturbation command is kept constant, and the steady-state following test is carried out on 7 typical frequency points of 0.1 Hz, 1 Hz, 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz respectively with decades as the step. The system extracts the real steady-state waveform data at each frequency point and plots the distribution characteristic curve of Total Harmonic Distortion (THD) (as shown in Fig. 8) in the whole frequency band.

Under broadband frequency sweep conditions, the impedance of the controlled object drifts drastically with frequency. The control strategy proposed in this paper achieves broadband adaptation by relying on the intelligent matching of multi-stage inductors and the adaptive algorithm. Based on the analysis of the broadband full-band THD characteristic curve: in the low-to-mid frequency band (0.1 Hz–1 kHz), the

THD value of the system fluctuates between 0.45×10^{-3} and 1.0×10^{-3} . This indicates that the underlying trapezoidal anti-windup actuator, combined with the large-capacity inductor of the low-frequency stage, can effectively suppress the switching chopping ripples that continuously accumulate over long periods. In the ultra-high frequency band (10 kHz–100 kHz), the system's inductive reactance increases exponentially as the excitation frequency rises. However, with the compensation from the outer DFT module—which extracts fundamental wave features in real time and adaptively increases the proportional gain—the system overcomes the limitation of the high-frequency current slew rate. Although the THD increases to some extent due to digital discretization, it is still strictly clamped below 3.0×10^{-3} at the highest point of 100 kHz.

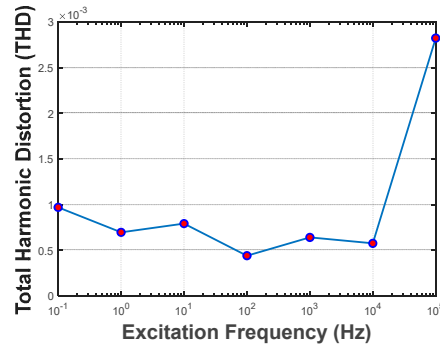


Figure 8: Wideband high-dynamic excitation power supply full-band THD characteristics.

Based on the above frequency domain characteristic data, the perturbation current output by the system shows a clean sine signal whether operating at an ultra-low frequency of 0.1 Hz (with a 10-s period) or an ultra-high frequency of 100 kHz (with a 10-microsecond period). The successful verification of this scenario achieves the hardware and algorithm basis for wideband detection under DC bias.

3.2.2 Comparison of Dynamic Reconstruction under Sudden Changes in Frequency Bands

The actual online THDA sweep test requires fast and intensive switching between different frequency points, which requires the excitation power supply to have fast transient reconstruction capabilities and cross-band adaptability. In order to fully verify the dynamic response bandwidth of the algorithm, the simulation setting scenario 2: At 0.05 s, the THDA target instruction frequency undergoes two sets of step changes (1 kHz to 10 kHz and 1 kHz to 100 Hz). The traditional fixed-parameter PI controller and the adaptive PI controller in this paper are subjected to parallel comparison tests, and the waveform and amplitude envelope extraction results are shown in Figs. 9–11.

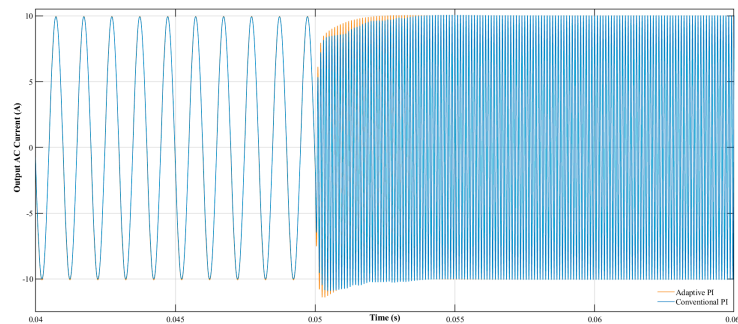


Figure 9: Comparison of the tracking performance of traditional fixed parameter PI and adaptive PI under frequency 1 kHz–10 kHz step change.

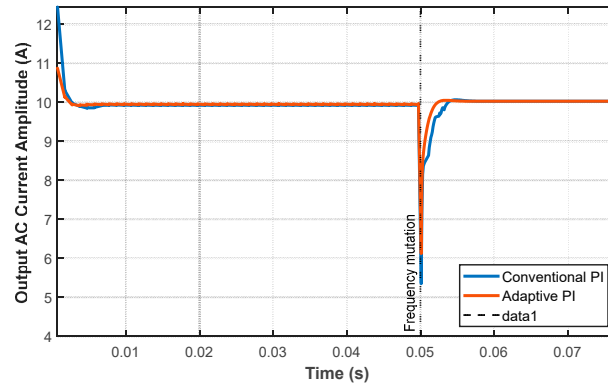


Figure 10: Amplitude characteristics of traditional fixed parameter PI and adaptive PI under frequency 1 kHz–10 kHz step change.

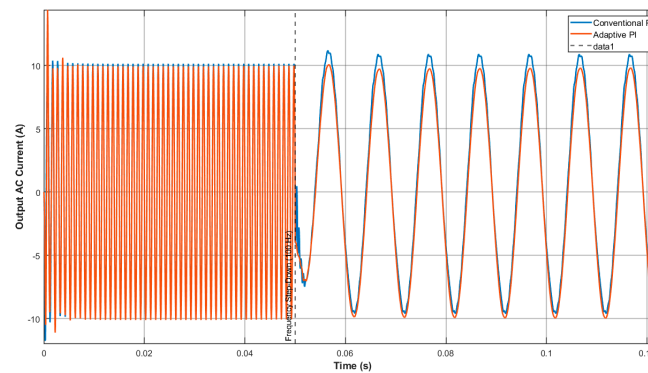


Figure 11: Comparison of the tracking performance of traditional fixed parameter PI and adaptive PI under frequency 1 kHz–100 Hz step change.

Combined with the high-frequency dense waveform in Figs. 9 and 10 and the extracted amplitude envelope trajectory, it can be seen that when the command frequency changes suddenly, the inductance of the loop soars instantly, requiring the controller to instantaneously output an exceptionally high driving voltage. Due to the lack of parameter adaptive adjustment mechanism, the fixed proportional gain cannot provide sufficient transient driving force due to the lack of a fixed parameter PI controller. From Fig. 10, it can be concluded that at the moment of 0.05 s step change, the output current amplitude under the traditional control decreases significantly (from 10 A to about 5.5 A, with an attenuation of 45%). Due to the inherent integration lag effect, its envelope experienced an oscillatory climb of more than 5 ms before returning to steady state.

In contrast, the adaptive PI control strategy proposed in this paper shows strong dynamic reconstruction ability. At the moment when the initial amplitude attenuation is triggered by the frequency surge, the algorithm senses the steady-state amplitude deviation through the outer ring DFT, and quickly activates the dynamic update law to greatly increase the underlying proportional gain in real time. This mechanism completely compensates for the gain attenuation in about 2 ms, allowing the current envelope to be pulled up at a high slope and stabilized at the target amplitude of 10 A.

Combined with Fig. 11, it can be seen that when the excitation frequency drops suddenly, the inductive reactance of the system decreases instantaneously. The traditional PI controller accumulates too large integral terms to overcome the inductive reactance in the early 1 kHz high-frequency stage, and cannot be

released quickly at the moment of frequency drop, resulting in obvious integration saturation overshoot and envelope distortion at the waveform junction. The adaptive PI algorithm can accurately sense the slowdown of phase and frequency, quickly converge gain, and realize the seamless transition of the envelope under the jump across orders of magnitude frequency bands.

3.2.3 Comparison of Anti-Disturbance Stability under the Sudden Change of Load Impedance on the Main DC Side

The most rigorous operational challenge for dual-power parallel systems stems from nonlinear electrical disturbances on the main DC side. This kind of disturbance can easily break through the AC inverter and cause energy backflow. Simulation setting scenario 3: At 0.03 s, the main DC bus voltage (initial 60 V) drops to 55 V and jumps to 65 V, respectively. This comprehensively tests the dynamic stiffness and robustness of the system in response to forward and reverse DC shocks.

When the bus voltage drops by 5 V in 0.03 s, the effective potential difference of the system-driven electrolyzer will deviate instantly. Combined with Figs. 12 and 13, it can be seen that due to the lack of sensing and dynamic adjustment ability of the system model, the output current has a positive runaway overshoot, and its peak instantaneously rises to about 19 A, resulting in a fault-level current shock that is nearly doubled, accompanied by a long-term high-frequency chopping ripple. In contrast, the proposed adaptive PI algorithm instantly detects the steady-state error breaching its outer dead-zone threshold, initiating dynamic parameter updates to introduce active damping, which strictly clamps the initial overshoot spike at about 12 A, and absorbs the impact energy within 3 ms, quickly pulling the waveform back to the baseline of 10 A.

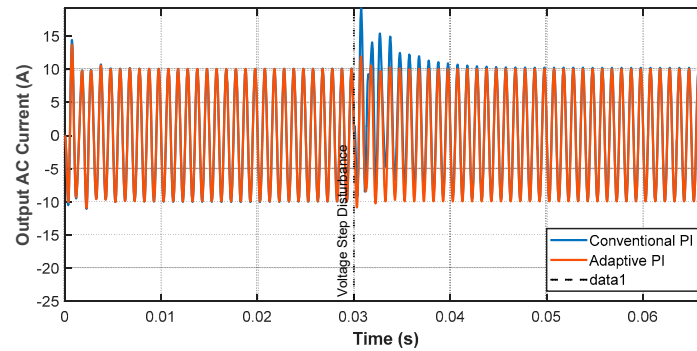


Figure 12: Comparison of the tracking performance of the traditional fixed parameter PI and the adaptive PI in the main DC bus voltage dropping from 60 V to 55 V.

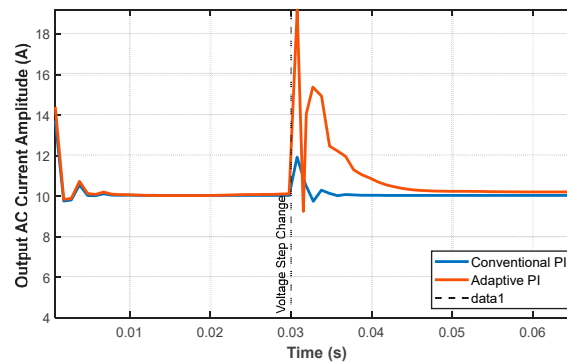


Figure 13: The amplitude characteristics of the traditional fixed parameter PI and the adaptive PI drop from 60 V to 55 V in the main DC bus voltage.

When the bus voltage jumps to 65 V in 0.03 s, the 5 V transient dropout attempts to inject DC energy into the AC excitation supply. Combined with Figs. 14 and 15, it can be seen that under this condition, the output waveform under traditional PI control is severely disrupted, and the current envelope is severely dropped (down to about 5.3 A), and the recovery process is slow. In the face of the same backflow shock, the adaptive PI control strategy relies on an instantaneously increased anti-disturbance gain to effectively buffer the voltage inrush. The current drop was significantly compressed (only down to about 8.8 A) and reconstituted in 2 ms.

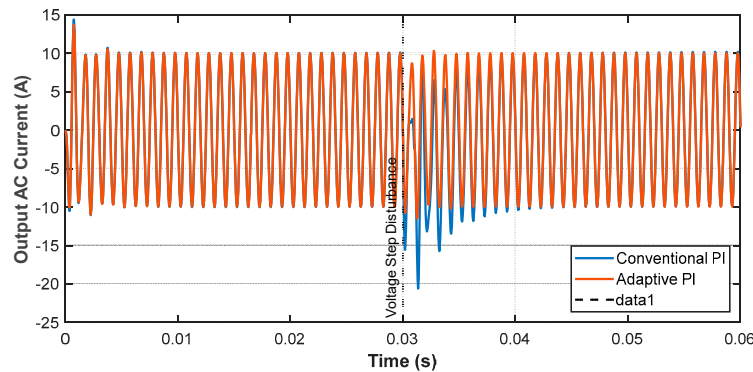


Figure 14: Comparison of the tracking performance of the traditional fixed parameter PI and the adaptive PI in the main DC bus voltage jumping from 60 V to 65 V.

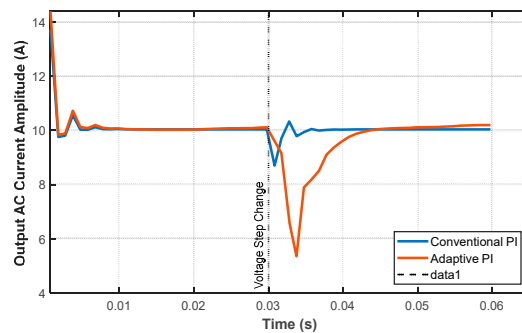


Figure 15: The amplitude characteristics of traditional fixed parameter PI and adaptive PI jump from 60 V to 65 V in the main DC bus voltage.

The two sets of forward and reverse voltage step tests comprehensively confirm that the software-hardware collaborative architecture in this paper has better dynamic stiffness and anti-disturbance robustness than traditional linear controllers when dealing with DC bus disturbances.

3.3 Physical Hardware Platform Construction and Software and Hardware Collaborative Testing

On the basis of simulation verification, in order to further investigate the practical engineering feasibility of the system, a set of excitation power supply hardware prototypes for THDA detection of hydrogen production equipment is developed, and a complete dual power supply parallel test platform is built.

3.3.1 Hardware Platform Composition and Panoramic Test System

The physical platform experimental system is mainly composed of the following core parts:

Digital main control board: It uses ST's STM32H750V8T6 as the main control chip, which is responsible for high-speed ADC sampling, DFT feature extraction, adaptive PI algorithm calculation, and generation of complementary PWM waves with dead zones.

Power inverter main circuit: To ensure thermal stability and operational efficiency under high-frequency chopping, this paper selects a high-performance silicon-based Super Junction Power Field-Effect Transistor (FET) (Model NCE60NF031T) to construct a bidirectional half-bridge topology. This device features a high drain source withstand voltage of 600 V and an ultra-low typical on-resistance of 31 m Ω , and is equipped with an advanced gate driver with optocoupler isolation to ensure reliable operation of high-frequency switches.

The multi-stage matching inductor network shown in Fig. 16 consists of a large-capacity silicon steel sheet core inductor, amorphous nanocrystalline inductor, and a high-frequency hollow coil to meet the switching needs of different frequency bands. To reliably reconstruct the inductor circuit under test conditions, this paper uses a high-current mechanical rocker switch (model: SS11-BBIWQ-RE20-R) as the hardware switching device, ensuring clear and reliable physical link reconstruction.

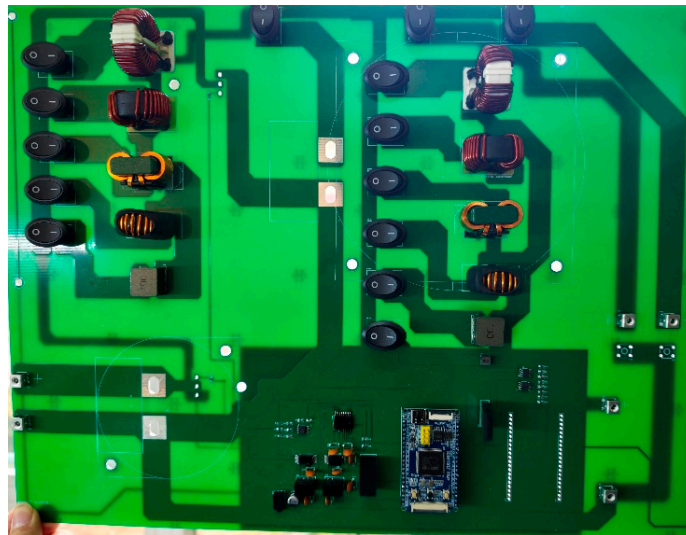


Figure 16: Physical prototype of excitation power supply.

Equivalent load: The hydrogen production equipment is not a simple linear pure resistive load, but a strongly coupled, non-linear complex electrochemical system. For ALK electrolyzers, the classical Randles equivalent circuit model is used as the controlled object model for control system design and steady-state feature extraction. The composition of the model is shown in Fig. 17: The Ohmic internal resistance is the conduction resistance of the electrolyte (such as potassium hydroxide (KOH) solution) and the contact resistance between the plate and the diaphragm. In the high frequency band (>10 kHz), the capacitance effect is short-circuited, and the overall impedance of the electrolyzer is mainly dominated by R_s . The charge transfer resistance R_{ct} is the activated polarization resistance that characterizes the electrochemical reaction on the electrode surface. The double-layer capacitance C_{dl} arises from the porous nature of the electrode materials, which form an electrical double layer at the electrode-electrolyte interface.

As shown in Fig. 18, an ALK electrolyzer (Randles model) is equivalently simulated using a PRD0618 bidirectional programmable DC power supply and configured it in constant voltage/constant resistance (CV/CR) composite load mode.

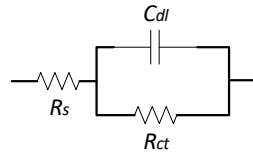


Figure 17: Electrolyzer Randles equivalent circuit model.



Figure 18: PRD0618 bidirectional programmable DC power supply simulates electrolyzer loads.

Monitoring system shown in Fig. 19: Using the Laboratory Virtual Instrument Engineering Workbench (LabVIEW) and high-performance data acquisition terminal, a global data observation link is constructed, which realizes the real-time accurate collection of high-frequency voltage and current signals at parallel nodes, and provides underlying data support for subsequent impedance spectrum analysis.

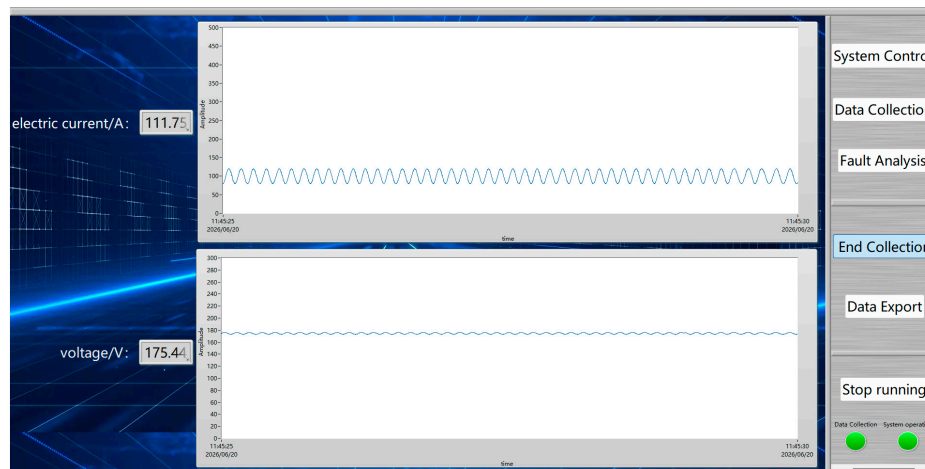


Figure 19: Monitoring system interface is displayed.

3.3.2 Steady-State Waveform and Impedance Decoupling Verification

The waveforms are collected on the dual-power parallel physical platform, and the steady-state waveforms of each frequency point are extracted and THD analysis is completed. The THD characteristic curve of the measured waveform in Fig. 20 shows that:

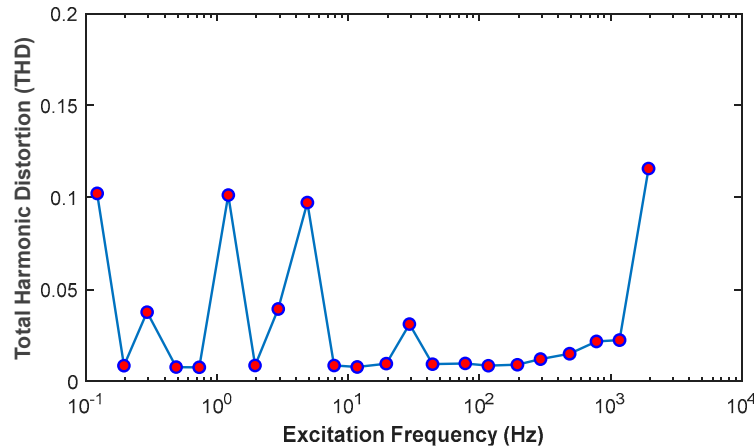


Figure 20: THD characteristics of the measured waveform.

The system perturbation output quality shows obvious frequency band characteristics, and the THD is stable within 2% in the 10 Hz–1 kHz frequency band. This indicates that in this range, the system achieves AC/DC impedance decoupling and high-frequency ripple flattening, ensuring the superposition of AC signals. In the frequency band of 0.1 Hz–10 Hz, THD shows regular fluctuations between 1%–10% due to the low frequency inductance attenuation of the device and the nonlinear accumulation of dead zones. In the >1 kHz frequency band, the THD rises to about 12% due to the discrete delay and dynamic bandwidth boundaries of the system control loop, which limits the ability to follow instructions. The measured data objectively confirm that the proposed software-hardware collaborative architecture has excellent strong impedance decoupling and high-fidelity perturbation injection capabilities in the core detection frequency band of hydrogen production equipment, which verifies the effectiveness and practical applicability of the scheme as a whole.

3.3.3 Core Error Analysis and Engineering Index Evaluation

The excitation current signal acquired by the prototype is compared with the ideal THDA reference signal for in-depth spectral comparison analysis. In the harsh electromagnetic environment where there are non-ideal factors such as stray inductance, switch pipe dead zone effect, and high-frequency temperature drift of the sensor, the prototype can still complete the online convergence of parameters through the adaptive PI algorithm.

To verify the robustness of the system under various operating conditions, the steady-state THD of the full-band injected harmonics was systematically measured under three different large DC baselines of 50 A, 70 A, and 80 A (the results are shown in Figs. 21 and 22). The measured data show that across all tested operating points, the fundamental amplitude steady-state tracking error remains strictly within $\pm 3\%$, while the output THD exhibits frequency-dependent characteristics consistent with the theoretical analysis in Section 3.3.2 (i.e., below 2% in the intermediate band, and rising in the marginal bands due to hardware nonlinearities). The measured error index meets the injection criteria required for offline/online electrochemical impedance spectroscopy (EIS) and THDA diagnosis of high-frequency weak signals in industrial-grade water electrolysis hydrogen production equipment. The test results of the physical hardware platform are consistent with the Simulink simulation data, which confirms the stability, practical feasibility, and architectural baseline value of the multi-level inductive half-bridge topology and steady-state feature adaptive algorithm proposed in this paper.

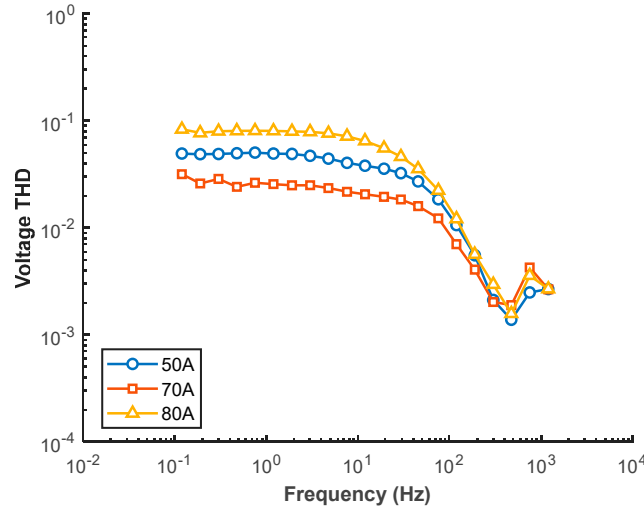


Figure 21: THD data analysis test at different currents.

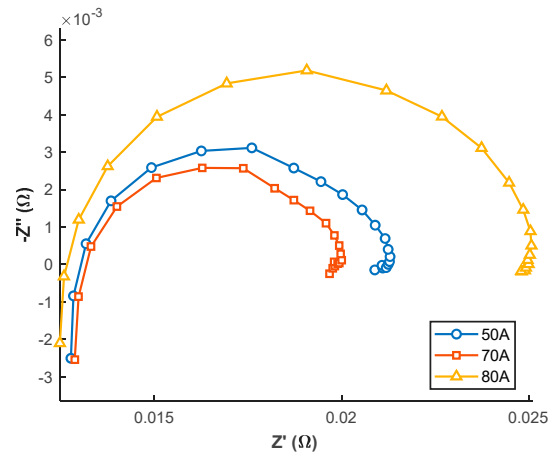


Figure 22: EIS data analysis test under different currents.

3.3.4 Benchmarking and Quantitative Evaluation

To further evaluate the comprehensive performance of the proposed scheme, this section selects two broadband excitation power supply schemes common in the current literature for benchmarking comparison. Scheme 1 is a traditional single-unit large-capacity wideband converter architecture, and Scheme 2 is a dual-power parallel architecture adopting a single passive filter and conventional PI control. The comparative evaluation is conducted around key performance indicators (KPIs) including topology, effective frequency band, dynamic tracking, disturbance recovery, and thermal stress:

Scheme 1 adopts an AC/DC coupled output topology. Since there is no node interference from AC/DC parallel coupling, this architecture possesses inherent stability when facing ± 5 V step disturbances on the DC bus, and exhibits a low amplitude attenuation rate under high-frequency steps from 1 kHz to 10 kHz. However, to achieve high-frequency perturbation injection while outputting a large-capacity DC baseline, the full-power switching devices must withstand high-frequency chopping under heavy currents. This introduces higher switching losses and thermal management pressure. Constrained by thermal stress

bottlenecks, its effective detection band is restricted to 0.1 Hz–10 kHz, which poses severe challenges to its expansion into megawatt-level large-capacity hydrogen production systems.

Scheme 2 significantly reduces main-circuit switching losses and thermal stress through the AC/DC decoupled parallel mechanism, but exposes obvious bandwidth limitations during wideband sweeps. Due to the use of a single passive filter and fixed-parameter PI control, impedance mismatch occurs easily in the high-frequency range, limiting its effective detection band to 0.1 Hz–1 kHz. When the perturbation instruction steps from 1 kHz to 10 kHz, the sharp surge in inductive reactance causes an output amplitude attenuation of up to 45%; dynamic tracking is severely limited, causing the high-frequency (≥ 10 kHz) THD to deteriorate to over 12%. Furthermore, when the main bus suffers a ± 5 V step voltage impact, the lag effect of the fixed-parameter controller leads to a disturbance recovery time exceeding 5 ms, accompanied by obvious transient current distortion.

In contrast, Scheme 3 conducts targeted system-level optimizations based on the dual-power parallel architecture. At the hardware level, the multi-stage inductor switching mechanism strikes a pragmatic balance between low-frequency ripple suppression and high-frequency signal pass-through, extending the effective detection band to 0.1 Hz–100 kHz while keeping the high-frequency THD within 3%. At the algorithmic level, the adaptive PI strategy achieves rapid reconstruction of the waveform amplitude within approximately 2 ms during frequency steps, and effectively introduces active damping when facing ± 5 V DC bus impacts, compressing the disturbance recovery time to within 3 ms. Quantitative data indicate that under the current scaled-down prototype conditions, the proposed scheme achieves a good balance between wideband perturbation injection accuracy and parallel stability while effectively reducing thermal stress. Therefore, it provides a feasible architectural baseline for future exploration of online THDA diagnostics in high-capacity water electrolysis systems.

3.4 Performance Boundaries and Engineering Limitations

Although the above simulations and prototype experiments verify the basic functions of the proposed solution in broadband detection, the objective trend of waveform distortion rate with frequency (as shown in Fig. 20) also reflects the underlying performance boundaries of the architecture. The system's high-fidelity output in the 10 Hz–1 kHz core frequency band, combined with the increased distortion in the >1 kHz high frequency band, is essentially determined by the time-frequency domain coupling characteristics of loop impedance and the nonlinearity of the actual components.

Within the conventional characterization frequency band 10 Hz–1 kHz, the core of the system maintaining injection accuracy lies in time-frequency domain decoupling of AC/DC circuits. At the main circuit end, the series matching inductor utilizes its low-frequency conduction and high-frequency current blocking characteristics to form transient high impedance at the parallel node, effectively clamping the reverse backflow caused by main bus disturbances; On the control side, DFT fundamental extraction approximately converts the originally nonlinear time-varying controlled process into linear optimization of PI gain within the time domain. This combination of loop decoupling and parameter adaptation enables the system to effectively withstand nonlinear backflow shocks under high DC bias.

However, when the injection frequency is further pushed to high frequencies (>1 kHz, up to 100 kHz), the system's THD significantly deteriorates. This high-frequency attenuation is mainly constrained by non-ideal factors under multiphysics coupling: on one hand, the parasitic parallel capacitance effect inside the matching inductor begins to appear at high frequencies, causing the inductor to develop a tendency for self-resonance, leading to high-frequency current blocking and filter performance roll-off; On the other hand, Hall current sensors have inherent phase lag and amplitude attenuation when detecting tiny sine

signals at hundred-kilohertz levels, and common-mode electromagnetic interference generated by the inverter under high-frequency chopping easily couples into the sampling link, interfering with precise extraction of fundamental features. Additionally, to overcome the rapid increase in inductive reactance at ultra-high frequencies in series inductors, the inverter must output a relatively high induced voltage, and the duty cycle easily reaches the limit of the linear modulation region, resulting in slight peak cutting at the output waveform.

When expanding hydrogen production projects with larger capacity, the suitability of this scheme is also constrained by both thermal stress and equivalent load models. On the hardware operation side, the silicon-based superjunction transistor (NCE60NF031T) selected in this paper avoids the static losses of main DC, but dynamic switching losses remain significant under 1 MHz continuous hard switching chopper. Without introducing soft switching topology, thermal design becomes a bottleneck for improving power density. In the test environment, this study validates the Randles equivalent circuit based on programmable DC power simulation. Although this load reproduces the basic ohmic resistance and double-layer capacitance, it cannot realistically simulate the nonlinear polarization noise caused by bubble precipitation (bubble masking effect), electrolyte temperature drift, and plate aging in industrial electrolyzers during operation. Accordingly, it must be explicitly noted that this study primarily validates the wideband excitation signal generation and the AC/DC impedance decoupling behavior under constant baselines. It has not yet proved actual fault diagnosis accuracy, long-term continuous operation, aging detection capability, online integration with a real industrial electrolyzer, or scalability to megawatt-level systems. These unverified dimensions constitute the practical boundaries of the current proof-of-concept and define the roadmap for subsequent field-level research.

4 Conclusions

This paper addresses engineering pain points such as wideband impedance mismatch, cross-band dynamic lag, and strong DC backflow faced by online total harmonic distortion analysis (THDA) for large-scale water electrolysis systems, and proposes and validates a software-hardware collaborative broadband high-dynamic excitation power supply solution. At the hardware level, an improved bidirectional half-bridge topology with series multi-stage matching inductors is constructed, achieving transient impedance decoupling and energy return blocking at AC/DC parallel nodes; At the control level, a dual-layer adaptive PI control strategy based on AC steady-state error feature extraction is proposed. Relying on DFT to extract fundamental features in real time and dynamically adjust gain, it effectively overcomes the control limitations caused by wide-frequency time-varying inductance and nonlinear load disturbances. Fully digital simulation and prototype experiments show that the system has good dynamic recovery capability under 0.1 Hz–100 kHz wideband steady-state scanning, cross-band stepping, and busbar disturbance conditions. In the multi-step DC baseline measurements from 50 A to 80 A, the prototype strictly controlled the fundamental amplitude steady-state tracking error within $\pm 3\%$; The output current THD is below 2% within the 10 Hz–1 kHz core frequency band, and under the edge conditions of 0.1 Hz and >1 kHz, it is constrained by actual hardware, fluctuating at 1%–10% and reached approximately 12%, respectively.

Although this solution has verified basic electrical functions in laboratory benchmark tests, there are still clear technical limitations when applying it to practical engineering applications. First, on the hardware reconfiguration side, the current prototype uses mechanical switches for multi-stage inductor network frequency switching by frequency bands, which means that when performing continuous automatic sweeping across the full frequency band, the system must be stopped in segments for reconfiguration, making seamless fully automated transition impossible. Moreover, hard cutting while under load poses

short-term transient current spike hazards. Secondly, on the algorithm optimization side, the steady-state feature extraction of the outer-loop DFT essentially requires at least one fundamental period window to accumulate data. This inherent mechanism means that when the system handles sub-cycle extreme dynamic disturbances, there is still a time lag that is difficult to completely eliminate.

From the perspective of application maturity, this study currently verifies the generation and impedance decoupling behavior of broadband excitation signals at a maximum of 80 A; Its accuracy in real-world fault diagnosis, long-term continuous operation capability, aging detection performance, feasibility of online integration with real industrial-grade electrolyzers, and scalability to megawatt-scale systems have not yet been proven. Based on these practical boundaries, the research group's future research will focus on three dimensions: first, introducing seamless topological switching based on bidirectional solid-state switches to replace mechanical contacts to achieve smooth sweeping across the entire frequency band; Second, exploring the introduction of advanced algorithms such as Model Predictive Control (MPC) to further reduce the time lag caused by feature extraction; Third, it aims to connect this power architecture to a megawatt-level industrial water electrolysis hydrogen production platform and a real multi-chamber electrolyzer stack, systematically testing its online diagnostic performance under on-site conditions filled with electrochemical noise.

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Ethics Approval: This study did not involve human participants, animal subjects, or any clinical data. Therefore, ethical review and approval were not required for this research.

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