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ARTICLE

A Novel Non-Isolated Cubic DC-DC Converter with High Voltage Gain for Renewable Energy Power Generation System

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ABSTRACT

In recent years, switched inductor (SL) technology, switched capacitor (SC) technology, and switched inductor-capacitor (SL-SC) technology have been widely applied to optimize and improve DC-DC boost converters, which can effectively enhance voltage gain and reduce device stress. To address the issue of low output voltage in current renewable energy power generation systems, this study proposes a novel non-isolated cubic high-gain DC-DC converter based on the traditional quadratic DC-DC boost converter by incorporating a SC and a SL-SC unit. Firstly, the proposed converter's details are elaborated, including its topology structure, operating mode, voltage gain, device stress, and power loss. Subsequently, a comparative analysis is conducted on the voltage gain and device stress between the proposed converter and other high-gain converters. Then, a closed-loop simulation system is constructed to obtain simulation waveforms of various devices and explore the dynamic performance. Finally, an experimental prototype is built, experimental waveforms are obtained, and the experimental dynamic performance and conversion efficiency are analyzed. The theoretical analysis's correctness is verified through simulation and experimental results. The proposed converter has advantages such as high voltage gain, low device stress, high conversion efficiency, simple control, and wide input voltage range, achieving a good balance between voltage gain, device stress, and power loss. The proposed converter is well-suited for renewable energy systems and holds theoretical significance and practical value in renewable energy applications. It provides an effective solution to the issue of low output voltage in renewable energy power generation systems.

KEYWORDS

Cubic DC-DC converter; high voltage gain; low device stress; high efficiency; renewable energy

1 Introduction

The excessive utilization of conventional fossil fuels has been found to contribute significantly to the escalation of carbon emissions, thereby triggering a detrimental impact on the global environment, particularly through the exacerbation of global warming [1]. Moreover, due to the insufficient reserves of these traditional energy sources, the surging consumer demand remains unmet, necessitating the exploration of alternative avenues. Consequently, the pursuit of renewable energy sources has emerged as a paramount strategy to combat environmental pollution and address the ongoing energy crises, captivating the attention of researchers worldwide [2,3]. In order to facilitate the effective utilization of renewable energy, the development and implementation of renewable energy generation systems have become imperative. Nevertheless, the prevailing setback lies in the inability of current renewable energy

generation systems to generate output voltage at levels sufficient to fulfill the requirements of the DC bus outputs [4,5]. This pressing challenge can be effectively surmounted through the application of DC-DC boost converter technology, as illustrated in Fig. 1. By employing the aforementioned DC-DC boost converter, the electricity derived from renewable energy sources can be effectively elevated to meet the voltage requirements of the DC bus, ensuring the smooth transmission of power to the load side. Consequently, the significance and demand for boost converters continue to experience an upward trajectory.

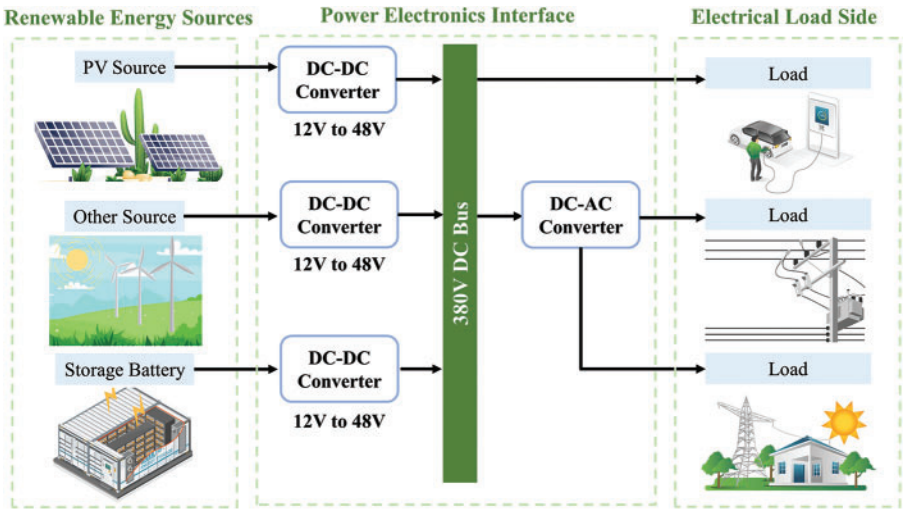

Figure 1: Typical application of DC-DC converter

Among the array of boost converters available, non-isolated DC-DC converters have garnered considerable interest owing to their relatively diminutive size, reduced losses, and cost-effectiveness [6]. With their uncomplicated structure and the ability to amplify voltage by adjusting the duty cycle, traditional non-isolated DC-DC converters have witnessed widespread adoption in industrial production settings [7]. The voltage gain ideally tends toward infinity as the duty cycle approaches unity. However, this amplified voltage gain can precipitate complications such as diode reverse recovery and transient response issues [8–10]. Additionally, the heightened current stress imposed on devices accentuates conduction losses, consequently impeding converter efficiency. Hence, while traditional DC-DC converters boast simplicity and affordability, their limited voltage boost ratio characteristics serve to restrict their range of application scenarios.

To achieve high voltage gain, researchers have conducted extensive investigations on high-gain DC-DC converters [11–14], such as quadratic DC-DC converters [15–17], two-switch DC-DC converters [18] and single-switch DC-DC converters [19–20]. For instance, references [21–23] proposed a cascade structure in the topology that enhances the overall output voltage by connecting two boost converters together in a back-to-back configuration. However, this particular topology necessitates the utilization of numerous components, engendering an enlargement in size, augmented costs, and increased power losses. References [24,25] introduced a quadratic DC-DC converter that exhibited high-voltage boost characteristics. Nonetheless, to attain a voltage gain of 10, this converter necessitates operation at an exceedingly high duty cycle, resulting in heightened device stress, which compromises the efficiency. The converter proposed in reference [26] attains an ultra-high voltage gain of 10 by operating at a duty cycle of 0.5. Alas, the associated topology manifests significant complexity,

with the doubling unit alone comprising one inductor, three capacitors, and two diodes, resulting in a grand total of 18 components. As a consequence, this intricacy incurs elevated costs and power losses. Consequently, an only pursuit of voltage gains in DC-DC converters may inadvertently give rise to adverse implications such as escalated device stress and diminished conversion efficiency. Thus, for DC-DC boost converters, it is crucial to strike a balance among voltage gain, device stress, and power loss.

Switched-capacitor (SC) and switched-inductor (SL) technologies offer solutions to the above limitations. SC and SL possess the advantage of simple structures and low costs. The incorporation of SC and SL technology into a simple DC-DC boost converter holds the potential to optimize performance, enabling higher voltage gains while mitigating voltage stress on components. This approach facilitates the attainment of a harmonious balance between voltage gain, device stress, and power loss [12,20,27–30]. Furthermore, the amalgamation of SC and SL technology, leading to the emergence of switched inductor-capacitor (SL-SC) technology, presents an additional avenue to diminish voltage stress and power loss within DC-DC boost converters, attracting considerable attention in recent years [31–33]. Consequently, this paper proposes a novel cubic high-gain DC-DC boost converter that utilizes the incorporation of a SC unit and a SL-SC unit into the conventional quadratic DC-DC boost converter.

Section 2 provides a detailed description of the proposed converter, including its topology, operating mode, voltage gain, device stress, converter parameter design, and power loss. Section 3 presents an analysis that compares the converter in this paper with other converters. The simulation analysis results are presented in Section 4. Finally, Section 5 presents an experimental prototype that validates the theoretical analysis through experiments.

2 Details of the Proposed Converter

2.1 Configuration of the Proposed Converter

The topology of the proposed converter is illustrated in Fig. 2. This work suggests a novel non-isolated cubic DC-DC converter that incorporates a switched capacitor (SC) unit and a switched inductor-capacitor (SL-SC) unit into the traditional quadratic boost converter, resulting in a cubic boost ratio. SL-SC and SC may require more space due to the larger volume of inductors and capacitors. Additionally, fast charging and discharging in SL-SC and SC necessitate the use of high-speed switching devices, which may result in compromised performance and noise interference in high-frequency applications. Despite the aforementioned disadvantages of the converter, the advantages of the converter are significant, with the main benefits being:

(1) The converter delivers high voltage gain while maintaining low device stress and high conversion efficiency.

(2) The cubic voltage gain of the converter results in an extensive input voltage range.

(3) Utilizing a single switch structure simplifies the control of the converter.

(4) The converter requires fewer components than the high-gain converters presented in references [22] and [26].

(5) The input current remains continuous, with shared ground facilities between the input and load terminals.

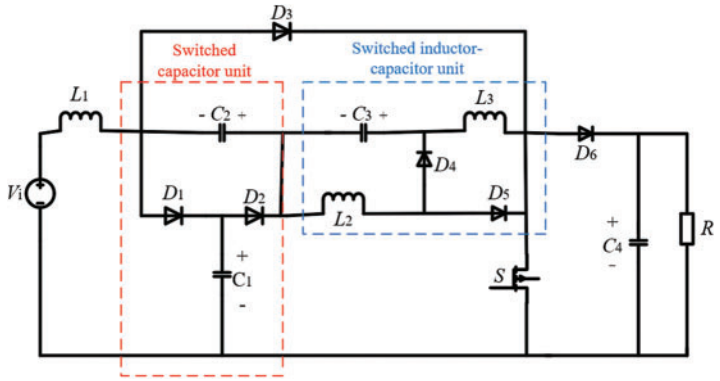

Figure 2: A novel non-isolated cubic DC-DC converter

The converter comprises a switch (S), inductors (L_1–L_3), capacitors (C_1–C_4), diodes (D_1–D_6), and a resistance (R). Fig. 3 illustrates the switching characteristics of the proposed converter. The analysis of the operating principle of the proposed converter in the subsequent sections is based on the hypotheses: (1) the switch and diodes are considered ideal devices, (2) the capacitance is sufficiently large to maintain the capacitance voltage constant for one cycle, and (3) inductors L_1, L_2, and L_3 all function in continuous conduction mode (CCM).

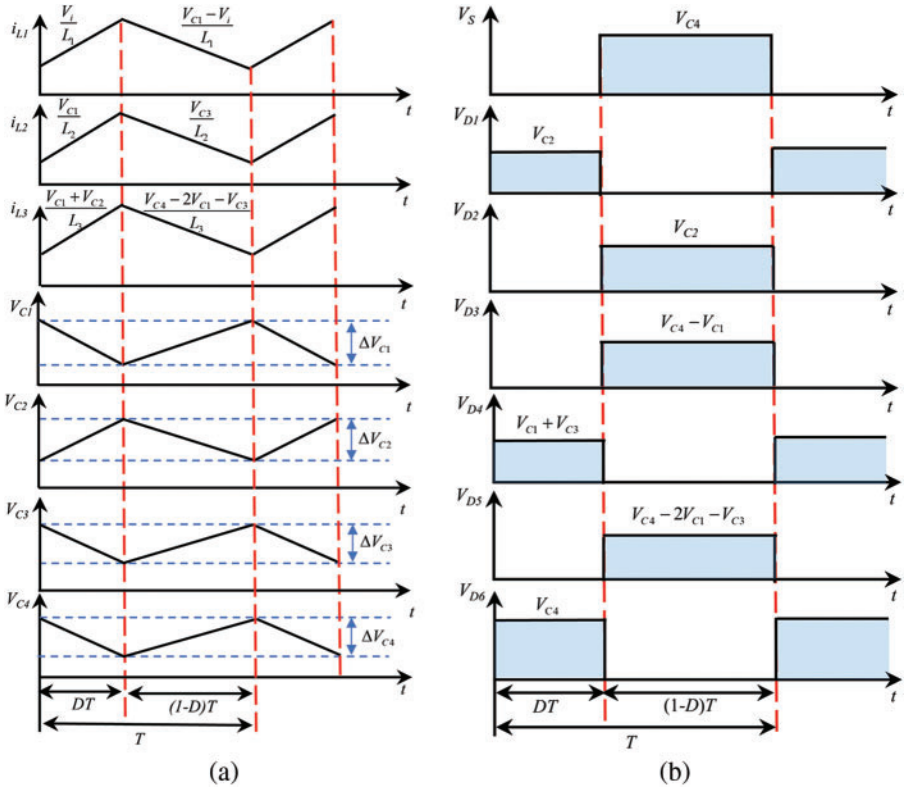

Figure 3: Switching characteristics of the converter: (a) Signals of reactive elements. (b) Signals of semiconductor elements

The converter features only one switch S, resulting in two operating modes within a single switching cycle T_S, namely, conduction and off mode. Figs. 4 and 5 show the equivalent circuits of the two modes, with D representing the converter duty cycle. Detailed elaboration on the working principles of these modes will be provided in the subsequent sections.

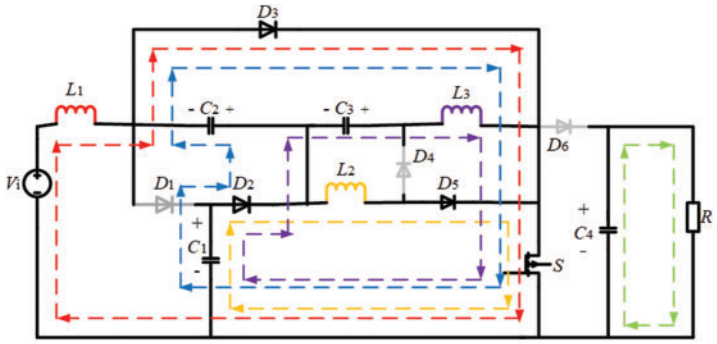

Figure 4: Switch tube conduction mode of the proposed converter, $0 < t \leq DT_S$

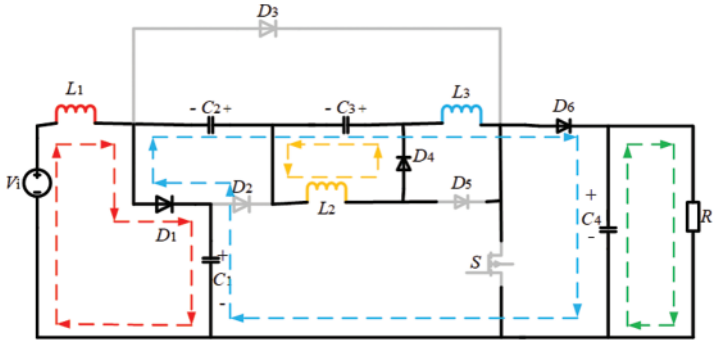

Figure 5: Switch tube off mode of the proposed converter, $DT_S < t \leq T_S$

2.2 Switch Tube Conduction Mode

In the present mode (Fig. 4), the switch tube S is turned on, causing diodes D_1, D_4, and D_6 to turn off by reverse voltage drop, while diodes D_2, D_3, and D_5 turn on by forward voltage drop. The input voltage V_i transfers energy to the inductor L_1; Capacitor C_1 charges capacitor C_2; The capacitor C_1 charges the energy storage inductor L_2; The capacitors C_1 and C_3 are connected in series to convey power to L_3; The resistance R is powered by the capacitor C_4. The waveform of inductive current i_{L1}, i_{L2}, and i_{L3} shows a linear upward trend. This process encompasses the following:

$$\begin{cases} L_1 \dfrac{di_{L1}}{dt} = V_i, L_2 \dfrac{di_{L2}}{dt} = V_{C1} = V_{C2}, L_3 \dfrac{di_{L3}}{dt} = V_{C1} + V_{C3} \\ C_1 \dfrac{dV_{C1}}{dt} = -I_{L2} - I_{C2} - I_{L3}, C_2 \dfrac{dV_{C2}}{dt} = I_{C2}, C_3 \dfrac{dV_{C3}}{dt} = -I_{L3}, C_4 \dfrac{dV_{C1}}{dt} = -I_o \end{cases} \tag{1}$$

2.3 Switch Tube off Mode

In switch tube off mode (Fig. 5), the switch tube S is turned off, D_2, D_3, and D_5 are deactivated by withstanding a reverse voltage drop, and D_1, D_4, D_6 are conducted by withstanding a forward voltage drop. The input voltage V_i and the input inductor L_1 charge the capacitor C_1; V_i, L_1, C_2, C_3, L_3 charge

C_4; L_2 charges C_3; The resistance R is powered by C_4. The waveform of inductive current i_{L1}, i_{L2}, and i_{L3} shows a linear downward trend. This process includes:

$$\begin{cases} L_1\dfrac{di_{L1}}{dt} = V_{C1} - V_i; L_2\dfrac{di_{L2}}{dt} = V_{C3}; L_3\dfrac{di_{L3}}{dt} = V_o - 2V_{C1} - V_{C3} \\ C_1\dfrac{dV_{C1}}{dt} = I_{C2} + I_{L1}; C_2\dfrac{dV_{C2}}{dt} = -I_{L3}; C_3\dfrac{dV_{C3}}{dt} = I_{L2} - I_{L3}; C_4\dfrac{dV_{C1}}{dt} = I_{L3} - I_o \end{cases} \tag{2}$$

2.4 Voltage Gain Equation

Based on the volt-second balance principle on the inductors within a single switching period T_S, we can deduce that:

$$\begin{cases} DV_i = (1-D)(V_{C1} - V_i) \\ DV_{C1} = (1-D)V_{C3} \\ D(V_{C1} + V_{C3}) = (1-D)(V_o - 2V_{C1} - V_{C3}) \end{cases} \tag{3}$$

The voltage stress equations for capacitors $C_1 \sim C_4$ can be obtained from Eq. (3):

$$\begin{cases} V_{C1} = \dfrac{1}{1-D}V_i \\ V_{C2} = \dfrac{1}{1-D}V_i \\ V_{C3} = \dfrac{D}{(1-D)^2}V_i \\ V_{C4} = V_o = \dfrac{1+(1-D)^2}{(1-D)^3}V_i \end{cases} \tag{4}$$

The mathematical expression for the voltage gain of the converter can be derived by using Eqs. (3)~(4):

$$M = \frac{V_o}{V_i} = \frac{1+(1-D)^2}{(1-D)^3} \tag{5}$$

where V_i, V_o, M, and D are the input voltage, output voltage, voltage gain, and duty cycle of the converter, respectively. Therefore, the final output voltage of the proposed converter can be calculated using the subsequent expression:

$$V_o = \frac{1+(1-D)^2}{(1-D)^3}V_i \tag{6}$$

2.5 Calculation of Voltage Stress and Current Stress

In the conduction mode, the diodes D_1, D_4, and D_6 are turned off; In the off mode, the diodes D_2, D_3, and D_5 are turned off. The voltage across the switch tube S equals the voltage across the capacitor C_4. The following formula is the voltage stress expression for switch tube S and diodes $D_1 \sim D_6$:

$$\begin{cases} V_S = V_{C4} = V_o = \dfrac{1+(1-D)^2}{(1-D)^3}V_i \\ V_{D1} = V_{C1} = \dfrac{1}{1-D}V_i; V_{D2} = \dfrac{1}{1-D}V_i; V_{D3} = \dfrac{1}{(1-D)^3}V_i \\ V_{D4} = \dfrac{1}{(1-D)^2}V_i; V_{D5} = \dfrac{D}{(1-D)^3}V_i; V_{D6} = V_{C4} = \dfrac{1+(1-D)^2}{(1-D)^3}V_i \end{cases} \tag{7}$$

According to the ampere-second balance principle on the capacitors, the current stress expressions for $D_1 \sim D_6$ can be obtained:

$$\begin{cases} I_{D1} = \dfrac{1}{(1-D)^2} I_o; I_{D2} = \dfrac{1}{D(1-D)^2} I_o \\ I_{D3} = \left(\dfrac{1+(1+D)^2}{(1-D)^3} + \dfrac{1}{D} \right) I_o \\ I_{D4} = \dfrac{1}{1-D} I_o; I_{D5} = \dfrac{D}{(1-D)^2} I_o; I_{D6} = I_o \end{cases} \tag{8}$$

The capacitive current stress can be obtained under the switch tube conduction and off mode:

$$\begin{cases} i_{C1} = \begin{cases} \dfrac{I_o}{D(1-D)^2} & 0 \le t < DT_s \\ \dfrac{I_o}{(1-D)^2} & DT_s \le t < T_s \end{cases}; i_{C2} = \begin{cases} \dfrac{I_o}{D} & 0 \le t < DT_s \\ \dfrac{-I_o}{1-D} & DT_s \le t < T_s \end{cases} \\ i_{C3} = \begin{cases} \dfrac{-I_o}{1-D} & 0 \le t < DT_s \\ \dfrac{DI_o}{(1-D)^2} & DT_s \le t < T_s \end{cases}; i_{C4} = \begin{cases} -I_o & 0 \le t < DT_s \\ \dfrac{DI_o}{1-D} & DT_s \le t < T_s \end{cases} \end{cases} \tag{9}$$

The mean current passing through the switch during the conduction mode is:

$$I_{ds} = \frac{1-D(1-D)^2}{(1-D)^3} I_o \tag{10}$$

2.6 Converter Parameter Design

Under lossless conditions, the input power and output power of the converter should be equivalent, so it can be expressed as:

$$\begin{cases} P_i = P_0 \\ \dfrac{I_i}{I_0} = \dfrac{V_0}{V_i} = M = \dfrac{1+(1-D)^2}{(1-D)^3} \\ I_i = I_{L1} = \dfrac{\left(1+(1-D)^2\right)}{(1-D)^3} I_o \\ I_{L1} = \dfrac{\left(1+(1-D)^2\right)^2 V_i}{(1-D)^6 R} \end{cases} \tag{11}$$

According to the ampere-second balance principle on C_3 and C_4, and combining Eqs. (1)~(2), it can be obtained that:

$$\begin{cases} D(-I_{L3}) + (1-D)(I_{L2} - I_{L3}) = 0 \\ D(-I_o) + (1-D)(I_{L3} - I_o) = 0 \end{cases} \tag{12}$$

The expressions of $I_{L1}\sim I_{L3}$ can be obtained from Eqs. (11)∼(12):

$$\begin{cases} I_{L1}=\dfrac{\left(1+(1-D)^2\right)}{(1-D)^3}I_o=\dfrac{\left(1+(1-D)^2\right)^2V_i}{(1-D)^6R} \\ I_{L2}=\dfrac{1}{(1-D)^2}I_o=\dfrac{\left(1+(1-D)^2\right)V_i}{(1-D)^5R} \\ I_{L3}=\dfrac{1}{1-D}I_o=\dfrac{\left(1+(1-D)^2\right)V_i}{(1-D)^4R} \end{cases} \tag{13}$$

After turning on the switch tube, the voltages of the inductors $L_1\sim L_3$ can be obtained from Eq. (1), and we can derive the formula for the inductor current ripple as follows:

$$\begin{cases} L_1\dfrac{di_{L1}}{dt}=V_i\Rightarrow\dfrac{\Delta i_{L1}}{DT_s}=\dfrac{V_i}{L_1}\Rightarrow\Delta i_{L1}=\dfrac{V_iDT_s}{L_1} \\ L_2\dfrac{di_{L2}}{dt}=\dfrac{1}{1-D}V_i\Rightarrow\dfrac{\Delta i_{L2}}{DT_s}=\dfrac{V_i}{(1-D)L_2}\Rightarrow\Delta i_{L2}=\dfrac{V_iDT_s}{(1-D)L_2} \\ L_3\dfrac{di_{L3}}{dt}=\dfrac{1}{(1-D)^2}V_i\Rightarrow\dfrac{\Delta i_{L3}}{DT_s}=\dfrac{V_i}{(1-D)^2L_3}\Rightarrow\Delta i_{L3}=\dfrac{V_iDT_s}{(1-D)^2L_3} \end{cases} \tag{14}$$

According to the boundary conditions when the inductive current operates at CCM:

$$I_{L\min}=I_L-\frac{1}{2}\Delta i_L\geq 0 \tag{15}$$

By substituting Eqs. (13)∼(14) into Eq. (15), the subsequent expression can be derived:

$$\begin{cases} \dfrac{\left(1+(1-D)^2\right)^2V_i}{(1-D)^6R}-\dfrac{V_iDT_s}{2L_1}\geq 0\Rightarrow L_1\geq\dfrac{(1-D)^6DR}{2\left(1+(1-D)^2\right)^2f_s} \\ \dfrac{\left(1+(1-D)^2\right)V_i}{(1-D)^5R}-\dfrac{V_iDT_s}{2(1-D)L_2}\geq 0\Rightarrow L_2\geq\dfrac{(1-D)^4DR}{2\left(1+(1-D)^2\right)f_s} \\ \dfrac{\left(1+(1-D)^2\right)V_i}{(1-D)^4R}-\dfrac{V_iDT_s}{2(1-D)^2L_3}\geq 0\Rightarrow L_3\geq\dfrac{(1-D)^2DR}{2\left(1+(1-D)^2\right)f_s} \end{cases} \tag{16}$$

After activating the switch tube S, the current of the capacitors C_1 to C_4 can be obtained from Eq. (9), and the expression of the capacitor voltage ripple is obtained as follows:

$$\begin{cases} \left|C_1\dfrac{dV_{C1}}{dt}\right|=\left|\dfrac{I_o}{D(1-D)^2}\right|\Rightarrow\left|\dfrac{\Delta V_{C1}}{DT_s}\right|=\left|\dfrac{I_o}{D(1-D)^2C_1}\right|\Rightarrow\Delta V_{C1}=\dfrac{\left(1+(1-D)^2\right)V_iT_s}{C_1(1-D)^5R} \\ \left|C_2\dfrac{dV_{C2}}{dt}\right|=\left|\dfrac{I_o}{D}\right|\Rightarrow\left|\dfrac{\Delta V_{C2}}{DT_s}\right|=\left|\dfrac{I_o}{DC_2}\right|\Rightarrow\Delta V_{C2}=\dfrac{\left(1+(1-D)^2\right)V_iT_s}{C_2(1-D)^3R} \\ \left|C_3\dfrac{dV_{C3}}{dt}\right|=\left|\dfrac{-I_o}{1-D}\right|\Rightarrow\left|\dfrac{\Delta V_{C3}}{DT_s}\right|=\left|\dfrac{-I_o}{(1-D)C_3}\right|\Rightarrow\Delta V_{C3}=\dfrac{\left(1+(1-D)^2\right)V_iDT_s}{C_3(1-D)^4R} \\ \left|C_4\dfrac{dV_{C4}}{dt}\right|=|-I_o|\Rightarrow\left|\dfrac{\Delta V_{C4}}{DT_s}\right|=\dfrac{|-I_o|}{C_4}\Rightarrow\Delta V_{C4}=\dfrac{\left(1+(1-D)^2\right)V_iDT_s}{C_4(1-D)^3R} \end{cases} \tag{17}$$

If the capacitance voltage ripple value does not exceed 1% of the average capacitance voltage, there are:

$$\begin{cases} \Delta V_{C1} \le \dfrac{1}{100} V_{C1} \Rightarrow \Delta V_{C1} \le \dfrac{1}{100} \times \dfrac{1}{1-D} V_{\mathrm{i}} \Rightarrow C_1 \ge 100 \times \dfrac{\left(1+(1-D)^2\right)}{R(1-D)^4 f_s} \\ \Delta V_{C2} \le \dfrac{1}{100} V_{C2} \Rightarrow \Delta V_{C2} \le \dfrac{1}{100} \times \dfrac{1}{1-D} V_{\mathrm{i}} \Rightarrow C_2 \ge 100 \times \dfrac{\left(1+(1-D)^2\right)}{R(1-D)^2 f_s} \\ \Delta V_{C3} \le \dfrac{1}{100} V_{C3} \Rightarrow \Delta V_{C3} \le \dfrac{1}{100} \times \dfrac{D}{(1-D)^2} V_{\mathrm{i}} \Rightarrow C_3 \ge 100 \times \dfrac{\left(1+(1-D)^2\right)}{R(1-D)^2 f_s} \\ \Delta V_{C4} \le \dfrac{1}{100} V_{C4} \Rightarrow \Delta V_{C4} \le \dfrac{1}{100} \times \dfrac{\left(1+(1-D)^2\right)}{(1-D)^3} V_{\mathrm{i}} \Rightarrow C_4 \ge 100 \times \dfrac{D}{R f_s} \end{cases} \tag{18}$$

2.7 Power Loss Analysis

The converter's power loss is composed of four primary components: capacitance loss, switch loss, diode loss, and inductance loss. Fig. 6 displays the equivalent circuit of the proposed converter, incorporating parasitic parameters, to investigate its power consumption. r_{s1} represents the parasitic resistance of the power switch, and t_{on} and t_{off} represent the conduction and off delay times of the switch, respectively. $V_{F1}\sim V_{F6}$ are the forward conduction voltage drops of diodes $D_1\sim D_6$, individually. $r_{D1}\sim r_{D6}$ are the forward conduction resistances of diodes $D_1\sim D_6$. $r_{C1}\sim r_{C4}$ represent the series parasitic resistance of capacitors $C_1\sim C_4$, respectively. $r_{L1}\sim r_{L3}$ represent the series parasitic resistance of inductors $L_1\sim L_3$, correspondingly.

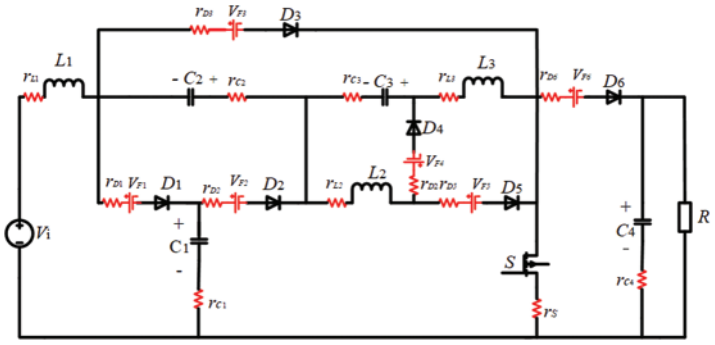

Figure 6: Equivalent circuit of the converter considering parasitic parameters

When S is activated, the power loss produced by it is primarily categorized into conduction and switching losses. The total loss of the switch tube can be calculated using Eq. (19). Where V_{ds} and I_d are the average voltage and average current of the switch tube, I_{S_rms} represents the effective value of the switch current.

$$P_{S\_total} = P_{S\_conduction} + P_{S\_switching} = (I_{S\_rms})^2 r_s + \frac{1}{T_s}\left(\int_0^{t_{on}} V_{ds\_avg} I_{ds\_avg} dt + \int_0^{t_{off}} V_{ds} i_{ds} dt\right) \tag{19}$$

The power loss in diodes primarily results from forward conduction resistance and forward conduction voltage drop. The power loss of the diode can be calculated by Eq. (20). Where $I_{\mathrm{D\_rms}}$ represents the effective value of diode current, $I_{\mathrm{D\_avg}}$ represents the average value of diode current.

$$P_{D\_total} = P_{D\_r_D} + P_{D\_V_F} = \sum_{n=1}^{6} \left(I_{Dn\_rms}^2 r_{Dn}\right) + \sum_{n=1}^{6} \left(I_{Dn\_avg} V_{Fn}\right) \tag{20}$$

The inductance loss and capacitance loss are mainly generated by their respective series parasitic resistors. The calculation formula is shown as Eq. (21). Where $I_{\mathrm{L\_rms}}$ and $I_{\mathrm{C\_rms}}$ represent the effective value of the inductive current and the effective value of the capacitive current, respectively.

$$\begin{cases} P_{L\_total} = \sum_{n=1}^{3} I_{Ln\_rms}^2 r_{\mathrm{L}n} \\ P_{C\_total} = \sum_{n=1}^{4} I_{Cn\_rms}^2 r_{Cn} \end{cases} \tag{21}$$

The total power loss of the converter is:

$$P_{Loss} = P_{S\_total} + P_{D\_total} + P_{C\_total} + P_{L\_total} \tag{22}$$

The conversion efficiency of the converter can be obtained from Eq. (23), where P_{o} represents the output power.

$$\eta = \frac{P_0}{P_0 + P_{Loss}} \times 100\% \tag{23}$$

3 Comparison with Other Converters

The present study compares the voltage gain, switch voltage stress, and switch quantity of the proposed converter with other high-gain converters, as outlined in Table 1. For equitable comparison, this study selects the capacitor and the diode with the lowest stress values from each converter. The minimum voltage stress of the capacitor and diode for various converters is also presented in Table 1.

Table 1: Comparison of converters

Type	Voltage gain ($V_{\mathrm{o}}/V_{\mathrm{i}}$)	Switch tube voltage stress ($V_{\mathrm{S}}/V_{\mathrm{i}}$)	Diode voltage stress ($V_{\mathrm{D}}/V_{\mathrm{i}}$)	Capacitor voltage stress ($V_{\mathrm{C}}/V_{\mathrm{i}}$)	Switch tube number
Traditional quadratic boost converter	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1
Traditional cubic boost converter	$\frac{1}{(1-D)^3}$	$\frac{1}{(1-D)^3}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1
Reference [13]	$\frac{D^3-3D^2+3D}{(1-D)^3}$	$\frac{1}{(1-D)^3}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1

(Continued)

Table 1 (continued)

Type	Voltage gain (V_o/V_i)	Switch tube voltage stress (V_S/V_i)	Diode voltage stress (V_D/V_i)	Capacitor voltage stress (V_C/V_i)	Switch tube number
Reference [14]	$\frac{1}{(1-D)^3}$	$\frac{1}{(1-D)^2}$	$\frac{1}{1-D}$	$\frac{D}{1-D}$	1
Reference [15]	$\frac{D^2}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	$\frac{D}{(1-D)^2}$	1
Reference [16]	$\frac{D(2-D)}{(1-D)^2}$	$\frac{1}{(1-D)^2}$	$\frac{D}{1-D}$	$\frac{D}{(1-D)^2}$	1
Reference [17]	$\frac{1+3D}{1-D}$	S_1: $\frac{1+D}{1-D}$ S_2: $\frac{2D}{1-D}$	$\frac{1+3D}{1-D}$	$\frac{D}{1-D}$	2
Reference [20]	$\frac{2+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	1
Reference [27]	$\frac{3+D}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	$\frac{1}{1-D}$	4
The proposed converter	$\frac{1+(1-D)^2}{(1-D)^3}$	$\frac{1+(1-D)^2}{(1-D)^3}$	$\frac{D}{(1-D)^2}$	$\frac{1}{1-D}$	1

The findings indicate that the proposed converter offers decreased switch tube quantity and simpler control when compared to the references [17] and [27]. While the number of switching tubes in other references aligns with that in this study, there are variations in voltage gain and device stress. To provide a visual comparison, Figs. 7a∼7d display the curve of voltage gain *vs*. duty ratio D (D = 0.2 to 0.7), the curve of diode stress *vs*. voltage gain, the curve of capacitor stress *vs*. voltage gain, and the curve of switch stress *vs*. voltage gain, respectively. Under the same duty ratio, the proposed converter has a larger gain value compared to converters [13–17,20,27], conventional quadratic boost converter and conventional cubic boost converter, as depicted in Fig. 7a. At a duty cycle of 0.4, the proposed converter achieves a voltage gain of 6.3, which is 1.73, 1.34, 3.57, 1.71, 1.56 and 1.17 times the voltage gain in references [13,14,16,17,20] and [27], respectively, and even 15.36 times the voltage gain in reference [15], reflecting the high gain advantage of the proposed converter. Furthermore, Figs. 7b and 7c suggest that the proposed converter provides the advantage of low voltage stress for the capacitor and diode. As depicted in Fig. 7d, the voltage stress on the power switch of the proposed converter is less than that in references [13,15–16], and is flush with traditional quadratic and traditional cubic boost converters. While the switch voltage stress in converters [14,17,20] and [27] is lower, these converters require higher duty ratios to obtain the desired voltage boost ratio. This can lead to transient response issues [19]. Additionally, the capacitor and diode stress in these converters is higher. Therefore, overall, when compared to other converters, the proposed converter offers significant advantages in terms of both device stress and voltage gain.

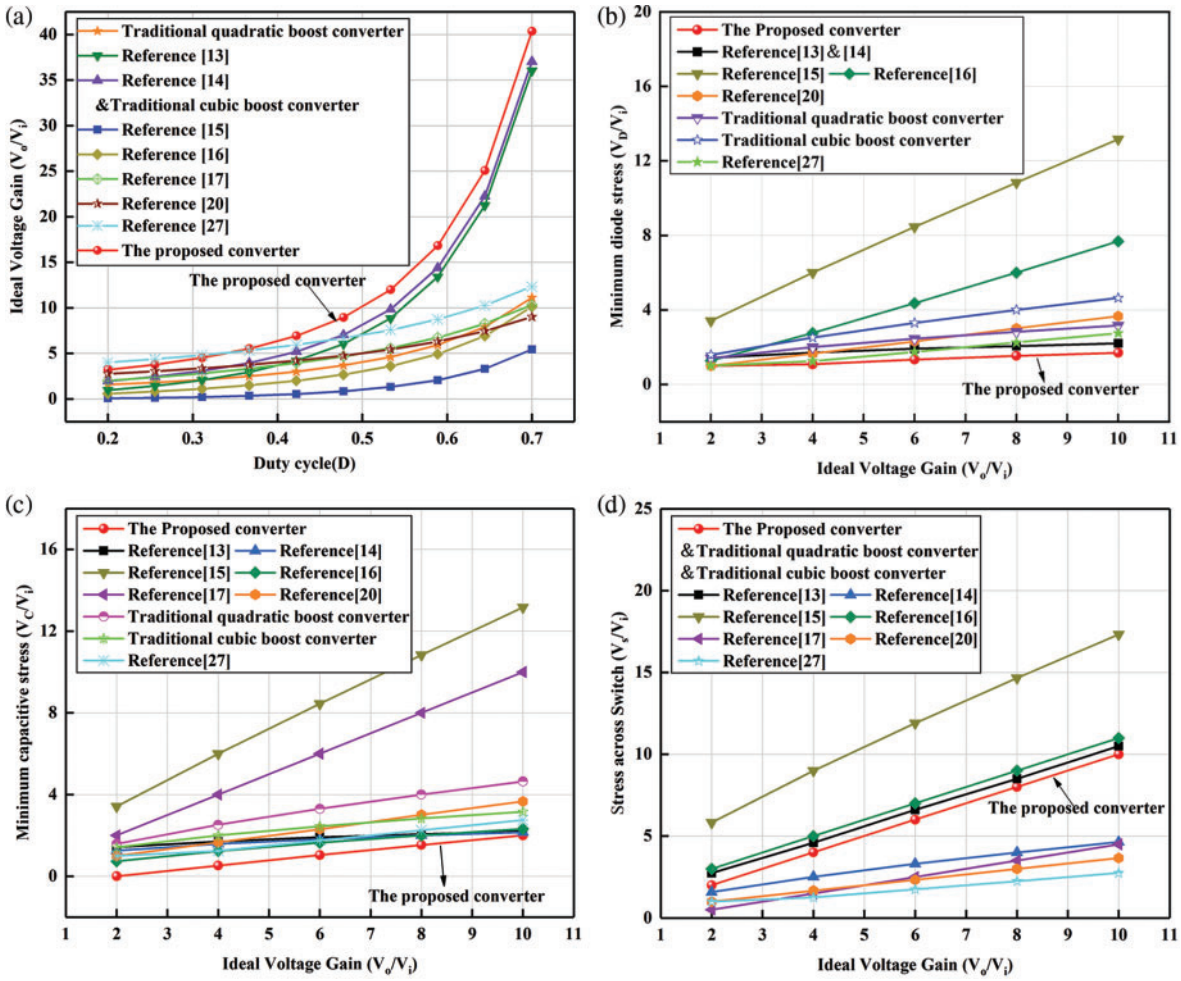

Figure 7: Comparison of converters: (a) voltage gain *vs*. duty ratio, (b) diode stress *vs*. voltage gain, (c) capacitor stress *vs*. voltage gain, (d) switch stress *vs*. voltage gain

4 Simulation Analysis

Table 2 lists the main circuit parameters for closed-loop simulation. The selection of inductor values L_1, L_2, and L_3 considers the minimum inductance requirement specified in Eq. (16), while retaining a certain margin and taking into account cost and performance. Similarly, capacitor parameters C_1, C_2, C_3, and C_4 are chosen to meet the minimum capacitance value requirement stated in Eq. (18), while also retaining a certain margin and considering cost and performance.

Table 2: Circuit parameter settings

Parameters	Values
Input voltage	12 V
Switching frequency	50 kHZ

(Continued)

Table 2 (continued)

Parameters	Values
Output resistor	100 Ω
Duty cycle	0.4
L_1, L_2, L_3	150, 330, 330 μH
C_1, C_2, C_3, C_4	220, 220, 330, 330 μF

The simulation waveforms of different devices with a duty ratio of 0.4 are presented in Fig. 8. Figs. 8a∼8c indicate that the average currents of inductors L_1, L_2, and L_3 are 4.71, 1.98, and 1.25 A, respectively, which are consistent with the results obtained from Eq. (13). Fig. 8a shows that the input current (equal to inductance L_1 current) is essentially continuous, which is crucial for the application of new energy [20]. Additionally, the average output current is around 0.75 A, as shown in Fig. 8d, which confirms the theoretical analysis results. The capacitor voltage waveform is shown in Figs. 8e∼8h, the average voltages of capacitors C_1, C_2, C_3, and C_4 are approximately 20, 20, 13.3, and 75.5 V, respectively, consistent with the theoretical analysis results obtained in Eq. (4). Figs. 8i∼8p display the semiconductor voltage and output voltage waveforms. For the proposed converter, the load voltage is equal to the output voltage. According to Fig. 8j, the output voltage (load voltage) is around 75.5 V, which is achieved with an input voltage of 12 V. The voltage gain is 6.3. The simulation results verify the high-gain advantage of the proposed converter. Moreover, the voltage of the switch tube is about 75.5 V, as shown in Fig. 8i. The voltages of diodes D_1, D_2, D_3, D_4, D_5, and D_6 in Figs. 8k∼8p are approximately 20, 20, 55.5, 33.3, 22.25, and 75.5 V, respectively, consistent with the theoretical calculation results in Eq. (7).

In summary, the simulation analysis results confirm the validity of the theoretical analysis and demonstrate the excellent boost and device stress characteristics of the suggested converter.

The proposed converter employs the UC3842AN chip and peak current control (PCM) as its control strategy. Under this control strategy, dynamic simulation waveforms of the output voltage when input voltage jumps (Fig. 9a) are obtained, as shown in Fig. 9b. Additionally, dynamic simulation waveforms of the converter's output voltage and output current during the transition from half to full load are acquired, as depicted in Figs. 9c and 9d, respectively. As demonstrated in Fig. 9b, when the input voltage changes in steps between 10 and 16 V, the output voltage undergoes dynamic responses. The overshoot of the output voltage is small, less than 0.8 V in both cases, and the adjustment time is short, less than 15 ms in both cases. Observations from Figs. 9c and 9d reveal that when output power jumps from half load, 28.5 W, to full load, 57 W, the output voltage experiences a small overshoot, approximately 1 V, while the adjustment time is approximately 16 ms. Subsequently, the output voltage stabilizes at around 75.5 V, and the output current stabilizes at around 0.75 A. These dynamic simulation results suggest that the proposed converter exhibits excellent dynamic performance.

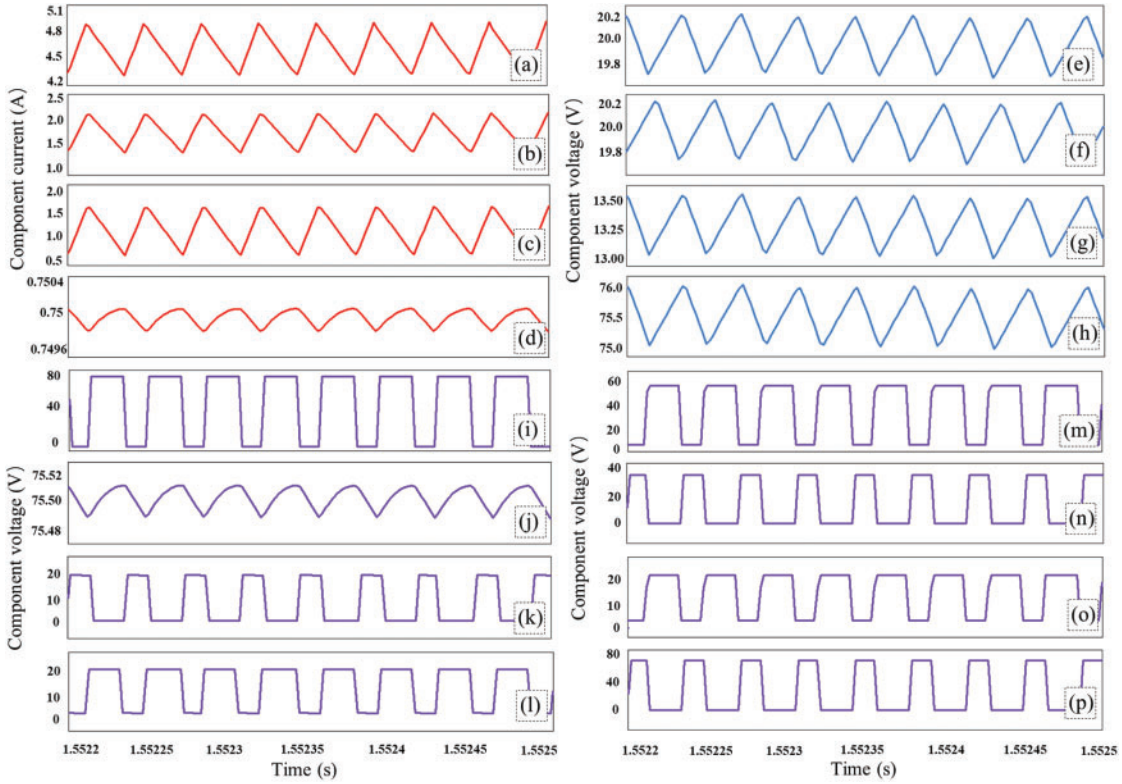

Figure 8: Simulation results: (a) current through the L_1, (b) current through the L_2, (c) current through the L_3, (d) ouput current I_o, (e) voltage across the C_1, (f) voltage across the C_2, (g) voltage across the C_3, (h) voltage across the C_4, (i) voltage across the S, (j) output voltage V_o (i.e., load voltage V_R), (k) voltage of the D_1, (l) voltage of the D_2, (m) voltage of the D_3, (n) voltage of the D_4, (o) voltage of the D_5, (p) voltage of the D_6

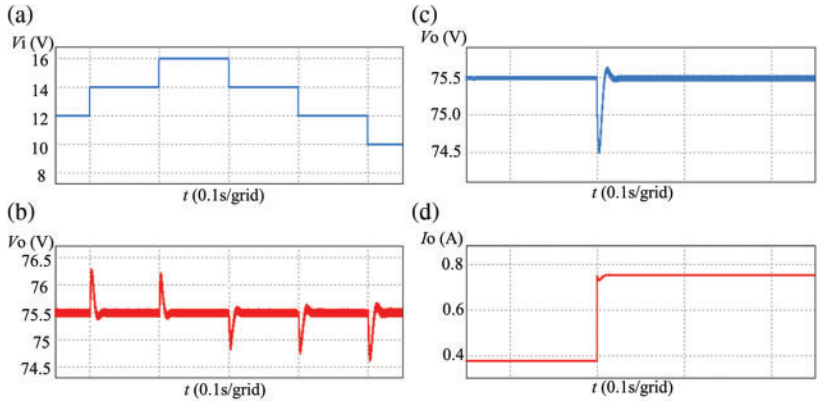

Figure 9: The dynamic simulation waveforms: (a) input voltage with a step change; (b) output voltage dynamic response; (c) output voltage in the transition from 28.5 to 57 W; (d) output current in the transition from 28.5 to 57 W

5 Experimental Analysis

To further verify the accuracy and validity of the theoretical model, this study constructs an experimental prototype for testing. The prototype operates on an input voltage of 12 V, produces an output voltage of 75.5 V, and has a full load power of 57 W. Table 3 presents the key parameters of the experimental prototype. The values of capacitors and inductors in the experiment are consistent with the simulation, while also meeting the requirements of Eqs. (16) and (18), retaining a certain margin and considering performance and cost comprehensively. Then, device models are selected based on the values of capacitors and inductors. Fig. 10 showcases the physical appearance of the experimental prototype. Fig. 11 illustrates the experimental waveforms of the switch driving voltage V_{GS}, power switch voltage V_S, output voltage V_o (i.e., load voltage V_R), capacitor C_1 voltage V_{C1}, diode D_1 voltage V_{D1}, diode D_4 voltage V_{D4}, inductor L_1 current I_{L1}, and output current I_o at a duty cycle of 0.4.

Table 3: The key parameters of the experimental prototype

Parameter	Numerical value	Model
Input voltage V_i	12 V	/
Output voltage V_o	75.5 V	/
Output power P_o	57 W	/
Load R	100 Ω	RXLG200-0.1-100
switching frequency f_s	50 kHZ	/
Capacitor C_1, C_2	220, 220 μF	EKXJ451ELL101MMP1S
Capacitor C_3, C_4	330, 330 μF	SM2271EME092RB
Inductor L_1 , L_2, L_3	150, 330, 330 μH	SLT050125T470MUB
Diode D_1, D_2, D_3, D_4, D_5, D_6	/	C3D10060A
Power switch S	/	SCT3060ALGC11
Control chip	/	UC3842AN
Optocoupler isolation driver chip	/	ACPL-W346-500E

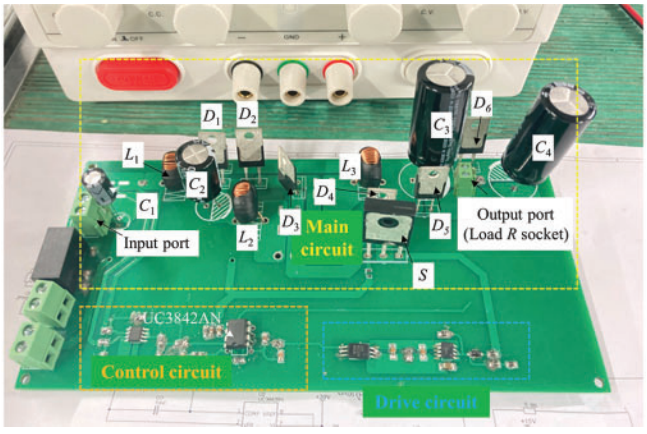

Figure 10: The physical appearance of the experimental prototype

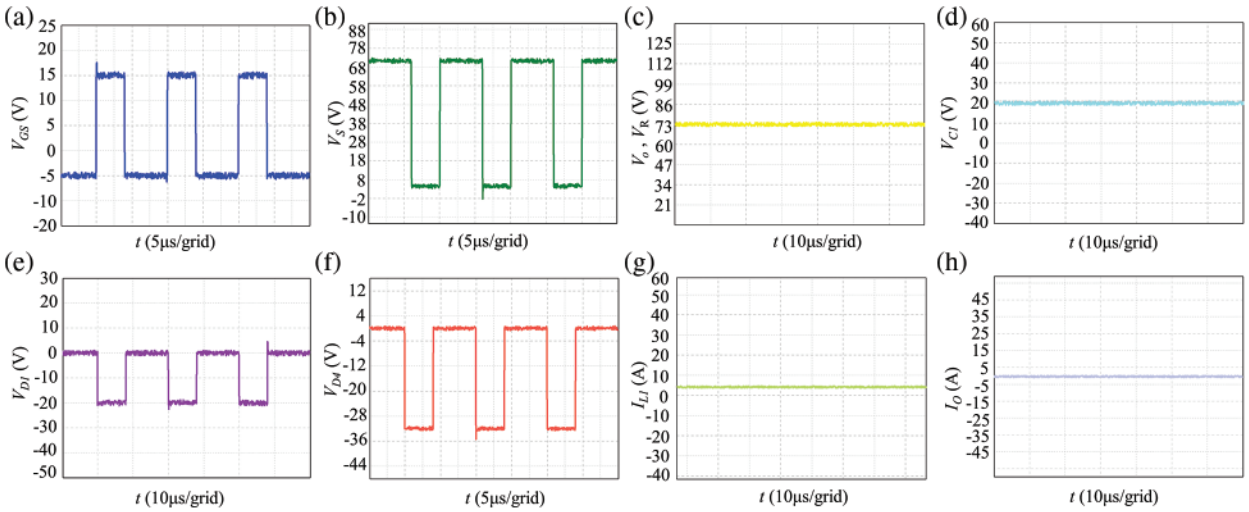

Figure 11: Experimental waveforms: (a) switching tube drive voltage V_{GS}, (b) switching tube voltage V_S, (c) output voltage V_o (i.e., load voltage V_R), (d) capacitor C_1 voltage V_{C1}, (e) V_{D1} voltage across D_1, (f) diode D_4 voltage V_{D4}, (g) inductor L_1 current I_{L1}, (h) output current I_o

As depicted in Fig. 11a, the switch tube's driving voltage V_{GS} signal cycle is approximately 20 μs (frequency $f = 50$ kHz). The conduction drive voltage is 15 V, while the turn-off drive voltage is −5 V. The drive voltage signal meets the requirements of the SiC switch tube. Experimental results in Figs. 11b∼11h are basically in agreement with theoretical calculation results. Nonetheless, the components are actually not ideal, and there are slight discrepancies between experimental and theoretical results. From Figs. 11c and 11h, the prototype's output voltage V_o (i.e., load voltage) and output current I_o are about 72.9 V and 0.72 A, respectively. However, the theoretical calculated values for V_o and I_o are 75.5 V and 0.75 A, respectively. The experimental values for V_o and I_o are lower by 3.44% and 4%, respectively, due to power loss of the devices. Fig. 11d illustrates that the capacitor voltage V_{c1} is consistent with the theoretical value of 20 V. The capacitor voltage stress is relatively low. From Figs. 11e∼11f, diode voltages V_{D1} and V_{D4} are approximately 19.8 and 32.2 V, respectively, consistent with theoretical calculation results. The experimental prototype has a higher voltage gain and lower device stress at a lower duty cycle. Table 4 presents a comprehensive comparison of the theoretical calculations, simulations, and experimental results for each parameter of the converter proposed in this paper. Table 4 indicates that the simulation and experimental results are largely consistent with the theoretical calculations, exhibiting minor errors, which affirms the accuracy of the theoretical analysis.

Fig. 12 illustrates the dynamic experimental waveform of the output voltage when the converter transitions from half load to full load. As indicated by Fig. 12, when the output power jumps from 28.5 to 57 W, the output voltage experiences a dynamic response, demonstrating a slight overshoot of approximately 2.1 V and a short adjustment time of approximately 18 ms. The experimental dynamic analysis results also attest to the proposed converter's excellent dynamic performance.

Table 4: Comparison of theoretical calculations, simulations, and experimental results for each parameter of the proposed converter

Parameters	Theoretical results	Simulation results	Experimental results	Error between simulation and theoretical results	Error between experimental and theoretical results
V_o (V_R)	75.5 V	75.45 V	72.90 V	0.07%	3.44%
I_o	0.75 A	0.75 A	0.72 A	0%	4%
I_{L1}	4.75 A	4.71 A	4.65 A	0.4%	2.11%
I_{L2}	2.02 A	1.98 A	1.95 A	1.9%	3.38%
I_{L3}	1.26 A	1.25 A	1.24 A	0.7%	1.5%
V_{C1}	20 V	20.01 V	19.9 V	0.05%	0.05%
V_{C2}	20 V	20.02 V	19.8 V	0.1%	0.1%
V_{C3}	13.33 V	13.3 V	12.89 V	0.2%	3.3%
V_{C4}	75.5 V	75.45 V	73 V	0.1%	3.31%
V_S	75.5 V	75.5 V	73.01 V	0.07%	3.3%
V_{D1}	20 V	20.01 V	19.8 V	0.05%	0.1%
V_{D2}	20 V	20.01 V	20.01 V	0.05%	0.05%
V_{D3}	55.56 V	55.5 V	54.8 V	0.1%	1.4%
V_{D4}	33.33 V	33.3 V	32.2 V	0.09%	3.4%
V_{D5}	22.25 V	22.26 V	22.13 V	0.04%	0.54%
V_{D6}	75.5 V	75.45 V	73.08 V	0.07%	3.2%

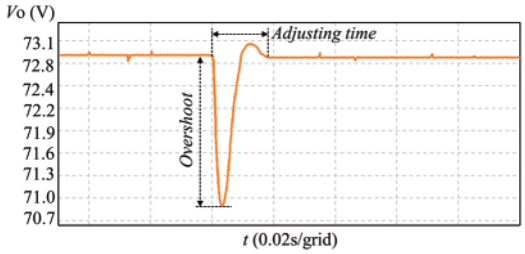

Figure 12: Output voltage dynamic experimental waveform

The power loss and conversion efficiency of the converter proposed in this paper are further analyzed. The theoretical efficiency and experimental efficiency of the converter are compared under varying duty ratios, as illustrated in Fig. 13a. While the experimental efficiency is slightly lower than the theoretical efficiency, the two measures remain generally close, exhibiting an error of less than 3%. This validates the accuracy of the theoretical calculation. Moreover, as the duty cycle increases, the theoretical and experimental efficiencies first increase and then decrease. Notably, when the duty ratio is 0.4, the power loss is found to be the smallest, and the theoretical and experimental efficiencies are the highest, reaching 93% and 91.9%, respectively. This observation confirms that the converter proposed in this study boasts high voltage gain and low device stress, while also achieving high conversion efficiency.

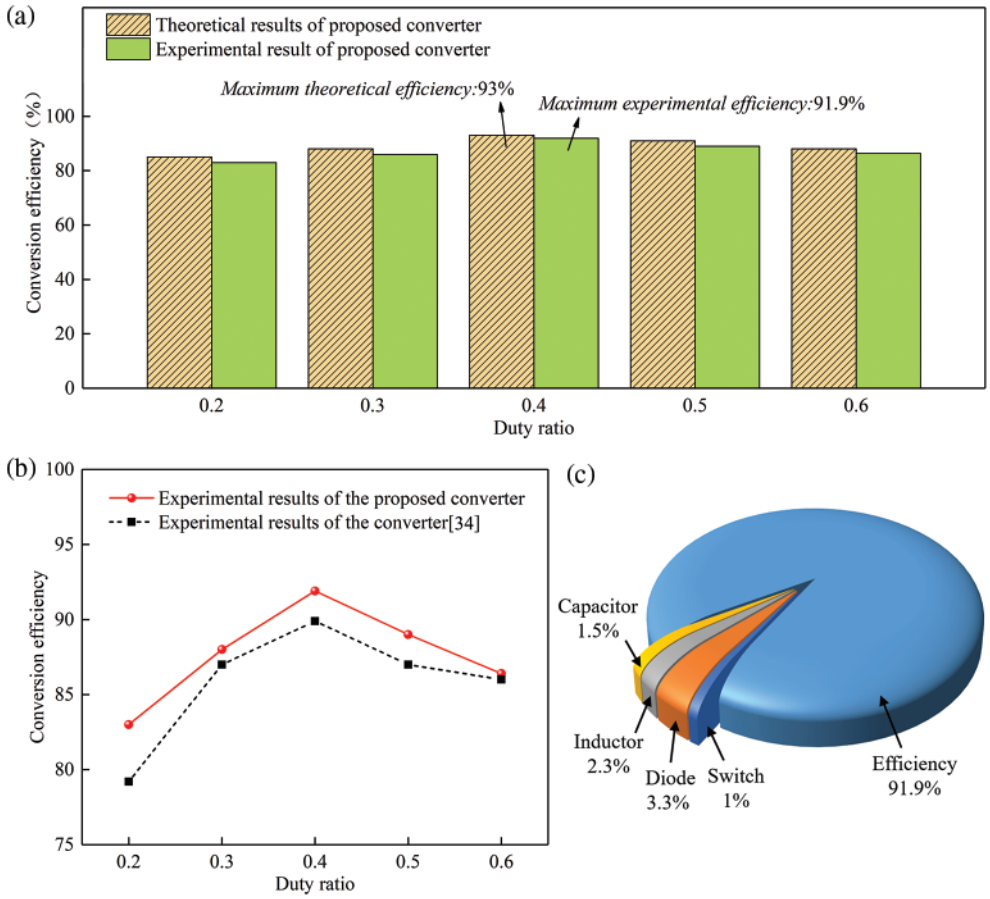

Figure 13: Power loss, conversion efficiency, and comparison: (a) the theoretical conversion efficiency and experimental efficiency of the proposed converter, (b) the experimental efficiency comparison, (c) the power loss distribution of the proposed converter

Furthermore, a comparison is made between the experimental efficiency of the proposed converter and that of a converter presented in a prior study [34], both under the same input voltage of 12 V, as illustrated in Fig. 13b. Although the efficiency of the proposed converter is almost identical to that of the converter [34] at a duty ratio of 0.6, the proposed converter exhibits a higher efficiency than the latter at duty ratios of 0.2, 0.3, 0.4, and 0.5, thus presenting a notable conversion efficiency advantage. Finally, Fig. 13c illustrates the power loss distribution of the proposed converter at a duty ratio of 0.4. The switch tube loss is the smallest, accounting for only 1% of the total loss. Meanwhile, the capacitor, inductor, and diode losses are found to account for 1.5%, 2.3%, and 3.3%, respectively. To further enhance the efficiency of the converter proposed in this work, high-quality circuit devices could be utilized.

6 Conclusion

This study introduces a novel non-isolated cubic high-gain DC-DC converter based on the traditional quadratic DC-DC boost converter by incorporating a SC and a SL-SC unit. Firstly, the proposed converter's details are elaborated, including its topology structure, operating mode, voltage

gain, device stress, and power loss. Subsequently, a comparative analysis is conducted on the voltage gain and device stress between the proposed converter and other high-gain converters. Then, a closed-loop simulation system is constructed to obtain simulation waveforms of various devices and explore the dynamic performance. Lastly, an experimental prototype is built, experimental waveforms are obtained, and the experimental dynamic performance and conversion efficiency are analyzed. The theoretical analysis's correctness is verified through simulation and experimental results. The proposed converter achieves a high voltage gain at low device stress and high conversion efficiency, realizing a good balance between voltage gain, device stress, and power loss. The proposed converter is well-suited for renewable energy systems and holds theoretical significance and practical value in renewable energy applications. It offers a viable solution to the issue of low output voltage in renewable energy power generation systems. In future research, the emphasis will be placed on verifying the practical application effect of the proposed converter in renewable energy systems, exploring its working performance in various renewable energy systems such as new energy vehicles and photovoltaic power generation, and targeting improvements and optimizations to enhance its practicality.

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Availability of Data and Materials: Data supporting this study are included within the article.

Conflicts of Interest: The authors declare that they have no conflicts of interest to report regarding the present study.

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