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# High-Bandwidth, Low-Power CMOS Transistor Based CAB for Field Programmable Analog Array

**Ameen Bin Obadi[1], Alaa El-Din Hussein[2], Samir Salem Al-Bawri[3,4,*], Kabir Hossain[5], Abdullah Abdulhameed[4], Muzammil Jusoh[1,6,7], Thennarasan Sabapathy[1,6], Ahmed Jamal Abdullah Al-Gburi[8] and Mahmoud A. Albreem[9]**

[1]Advanced Communication Engineering (ACE), Centre of Excellence, Universiti Malaysia Perlis (UniMAP), Faculty of Electronic Engineering Technology, Kangar, 01000, Malaysia
[2]Electrical Engineering, King Fahd University of Petroleum and Minerals, Dhahran, Eastern, 31261, Saudi Arabia
[3]Space Science Centre, Climate Change Institute, Universiti Kebangsaan Malaysia, Bangi, 43600, Malaysia
[4]Department of Electronics & Communication Engineering, Faculty of Engineering & Petroleum, Hadhramout University, Al-Mukalla, Hadhramout, 50512, Yemen
[5]Faculty of Engineering, Norwegian University of Science and Technology (NTNU), Gjøvik, N-2815, Norway
[6]Faculty of Electronic Engineering Technology, Universiti Malaysia Perlis (UniMAP), Kampus Alam UniMAP Pauh Putra, Arau, 02600, Malaysia
[7]Department of General Educational Development, Faculty of Science and Information Technology (FSIT), Daffodil International University, Dhaka, 1207, Bangladesh
[8]Department of Electronics and Computer Engineering (FKEKK), Center for Telecommunication Research and Innovation (CeTRI), Universiti Teknikal Malaysia Melaka (UTeM), Durian Tungal, 76100, Malaysia
[9]Department of Electrical Engineering, University of Sharjah, Sharjah, 27272, United Arab Emirates
*Corresponding Author: Samir Salem Al-Bawri. Email: samir@ukm.edu.my
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**Abstract:** This article presents an integrated current mode configurable analog block (CAB) system for field-programmable analog array (FPAA). The proposed architecture is based on the complementary metal-oxide semiconductor (CMOS) transistor level design where MOSFET transistors operating in the saturation region are adopted. The proposed CAB architecture is designed to implement six of the widely used current mode operations in analog processing systems: addition, subtraction, integration, multiplication, division, and pass operation. The functionality of the proposed CAB is demonstrated through these six operations, where each operation is chosen based on the user's selection in the CAB interface system. The architecture of the CAB system proposes an optimized way of designing and integrating only three functional cells with the interface circuitry to achieve the six operations. Furthermore, optimized programming and digital tuning circuitry are implemented in the architecture to control and interface with the functional cells. Moreover, these designed programming and tuning circuitries play an essential role in optimizing the performance of the proposed design. Simulation of the proposed CMOS Transistor Based CAB system is carried out using Tanner EDA Tools in 0.35 µm standard CMOS technology. The design uses a ±1.5 V power supply and results in maximum 3 dB bandwidth of 34.9 MHz and an

approximate size of 0.0537 $mm^2$. This demonstrates the advantages of the design over the current state-of-the-art designs presented for comparison in this article. Consequently, the proposed design has a clear aspect of simplicity, low power consumption, and high bandwidth operation, which makes it a suitable candidate for mobile telecommunications applications.

**Keywords:** CMOS; field programmable analog array; configurable analog block; current mode circuit

## 1 Introduction

Since the early 1990s of the previous century, researchers have begun to develop numerous designs of the analog equivalent of the field-programmable gate array (FPGA), which is the field-programmable analog array (FPAA) [1]. Analog solutions are becoming increasingly competitive with digital circuits, particularly for compact, low-power, and high-speed applications [2]. This is despite the fact that digital processing circuits currently hold the majority of the market share. This is because analog circuits are capable of performing essential signal processing activities quicker than their digital counterparts while also consuming less power and occupying a smaller area of silicon. The true value of FPAA design comes from its application in the prototyping, testing, and development of analog circuits. Because of its reconfigurable architecture, which enables rapid and low-cost prototyping, the FPAA would be an excellent tool for testing and prototyping analog circuitry design [2]. In addition, the use of analog circuits would be made accessible to designers who do not have extensive expertise in the relevant subject, capitalizing on the FPAAs features. Therefore, the trend toward shorter design cycles and cheaper prices for analog integrated circuits has required the creation of various advances in the area of FPAA and related configurable analog blocks (CABs) [3]. These advancements have been necessary because of the nature of the field itself and the need to reach a commonly used widely acceptable CAB Structure.

### *1.1 Related Work*

There has been recent interest by researchers in the area of FPAA and the design of its core element, which is the CAB. Many publications in the literature used active elements such as operational amplifier (Op-amp), operational transconductance amplifier (OTA), second-generation current conveyors (CCII), or current feedback operational amplifier (CFOA) in the design of CAB [4–8]. At this time, the vast majority of the FPAAs that are available (commercially and academically) are often based on CABs that involve operational amplifiers or other analog primitives with a similar function [9–11]. Because these designs are dependent on the active elements, the resulting CAB performance was restricted according to the capabilities of the elements themselves. In addition, some designs do not contain any active components; rather, these designs are built at the transistor level [1,12]. The transistor level design CAB can be accomplished with metal–oxide–semiconductor field-effect transistor (MOSFET) sub-threshold as described in [13], with BJT transistors as presented in [14], or with a multi trans-linear element (MITE) and Floating gate transistors (FG) as shown in [1,15]. Because of this, numerous CAB designs have been developed. These designs are at the core of the FPAA systems. The transistor level-based approach and other similar approaches were also the basis of the designs presented in [13,14,16].

The following Table 1 summarizes some of the designs in the literature and provides a comparative analysis of the approach adopted in each design and other important design features.

**Table 1:** Summary of related work and previous CAB designs

| Reference | Approach | Programmability & Configurability | BW | Remarks |
|---|---|---|---|---|
| [1] | Multi-input transient element (MITE) approach using sub-threshold pFETs. | Floating gate transistors. | 200 kHz | Used for LPF, HPF, and RMS to DC converter applications |
| [14,31] | CFOA and programmable R's & C's based approach using 0.35 µm CMOS technology | MOS pass transistor switch. | 11.3 MHZ | Used for signal processing and filtering |
| [16,33] | Current mode, transistor primitive based using 2 µm CMOS technology. | Branch activation via transistor switches | 10 MHz | Operates in saturation. |
| [18,34] | Current mode BJT transistor level approach | Modifying block's biasing conditions | 100 MHz in BPF | Used in universal filter application. |
| [29] | programmable OTA & capacitors-based approach using 2 µm CMOS technology in strong inversion | Programmable capacitors & MOS switches | Few kHz to few MHz | Used for continuous signal processing |
| [30] | Voltage mode digitally Programmable CCII-based approach using 90 nm CMOS technology | Direct wiring | 11.6 MHz | The resulting FPAA uses seven CABs arranged in a letter "I" structure. |

### *1.2 Research Gap and Contribution*

As highlighted earlier, the vast majority of available CAB designs incorporate an active element(s) as the basis of the design structure. Consequently, the designed CABs can only perform to the capabilities limits of the individual active element(s). Therefore, this article presents a design for a configurable analog block system based on the transistor-level design technique of MOSFETs operating in strong inversion. As a result, the highlighted limitations of using active primitive elements in the CAB are avoided, which opens the potential for numerous advancements in the CAB design. Furthermore, minimal research has been carried out in this field using a transistor-level design approach; hence, we took strides to contribute to this field. Even though few designs exist based on similar approaches, our proposed work innovatively incorporates several enhanced features in an optimized way.

The ever-presented demand for high-frequency operation and lower supply voltages are among the main requirements that affect the design of the CABs of any FPAA [17]. As highlighted throughout this

paper, the overall findings showed improved performance regarding the amount of power consumed and the bandwidth available based on our adopted method. Due to the system's integrated interface circuitry of the proposed design, it only utilizes three functional cells to perform addition/subtraction/pass, integration, and multiplication/division based on the user's selection. Apart from that, the outcome from the system suggested that the programming of the functions and parameters should primarily be accomplished by modifying the bias condition of the circuits, in addition to the limited use of three switches. Moreover, the use of limited switches is partially regarded for the bandwidth optimization.

The main contribution of this work is summarized in the following points:

- Design of a new optimized CAB structure at the transistor level with advanced features of high bandwidth, low power consumption, and a relatively small area for potential use as the main block in FPAA design.
- Design of a current mode functional cell at the transistor level to perform addition, subtraction, and pass functions with all programming, tuning, and interfacing circuitry needed.
- Design of a current model functional cell at the transistor level to perform integration function through optimizing an inverter lossless integrator and designing all programming, tuning, and interfacing circuitry needed.
- Design of a current model functional cell at the transistor level to perform multiplication and division functions through optimizing a current mode multiplier and designing all programming, tuning, and interfacing circuitry needed.
- Design of all interconnections and switches needed for the overall integration.
- Optimized Integration of the three design functional cells for advanced performance in bandwidth, power consumption, and area occupation.

The rest of this paper is organized as follows (2) Proposed Design (3) Results and Discussion (4) Conclusion.

## 2 Proposed Design

The CAB system circuitry is integrated and structured uniquely to make reconfigurability possible and to reduce power consumption for the unused parts of the design during certain operations. Fig. 1 depicts the proposed design, which consists mainly of the three functional cells connected in series where each is capable of processing certain functions on the input signals. The "adder, subtractor, pass" cell is the first cell in the circuit, and it is the one into which the input is initially inserted. The output of this cell is connected to the subsequent cell, which is an integrator cell. Within this cell, the signal can either be integrated or simply bypassed through a switch and sent on to the subsequent cell. The multiplier/divider cell is represented by the third cell in Fig. 1. The current mirrors at the output are connected to the multiplier/divider cell's output to complete the circuit. Since the three cells make up the CAB, this architecture makes it possible for the CAB to implement a single function, double functions, or even triple functions all at the same time. This is because the CAB is set up in such a way that each cell's bias currents can be individually controlled, allowing for activation or deactivation of the cell as needed. In addition, the design reduces the amount of power consumption required during the activation and deactivation of the bias currents present in the system.

Furthermore, bias current circuits are integrated with each cell to make activation and deactivation possible. Each functional cell was designed and then integrated with its bias currents. The final circuit of each designed cell was then simulated for its intended functionality.

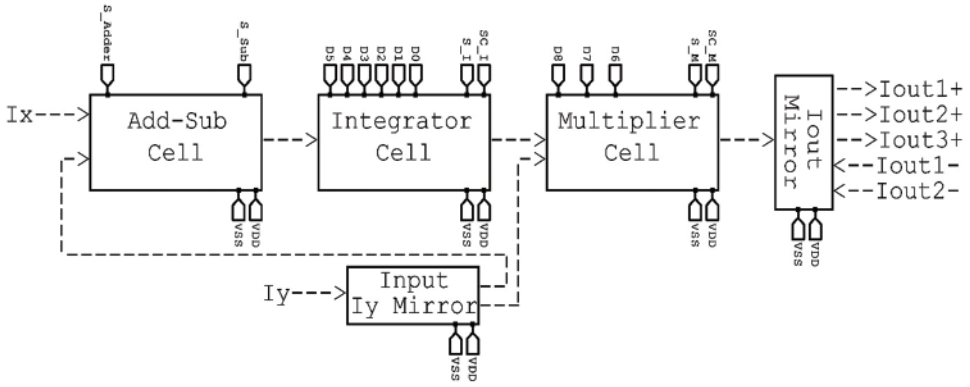



**Figure 1:** Proposed CAB system design and interfacing

### *2.1 Adder/Subtractor/Pass Functional Cell*

Even though addition and subtraction can be done relatively easily in the current mode, the proposed design avoids using switches in the signal path to ensure optimum performance, as depicted in Fig. 2. The current sources controlled the cell programmability are $I_{s1}$, $I_{s2}$, $I_{s3}$, $I_{a1}$, $I_{a2}$ and $I_{a3}$ as per the presented settings in Table 2 when $I_{s1}$, $I_{s2}$, $I_{s3}$, $I_{a1}$, $I_{a2}$ and $I_{a3}$ were considered as OFF condition, causes zero current to flow from the input node of the circuit Iy to $I_{out}$ so Ix.is passed directly as the output. The Addition case is achieved by setting $I_{s1}$, $I_{s2}$ and $I_{s3}$ to zero to ensure that no current is flowing from the drain of NMOS_s6 to the output node. At the same time, $I_{a1}$, $I_{a2}$ and $I_{a3}$ are kept ON delivering a copy of $I_y$ to $I_x$ node.

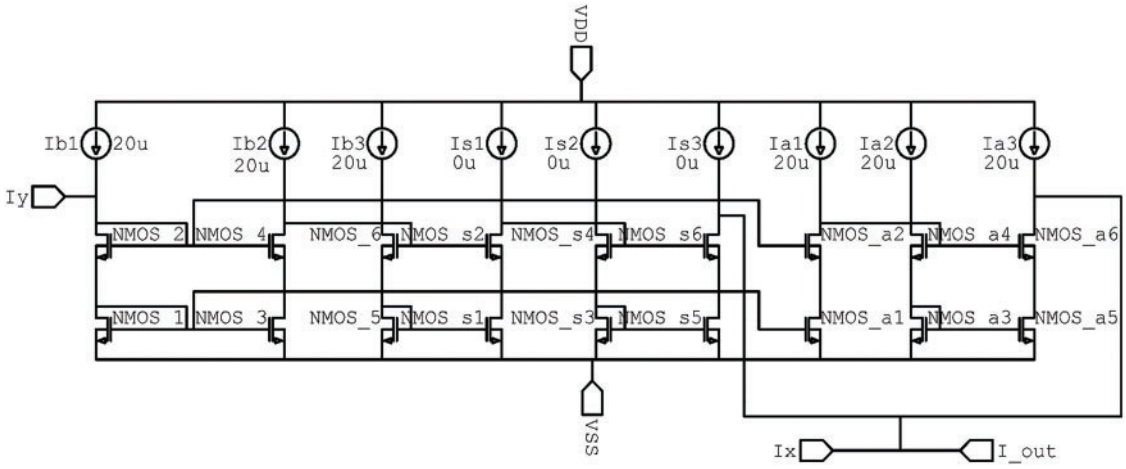



**Figure 2:** Proposed adder/subtractor/pass functional cell design

In the subtraction case, an inverted copy of $\mathbf{I_y}$ is delivered to $\mathbf{I_x}$ node while no current is flowing from the drain of **NMOS_a6** to the output node. This is done by activating certain current sources and deactivating others where specific operation selection can be achieved. This control can be done in the CAB design using the digital bit. In addition to reconfigurability, this helps in reducing the power consumption of the proposed system.

**Table 2:** Function modes of addition/subtraction/pass circuit

| Function mode | $I_{s1}$ | $I_{s2}$ | $I_{s3}$ | $I_{a1}$ | $I_{a2}$ | $I_{a3}$ |
|---|---|---|---|---|---|---|
| Pass ($I_{out} = I_x$) | OFF | OFF | OFF | OFF | OFF | OFF |
| Adder ($I_{out} = I_x + I_y$) | OFF | OFF | OFF | ON | ON | ON |
| Subtractor ($I_{out} = I_x$-$I_y$) | ON | ON | ON | OFF | OFF | OFF |

### *2.2 Integrator Circuit*

Switchless current mode integrators are highly recommended because the extensive use of switches and capacitors can severely degrade the frequency response of the circuit [18]. Several continuous time current mode integrators have been reported in the literature. One family of such integrators is the current mirrors transconductance capacitance ($G_m$_C) type and their filters [13,19–22]. The basic component of this type is the MOSFET trans-conductance and an additional capacitance. Most of the referred circuits are realized by cascading two inverting current mirrors (amplifiers), with the output of the second stage fed back to the first stage. The additional capacitance is placed in parallel with the input node for the circuit to realize a $G_m$_C block. These integrators can operate at relatively high frequencies, as in [13,20,21]. In addition, a fully differential version or inverting version can be easily made as in [19,20]. Moreover, they are capable of operation at low voltage and consumption of low power [13,19,20,22].

An integrator that is very much like the one described in [20] and shown in Fig. 3 was utilized here. The integrator in [20] does not make use of starting low-frequency operation. Its starting frequency operation is somewhere around 100 kHz, but for extended use and utilization, it needs to be extended to lower frequencies than that. In addition to this, it cannot be configured, nor can it be programmed. The proposed integrator shown in Fig. 3 gets around these restrictions by considering the values of the bias current to increase the frequency at which it can function. Furthermore, the integrator is made configurable through the manipulation of the bias currents that are used in the circuit. The components of this circuit are a capacitor labeled C 1, two straightforward current mirrors, and biasing currents. The operation of the integrator can be controlled and fine-tuned through the use of programmable current sources, as shown in Fig. 3. However, Fig. 4 depicts the small-signal model of the circuit with the output conductance omitted from consideration based on the mathematical model of low-level signals:

$$I_{in} = g_{m\_2} * V_A + (g_{m\_3} + SC\_1) * V_B \tag{1}$$

$$I_f = g_{m\_1} * V_A \tag{2}$$

$$I_f = -g_{m\_4} * V_B \tag{3}$$

Assuming that $g_{m\_1} = g_{m\_2}$ and $g_{m\_3} = g_{m\_4}$, the substitution of (2) and (3) into (1) results in:

$$I_{in} = g_{m\_2} * \frac{I_f}{g_{m\_1}} + (g_{m\_3} + SC\_1) * \left(-\frac{I_f}{g_{m\_4}}\right) \tag{4}$$

$$I_f = (-g_{m\_3}/SC\_1) * I_{in} \tag{5}$$

Since $I_f = I_{out}$, then:

$$\frac{I_{out}}{I_{in}} = -g_{m\_3}/SC\_1 = -A/S \tag{6}$$

Eq. (6) represents the transfer function of an inverting type lossless integrator. The integrator unity gain frequency is determined by the factor $\left(A = \omega = \frac{gm}{C}\right)$ which depends on MOSFET trans-conductance $g_m$:

$$g_m = \sqrt{2 * \mu_o * C_{ox} * W/L * I_c} \tag{7}$$

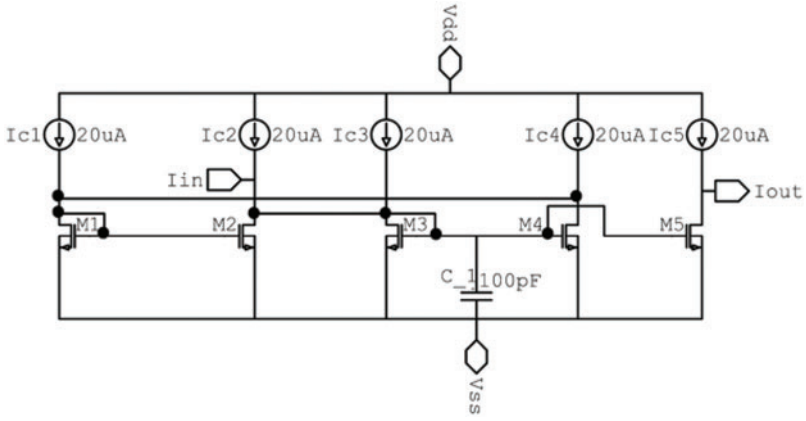



**Figure 3:** Proposed inverting lossless integrator

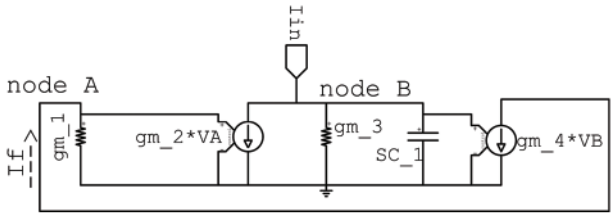



**Figure 4:** Integrator small signal model

### *2.3 Multiplier/Divider Circuit*

Multiplier circuits are very fundamental blocks in signal processing systems. This justifies the growing interest in developing this circuit, proven by many publications in this area; see [23–27]. A multiplier/divider circuit is reported in [23]. That circuit is based on dual trans-linear loops of MOSFET transistors operating in saturation. It is reported to achieve a bandwidth of 41.8 MHZ and power consumption of 340 μW. The improved circuit to [23] is in [28] and is designed by the authors of this paper to be used in the CAB design.

Fig. 5 represents the circuit structure of the proposed designed multiplier/divider circuit reported in [28] and proposed to be used here. Its achieved bandwidth has been enhanced to 440 MHz and the reported power consumption is reduced to about 158 μW. The relationship between the input currents ($I_x$, $I_y$) and output current $I_{out}$ of Fig. 5 is given by (8). It is derived assuming all transistors are in

saturation, $I_{b1} = I_{b2} = I_b$ (constant biasing current) and the trans-linear loop transistors are matched (for full derivation details, refer to [28]).

$$I_{out} = \frac{I_x I_y}{I_b} \tag{8}$$

From (8), it is obvious that the circuit functions as a multiplication of two signals $I_x$ and $I_y$, or a division by $I_b$.

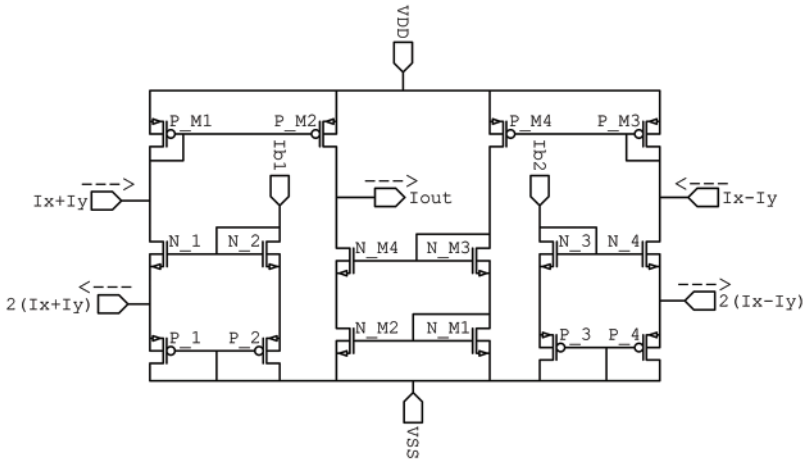
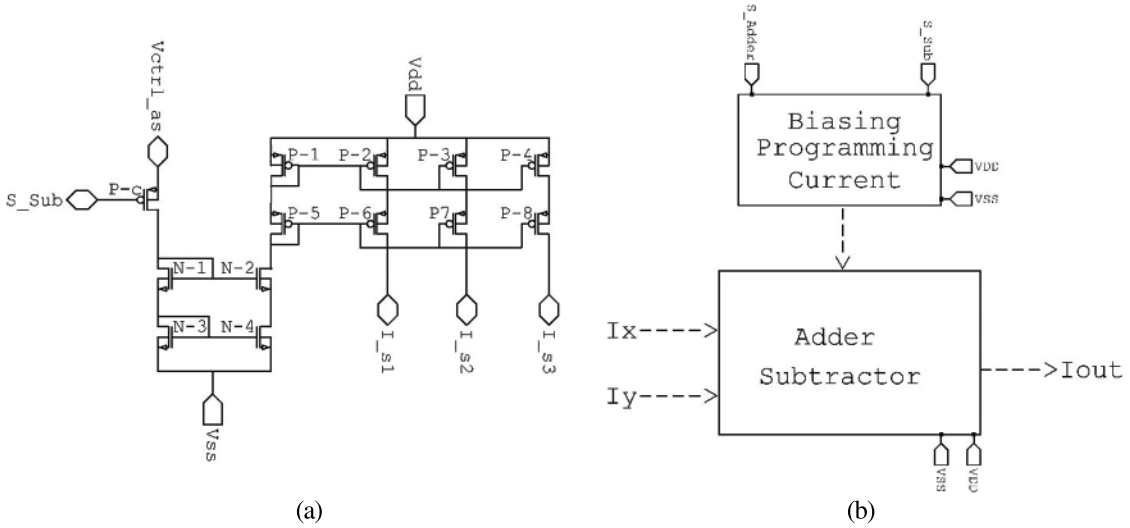



**Figure 5:** Proposed multiplier/divider circuit designed by the same authors in [28]

### *2.4 Configurable Biasing Sources, Programmable Tuning, and Interfacing Circuit Design*

The designed circuit was used as the configuring tool for the adder/subtractor is presented in Fig. 6a. It can to activate or deactivate the biasing currents. This, in turn, activates or deactivates the complete circuit connected to the biasing currents. This circuit was used to bias the adder-subtractor circuit previously shown in Fig. 2. This circuit generates three equal copies of current $I_{s1} = I_{s2} = I_{s3} =$ 20 μA. The value of this current depends on the voltage difference between the gate and the source of transistor P_c. The gate of this transistor controls the output currents and makes them either ON or OFF via S_Sub. Using the same principle, different copies of the similar circuit were used to bias and program the addition operation. Fig. 6b shows the complete circuit of addition/subtraction/pass functionality with the interface and programming currents. This circuit can be controlled with just two bits, S_sub and S_adder.

To control and tune the parameters of the integrator circuit, programmable tunable currents need to be designed and used in the integrator circuit as part of the configuring tool [18]. The digitally programmable currents circuit in Fig. 7 was used. The tunability in the design was achieved at two levels: coarse tuning and fine tuning. The circuit in Fig. 7 achieves the coarse tuning; The coarse tuning circuit can generate a current ranging from 0 μA to 70 μA in increments of 10 μA. A similar circuit, which operates according to the same fundamental principle, can also be used as fine tuning for the integrator biasing and can produce a current that varies from 0 μA to 7 μA by an increment of 1 μA. In addition, the multiplier/divider fine tunability of the bias current Ib is demonstrated by using a similar circuit design, which is based on the same principle.




(a) (b)

**Figure 6:** (a) Programming circuit for subtraction cell, (b) complete adder/subtractor configurable cell

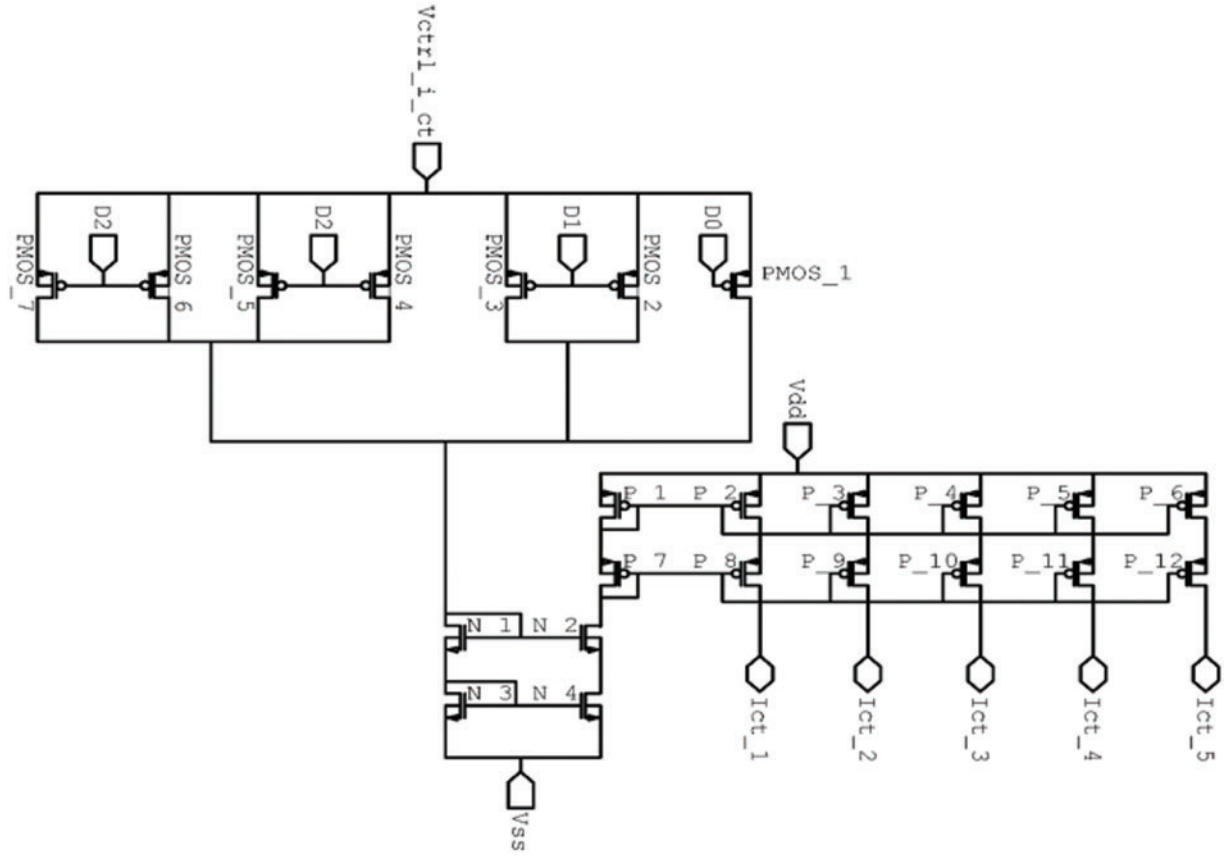



**Figure 7:** Digitally programmable coarse tuning current for the integrator

Fig. 8 presents the complete integrator programmable and tunable structure. This part of the overall design is programmed and controlled by five bits D_0 to D_5. In addition, limited use of only one switch at the input node is adopted. Furthermore, Fig. 9 shows the complete structure of the multiplier/divider circuit including the current mirrors, biasing and tuning currents, and limited use of two switches at the input and the output of the structure. It can also be noticed that this block can be controlled with three bits D_6 to D_8.

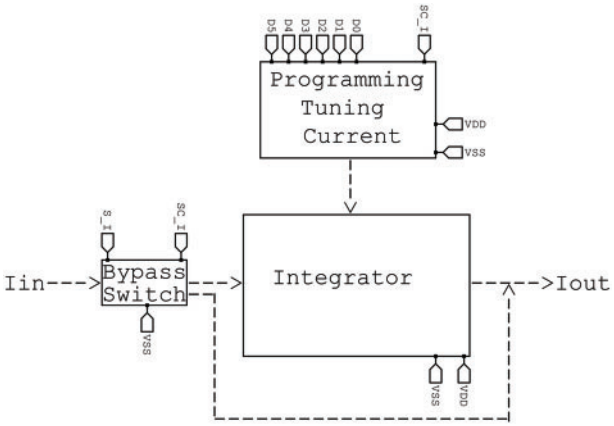



**Figure 8:** Complete integrator tunable cell

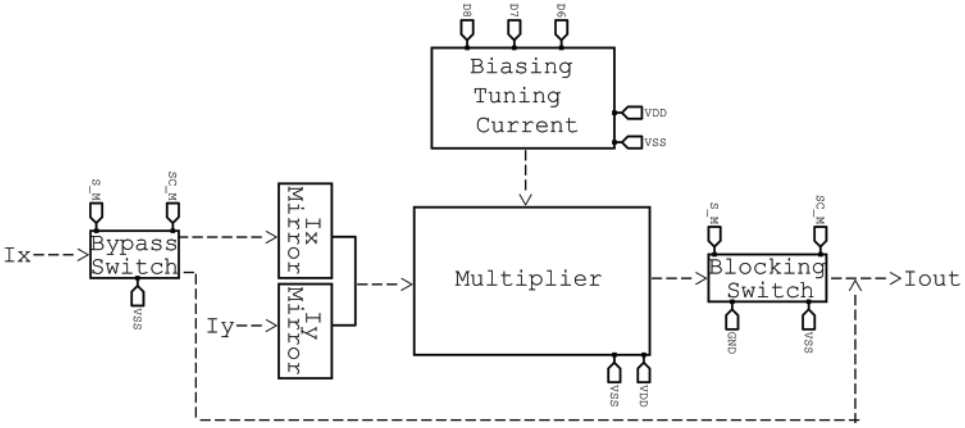



**Figure 9:** Complete configurable and tunable multiplier/divider cell

The utilization of CMOS transistor switches is included as a component of the design in very limited cases. A bypass switch and a blocking switch are the two kinds of switches that are utilized here. The bypass switch is situated at the integrator's input and can either allow the input to be incorporated into the circuit or divert it directly to the output of the integrator. Additionally, bypass transistors with the same functionality were utilized at the input (Ix) of the multiplier/divider. The output of the multiplier/divider was where the blocking switch was utilized. It only permits the current to flow in one direction from the output (out of the multiplier).

### *2.5 Control Word and Overall, CAB Interface*

The mode of operation of the CAB can be digitally selected using the bits that are displayed in Table 3, which are part of the control word. According to the preferences of the user, each of these bits in the table is in charge of activating or deactivating a specific part of the system that was designed. At this point, it is possible to ascertain the comprehensive CAB digital control word. It is made up of a total of 13 bits. As can be seen in Fig. 10, it is split into two sections: the part that deals with programming and the part that deals with tuning. Fig. 10 illustrates how the CAB interfaces with the control word.

**Table 3:** Programming bits for function selection

| $B3$ | $B2$ | $B1$ | $B0$ | Function |
|---|---|---|---|---|
| 0 | 0 | 1 | 1 | Pass |
| 0 | 0 | 1 | 0 | Addition |
| 0 | 0 | 0 | 1 | Subtraction |
| 0 | 1 | 1 | 1 | Integration |
| 1 | 0 | 1 | 1 | Multiplication/Division |

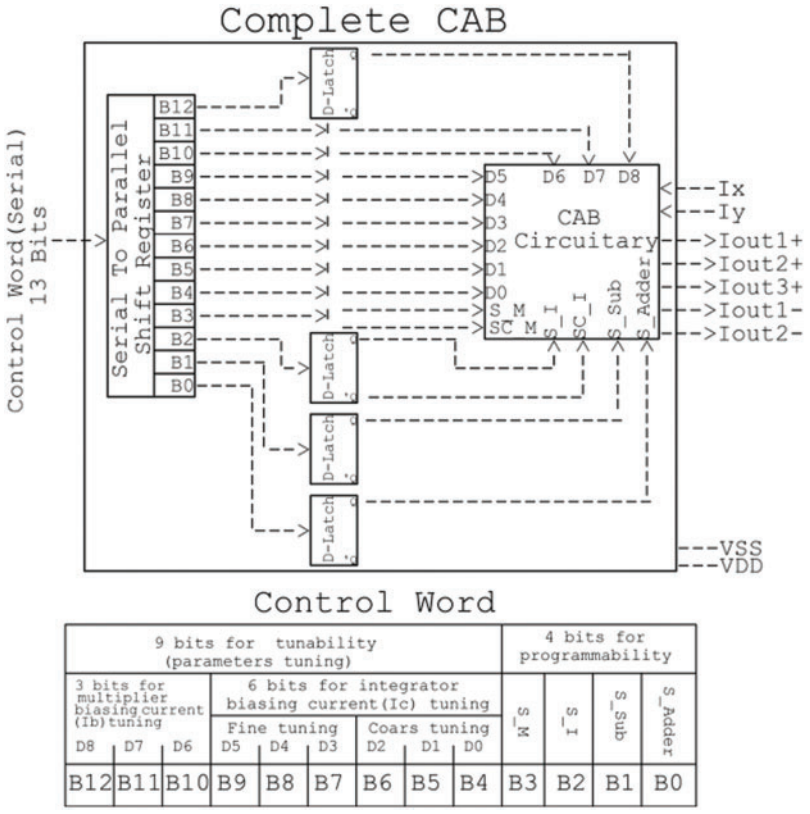
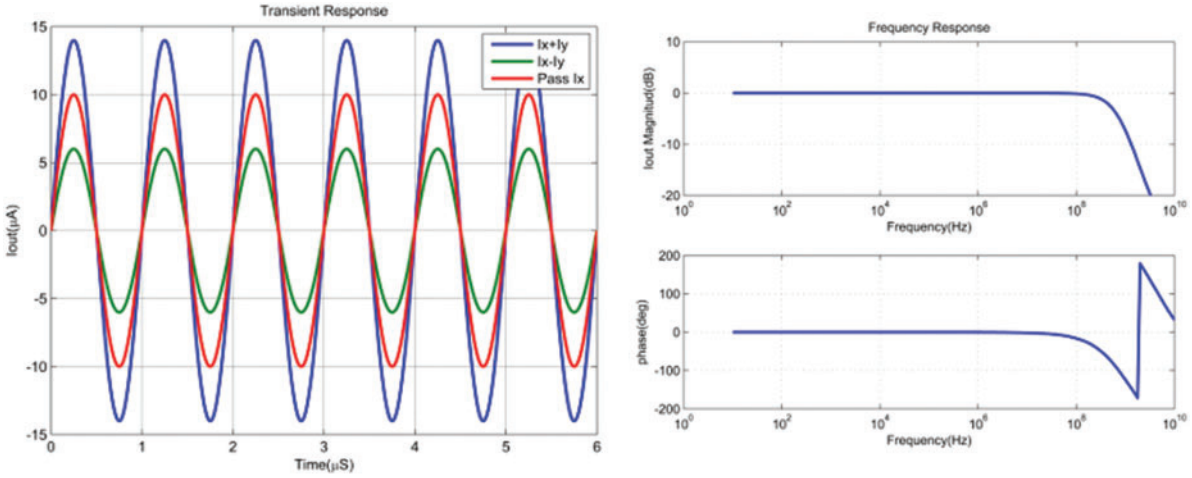



**Figure 10:** Complete CAB Illustration with the control word

## 3 Results and Discussion

To investigate the performance of the proposed circuits and to prove their functionality, Tanner simulation results are reported in this section using 0.35 µm standard CMOS technology. Simulation results of the circuit in Fig. 2 are obtained at biasing currents = 20 µA or 0 µA, $V_{dd}$ and $V_{ss}$ = ±1.5V and $R_{Load}$ = 1kΩ. The reported linearity errors are 0.065%, 0.075%, and almost 0% in the case of addition, subtraction, and pass, respectively. The power consumption in each case is 170, 170, and 84 µW, respectively.

Fig. 11a shows the transient response of the circuit when the inputs are sinusoidal signals. The input $I_x$ has an amplitude of 10 µA and frequency 1 MHz while $I_y$ has an amplitude of 4 µA and frequency of 1 MHz. The resulting output is shown for the three functions. Fig. 11b shows the magnitude and phase frequency characteristics of the circuit. The −3 dB bandwidth achieved is 550 MHz.

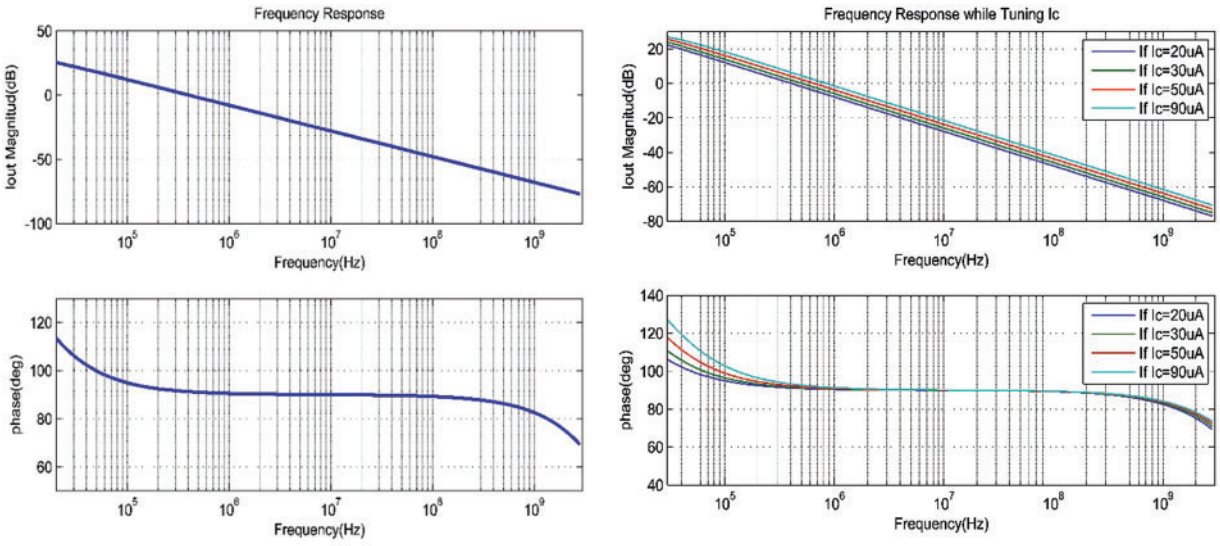



(a) (b)

**Figure 11:** (a) Transient response of the adder-subtractor cell for addition, subtraction, and pass, (b) frequency response of the adder-subtractor cell

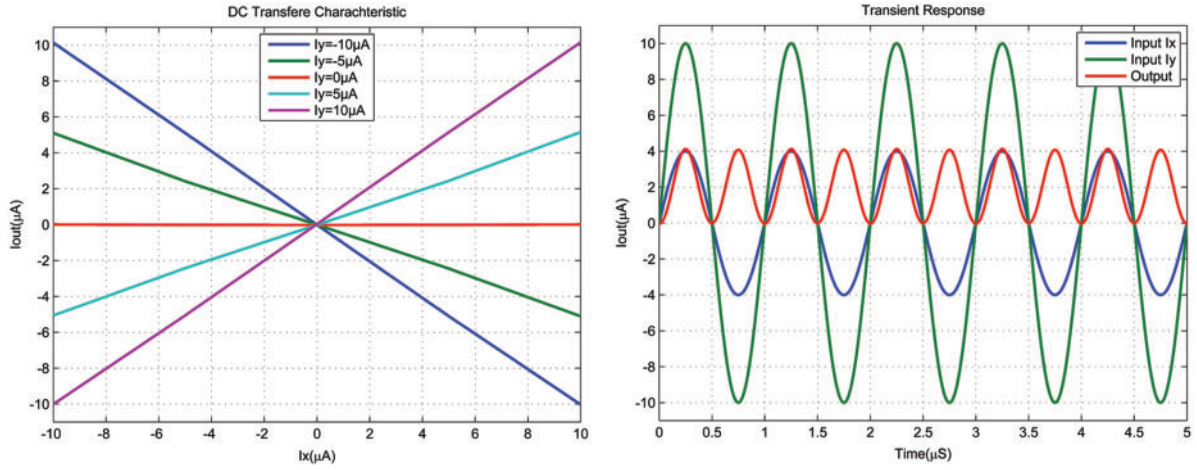
Simulation results of the circuit in Fig. 3 are obtained at biasing currents $I_{c1}$ to $I_{c5}$ = 20 µA, $V_{dd}$&$V_{ss}$ = ±1.5 V, capacitor C_1 = 100pF and $R_{Load}$ = 1kΩ. The power consumption of the circuit is around 87 µW. Fig. 12a depicts the phase and magnitude frequency response of the integrator, which reveals that it is capable of performing admirably from a frequency of 20 kHz up to a few gigahertz in range. On the other hand, the phase response exhibits deviations at the beginning and the end of the frequency range, which results in phase error. However, Fig. 12b illustrates the frequency response of the integrator while the value of the bias current is being tuned to various values, including 20, 30, 50, and 90 nA. It has been demonstrated that one can control the frequency at which unity gain is achieved by adjusting the bias current. Because of this, the potential exists for this integrator to be used in applications involving filters with controlled cutoff frequencies.

Simulation of the proposed multiplier/divider is carried out based on the following circuit parameters: $V_{dd}$ & $V_{ss}$ = ±1.5 V, bias current $I_b$ = 10 µA, and the output port is connected to a load resistance $R_{Load}$ = 1kΩ. The DC transfer characteristic of the proposed multiplier/divider is depicted in Fig. 13a when both inputs (Ix and Iy) were subjected to a range of variation between −10 microamperes and 10 microamperes.




(a) (b)

**Figure 12:** (a) Integrator frequency response, (b) integrator frequency response while tuning Ic




(a) (b)

**Figure 13:** (a) DC transfer characteristic of the proposed multiplier/divider, (b) transient response of the proposed multiplier/divider

The proposed circuit has an error in the linearity of approximately 1.1 percent and has a power consumption of approximately 158 microwatts. The transient response of the multiplier is depicted in Fig. 13b when both inputs (Ix and Iy) are sinusoidal signals operating at a frequency of 1 MHz with two different amplitudes. However, Fig. 14 illustrates the frequency response of the proposed multiplier/divider device. The circuit has a bandwidth of about 440 MHz when measured at a dB level of $-3$.

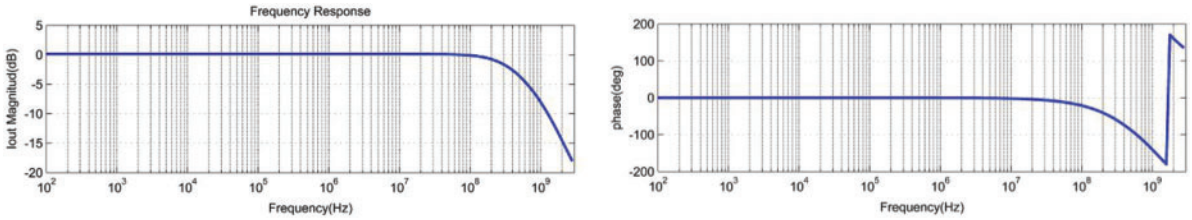



**Figure 14:** Frequency response of the proposed multiplier/divider

A comparison between the proposed CAB design and previous designs is reported in Table 4. The designs reported in [13,16] are based on the same method adopted in the proposed design. However, the proposed CAB enjoys better features, especially in terms of bandwidth. The design in [14] exhibits better bandwidth than the proposed CAB, however, this is because [14] adopts BJT technology rather than CMOS. Moreover, the introduced design consumes low power, and it is suitable for integration since it uses only MOSFET transistors and a grounded capacitor. To sum up, the main attractive features of this design are small size, simplicity, low power consumption, and high bandwidth. In addition, there is a lack of designs in the literature adopting the method used in this work which gives an advantage to this proposed design. However, one weakness of the design is in that the division function range is very limited. This is because the denominator is the bias current which can be varied only to a limited extent.

**Table 4:** Comparison between the proposed CAB design and state of the art

| Features | Ref [6] | Ref [10] | Ref [13] | Ref [14,18,34] | Ref [16,33] | Ref [18,29] | Ref [20] | Ref [30,31] | Ref [32] | Proposed CAB |
|---|---|---|---|---|---|---|---|---|---|---|
| Supply | ±0:6 V | ±0.75 V | - | ±1.5 V | - | 2.5 V | ±0.5 V | ±0.75 V | ±10 V | ±1.5 V |
| Max. 3 dB bandwidth | variable | 1.9 and 0.8 GHz | Below 100 kHz | 100 MHz | 10 MHz | few MHz | 11.6 MHz | 11.3 MHz | 575 kHz | 34.9 MHz |
| Approx. size ($\mathbf{mm}^2$) ** | - | - | 0.0338 | - | Between 0.445 and 0.89 | 0.469 | - | - | - | 0.0537 |
| Design method | OTA | Current-mode approach | Switches & transistor primitive elements | Transistor level-based design | Transistor primitive | OTA based | Digitally prog. CCII based | CFOA based | CFOA | Transistor level-based design |
| Technology | 90 nm CMOS | 0.25µm CMOS | 1.2$\mu m$ CMOS | BJT | 2$\mu m$ CMOS | 2$\mu m$ CMOS | 90 $nm$ CMOS | 0.35µm CMOS | - | 0.35$\mu m$ CMOS |
| Operation region | - | | Sub-threshold | active | saturation | Strong inversion | Saturation | Saturation | - | Strong inversion |

## 4 Conclusion

Within the scope of this paper, a novel architecture of CAB for FPAA application was presented. The current mode MOSFET transistor level was utilized for this design and was implemented to operate in the saturation region. The proposed CAB structure is capable of performing operations such as addition, subtraction, pass, multiplication, division, and integration based on only three functional cells. Because the functional cells are combined in series, the proposed design is also capable of performing double or triple operations at the same time due to the optimized functional cells. Furthermore, the programming of the CAB is accomplished primarily by adjusting the biasing condition of the circuit with limited use of switches. The proposed structure shows high-performance

results when compared to some of the state-of-the-art results. With the use of ±1.5 V, the design achieved a bandwidth of 34.9 MHz. In addition, due to the optimized simplicity of the design, its area was estimated to be around 0.0537 $mm^2$. Due to the demonstrated high performance, the designed CAB can be adopted as a core block in FPAA design.

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