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Process-dependent Thermal-Mechanical Behaviors of an Advanced Thin-Flip-Chip-on-Flex Interconnect Technology with Anisotropic Conductive Film Joints

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Abstract: User experiences for electronic devices with high portability and flexibility, good intuitive human interfaces and low cost have driven the development of semiconductor technology toward flexible electronics and display. In this study proposes, an advanced flexible interconnect technology is proposed for flexible electronics, in which an ultra-thin IC chip having a great number of micro-bumps is bonded onto a very thin flex substrate using an epoxy-based anisotropic conductive film (ACF) to form fine-pitch and reliable interconnects or joints (herein termed ACF-typed thin-flip-chip-on-flex (TFCOF) technology). The electrical and thermal -mechanical performances of the micro-joints are the key to the feasibility and effectiveness of the technology. Thus, the main goal of the study is to assess the process-induced thermal-mechanical behaviors of the interconnect technology during the bonding process. To undertake the process modeling, a process-dependent simulation methodology that integrates both thermal and nonlinear thermal-mechanical finite element (FE) analyses together with ANSYS® birth-death modeling technique is proposed. The validity of the process modeling is confirmed through various temperature and warpage measurements. Subsequently, the contact behaviors of the ACF joints under four-point bending and static bending tests are characterized through FE modeling. The simulated contact stresses are further correlated with the measured electrical resistance data using four-point probe method, by which the minimum threshold contact stress for achieving a reliable contact electrical performance is determined.

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1 Introduction

User experiences of electronic devices with high portability and flexibility, good intuitive human interfaces, high performance and low cost have pushed the development of novel and advanced manufacturing and packaging technologies toward flexible electronics. Flexibility and portability are generally associated with smaller, thinner, more rollable and lighter features. A great reduction of package's weight and a significant increase of stretchability and bendability are critically indispensable to meet the challenges. Over the years, most research and development activities for portable electronics have been placed on rigid silicon chips and substrates [Chen, Lin and Chiang (2005); Cheng, Yu and Chen (2005); Lin, Kung, Chen and Liang (2006); Cheng, Chen and Cheng (2008); Cheng, Tsai, Chen and Fang (2010)]. To extend electronics devices beyond the rigid form factor, flexible electronics have been extensively proposed and developed in recent years. It is highly recognized that the technology would bring a very vigorous drive toward the new flourish of economic growth in the electronics industry. The key application area of the technology include flexible display, paper-thin smart labels, particularly the RFID labels, miniaturized medical electronic systems, E-paper, E-label and memory chip stacking etc. Typically, flexible electronics can be achieved through the use of roll-to-roll (R2R) printing technologies. In fact, the emergence of the technologies might change the paradigm of fabrication of microelectronics circuits that have been being carried out through standard CMOS processing for years. However, key foreseeable issues facing the technologies need to be addressed, including high cost, low quality or accuracy, and limited yield, reliability and feasibility, mainly due to the lack of low-cost, high-resolution and high-speed ink-jet printing solution. Thus, a feasible alternative highly compatible to the current standard semiconductor fabrication and packaging process is of great demand and preference.

One of the most straightforward solutions for achieving flexible electronics through standard CMOS process is the so-called adhesive-based flexible interconnect technology [Chen, Zenner, Arneson and Mountain (1999); Marguet, Rozycki and Gornet (2006); Hoehla, Garner, Hohmann, Kuhls, Li, Schindler and Fruehauf (2011)]. The technology integrates three key flexible components: an IC chip, a flexible substrate that can be made of epoxy [Hoehla, Garner, Hohmann, Kuhls, Li, Schindler and Fruehauf (2011) or glass [Jokinen and Ristolainen (2002); Gaskell, Lee and Thompson (2010)] and a conductive/nonconductive adhesive [Cheng, Ho, Chi-

ang and Chang (2004); Cheng, Ho, Chen and Yang (2006); Cheng, Hwang, Kao, Tsang, Yang, An and Chang (2009)], such as anisotropic conductive film/adhesive (ACF/A), which makes the entire electronic assembly very flexible and thin. The I/O interconnection between the thin chip and flexible substrate is formed through flip chip thermal-compression bonding process using a conductive/nonconductive adhesive. Some obvious, compelling features, such as simple and flexible in structure, reworkable, low-cost, portable, indestructible and most importantly, compatible to the current standard semiconductor fabrication and microelectronics packaging process, make them great potential for next-generation ultra-thin and flexible applications. Thus, the technology attracts a great deal of worldwide research attention and interest.

Despite of its great advantageous characteristics, many significant technical challenges need to be solved prior to their industrial applications. For example, the technology may be subject to extreme environmental loading during bonding process and thermal-mechanical testing. This would potentially lead to high stress situation in the components because of the mismatch of temperature and thermal expansion coefficient (CTE) of bonded materials. High stresses together with a poor bond-line design tend to result in mechanical failures, such as adhesive delamination due to an excessive peeling stress, and the loss of electrical contact at the adhesive joints as a result of an insufficient contact stress on the bumps and mating electrodes, thereby leading to a great concern on yield and reliability. Typically, these failures can be correlated to the resulted thermal-mechanical behaviors developed during the bonding process or environmental testing. Accordingly, having a clear and thorough comprehension of these behaviors is of great importance for successful realization of the technology. An adequate mechanical design can help alleviate the level of the process- and testing-induced thermal-mechanical stresses and strains, and thus, eventually ends up with better mechanical reliability.

In the study, an ACF-based thin-flip-chip-on-flex (TFCOF) interconnect technology is first introduced (Fig. 1), together with its associated fabrication processes, including the wafer thinning process, plasma etching process and wafer cutting process. Subsequently, the process- and testing-induced thermal-mechanical behaviors of the interconnect technology during the ACF bonding process (Fig. 2) are investigated through numerical simulation using a process-dependent finite element (FE) simulation methodology and experimental validation using a micro-thermocouple technique for temperature measurement, a precision micro-figure measurement instrument (MFMI) and a laser scanner technique for warpage measurement, and four-point probe technique for electrical resistance measurement. Furthermore, the contact behaviors of the ACF joints under static bending (SB) (Fig. 3(a)) and four-point bending (FPB) (Fig. 3(b)) tests are characterized through FE modeling and

four-point probe method. The calculated contact stresses are correlated with the measured electrical resistance data to determine the minimum threshold contact stress for achieving a reliable contact electrical performance.

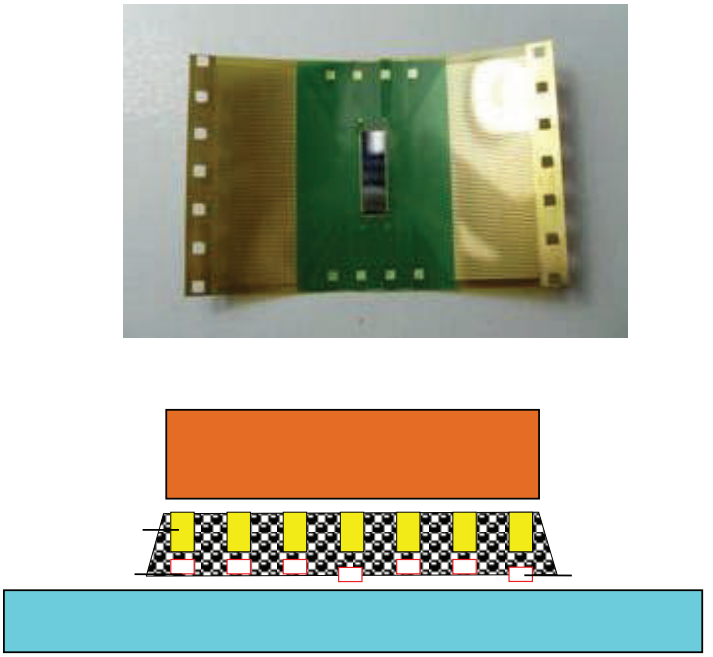
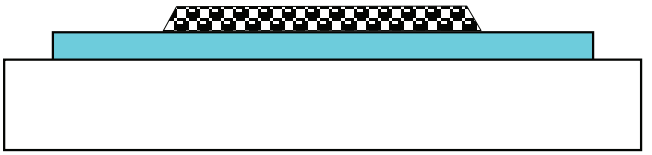


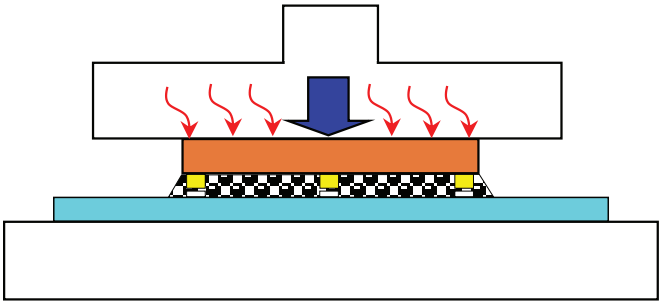
Figure 1: The TFCOF interconnect technology with ACF joints

2 The TFCOF Technology

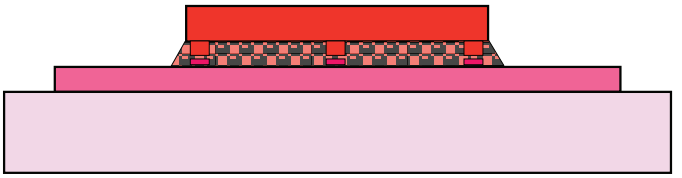
Figure 1 shows a prototype of the TFCOF technology and its cross-sectional schematic. The technology comprises three major components: an ultra-thin silicon IC chip with micro-bumps, a piece of polymer film for adhesion and an ultra-thin flexible circuit polymer substrate with electrodes. The adhesion film applied is an ACF [Cheng, Chen and Cheng (2008); Cheng, Tsai, Chen and Fang (2010); Hoehla, Garner, Hohmann, Kuhls, Li, Schindler and Fruehauf (2011); Marguet, Rozycki and Gornet (2006); Chen, Zenner, Arneson and Mountain (1999); Jokinen and Ristolainen (2002); Gaskell, Lee and Thompson (2010); Cheng, Ho, Chiang and Chang (2004); Cheng, Ho, Chen and Yang (2006)], which is a composite material made of an adhesive polymer resin and a great number of minuscule metal-coated polymer particles for electrical and signal interconnection. The ACF serves as mechanical



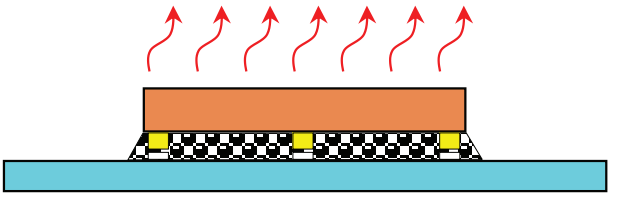
(a) Placement of an ACF on PI substrate



(b) Thermal-compression process

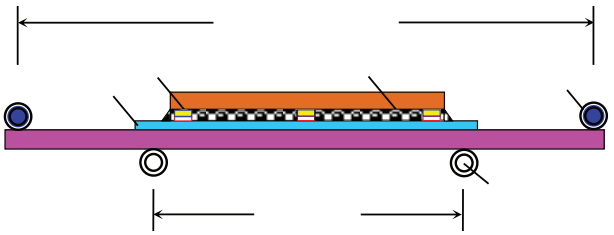


(c) Release of the compression pressure

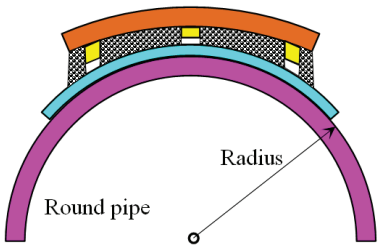


(d) Cooling of the technology to room temperature

Figure 2: The ACF bonding process



(a) Four point bending test (FPB)



(b) Static bending test (SB)

Figure 3: A schematic plot of the bending test setups

bonding of the thin silicon chip and the thin flexible substrate based on its adhesion strength. More importantly, a substantial contraction force of the ACF during its hardening and cooling process together with an applied external force can develop a reliable pressure contact between the micro-bumps of the silicon chip and the indium tin oxide (ITO) electrodes of the substrate to form the so-called ACF joints. The electrical connection between the thin silicon chip and the thin flexible substrate can be accomplished through the ACF joints. The micro-bumps and the mating electrodes, which form the ACF joints, are not fully bonded; as a result, the technology provides more compliant I/O interconnects.

The interconnect technology comprises a rectangular die with size of $10.86\times3\times 0.05$ (length$\times$width$\times$height) (mm^3) and 316 I/Os (ACF joints) with a pitch of 80 μm. The micro-bumps on the chip are made of Au alloy, the dimension of which is $120\times40\times10$ (μm^3). The flexible circuited substrate is made of polyimide (PI) and has a dimension of $48.175 \times 33.25 \times 0.035$ (mm^3). Besides, the electrodes on the flexible substrate are 10 μm thick, and are made of copper (Cu) coated by 1 μm thick nickel (Ni)/gold (Au) alloy. The top surface of the flexible substrate is deposited with an 8 μm thick Cu lead and a 3 μm thick electroplating Ni/Au layer. The ACF is a thermoset type of adhesive, in which chemical bonds are formed

during curing stage. Basically, the technology can be not only very thin but also extremely flexible due to the employment of an ultra-thin silicon chip, ACF joints and PI substrate.

Wafer bumping process is used to fabricate the micro-bumps on a wafer using standard electroplating process soon after the wafer is made by a semiconductor wafer fabrication house. For the wafer thinning, a two-step grinding process is introduced, which is a coarse grinding followed by a fine grinding, in which a standard wafer of 680 μm thick is first ground to around 75 μm thick using a coarse grinding process, followed by 20 μm thick removal using a fine grinding process. At last, the fine ground wafer is further thinned down to 50 μm using a plasma etching process. As soon as the wafer is thinned down to the targeted dimension, wafer cutting process using dicing by grinding (DBG) technique is performed. According to Ref. [Chen, Zenner, Arneson and Mountain (1999)], the mechanical strength of diced chips can be upgraded by as much as 15% using the DBG technique due to less chipping effect.

A schematic plot of the manufacturing procedure of the ACF bonding process is shown in Fig. 2. First, a piece of ACF adhesive is placed on the PI substrate prior to assembling (Fig. 2(a)). Next, the silicon chip is flipped, and then precisely aligned and pressed onto the PI substrate through the bonding head of a main bonder. As soon as an external bonding load is applied on the top side of the chip, thermal loading is also imposed on the assembly through the bonding head to thermoset the adhesive (Fig. 2(b)). Note that the required curing time is strongly dependent on the magnitude of thermal loading and also the chemical properties of the adhesive. Once the adhesive is fully cured, it becomes a key structural element and provides structural integrity of the interconnect technology. After that, the pressing force is released (Fig. 2(c)), and the assembly is cooled down to room temperature (Fig. 2(d)). In the present thermal-compression ACF bonding process, the imposed bonding force is 15 kgw and the applied thermal load for ACF curing is 180 °C with a heat curing duration of 30 seconds. It should be noted that the steel handling platform of the main bonder is preheated to 60 °C prior to the main bonding process.

3 Process Modeling

To facilitate the process modeling so as to characterize the process-induced thermal-mechanical behaviors of the TFCOF interconnect technology during the thermal-compression bonding process, a process-dependent FE simulation methodology [12-15] is proposed. The methodology integrates the three-dimensional (3D) FE approximations and the ANSYS death-birth technique [ANSYS user's manual Inc.]. The bonding process simulation involves both thermal and thermal-mechanical FE

analyses (Fig. 2). In addition, in the process modeling, all the major ACF bonding steps as described in the last section are considered, except the curing process of the ACP. It is neglected primarily due to that the contraction stress of the ACF during hardening is comparatively, insignificant because of its extremely low modulus. This was experimentally confirmed by Ref. [Cheng, Hwang, Kao, Tsang, Yang, An and Chang (2009)] that the contraction stress during the ACF bonding process is primarily attributed to the cooling process at temperature below the glass transition temperature T_g.

According to the ACF bonding process aforementioned, the process modeling can be categorized into four major modeling steps, which involve four static nonlinear thermal-mechanical FE models and one transient thermal FE model. The first modeling step is to simulate the thermal-compression process of the main bonder, by which both thermal and mechanical loads are imposed on the electronic assembly. More specifically, one transient thermal FE modeling for calculating the temperature distribution of the electronic assembly during the thermal curing of the ACF and one nonlinear thermal-mechanical FE modeling for simulating the corresponding thermal-mechanical behaviors are considered in the step. The calculated temperature at the end of the curing process is considered as an essential boundary condition of the thermal-mechanical FE modeling. The FE model at the process simulation step would not include the ACF component since it is not cured yet. Thus, at the step, it is temporarily deactivated from the FE model. At the second modeling step, the ACF is fully cured; as a result, the FE model of the component is reactivated. The third modeling step is to simulate the thermal-mechanical behaviors of the assembly when the imposed compression loading is released. At the modeling step, the FE model of the steel handling platform is deactivated since there is no need to take it into account in the FE modeling. At the last process simulation step, which is to model the cooling process of the assembly, the same FE model used in the third process simulation step is applied. It should be noted that in the process modeling, the contact behaviors between the micro-bumps and the mating electrodes and between the flex substrate and the steel handling platform of the main bonder are carried by solid-to-solid contact element.

3.1 Transient thermal FE modeling

3D transient thermal FE modeling is applied to simulate the temperature distribution of the TFCOF technology during the ACF curing process. The thermal FE model includes all the main components of the interconnect technology, such as the chip, ACF, PI substrate, micro joints, and also part of the steel handling platform of the main bonder. The transient thermal analysis accounts for natural convection, radiation, and conduction heat transfer. To achieve the goal, heat conduction FE

analysis can be effective for characterizing the thermal performance of an object if the surface temperature or heat transfer coefficient is known. For describing the heat dissipation from the surfaces of the interconnect technology to the external environment, many heat transfer coefficient correlation models are available based on either an isothermal or an isoflux assumption. In this investigation, the convective heat transfer coefficient correlation model h_c suggested by Ellison [Ellison (1989)] is used for describing surface natural convection, and the standard radiative heat transfer coefficient model h_r [see, e.g., Chen, Cheng and Shen (2003); Ridsdale, Joiner, Bigler and Torres (1996)] for describing surface radiation. They are, respectively, expressed as follows:

$$h_c = 0.83f\left(\left(T_w - T_a\right)/L_{ch}\right)^n, \tag{1}$$

$$h_r = Bge\left(T_w^2 + T_a^2\right)\left(T_w + T_a\right), \tag{2}$$

Table 1: Parameters of convective heat transfer coefficient correlation model

	L_{ch}	f	n
A horizontal plate facing upward	L×W/2(L+W)	1.0	0.33
A horizontal plate facing downward	L×W/2(L+W)	0.5	0.33
A vertical plate	Thickness	1.22	0.35
L: Length, W: Width			

where T_w is the surface temperature of the interconnect technology, T_a the ambient temperature, T_{ch} the characteristic length, f and n constants, which are listed in Table 1, B the Stephen-Boltzmann constant equivalent to 5.678×10^{-8} (Watt/m^{2}K^4), e the surface emissivity ($0 < e < 1$), and g the radiative view factor ($0 < g < 1$). Combining Eq. (1) and (2) yields the effective heat transfer coefficient h^T for describing the total surface heat transfer in a natural convection environment:

$$h^T = h_c + h_r, \tag{3}$$

It has be well confirmed that the approach is not only effective but also particularly efficient for subsequent parametric thermal design [Chen, Cheng and Shen (2003); Cheng, Chen and Cheng (2008)]

Note that the ACF layer entrapped in the bump-electrode interface is neglected from the thermal FE modeling due to its inconsiderable thickness (less than 3 μm). Since the size of the bonding head of the main bonder applied is larger than that of the chip, the air layer trapped between the bonding head and PI substrate is also considered in the modeling. Because of its extremely trivial thickness (less than 0.01

μm), heat transfer in the region is modeled by heat conduction, where a typical air thermal conductivity 0.03 (Watt/mK) is applied. Furthermore, as can be seen in Fig. 1, a layer of complex copper trace appears on the top side of the flexible substrate. Since the flexible substrate can serve as a major heat dissipation passage from the heat source to the ambient, detailed modeling of it is essential. However, detailed 3D modeling would be very difficult and time-consuming due to its complicated geometry and poor aspect ratio, and also computationally expensive because of a large mesh size. Thus, an effective approach using a rule-of-mixture technique is employed to perform thermal and thermal-mechanical modeling of the copper traces. In the thermal investigation, two thermal FE models are carried out. The first one is the TFCOF model shown in Fig. 1, and the other is the TFCOF test vehicle used for in-situ temperature measurement experiment, in which, as can be seen in the temperature measurement setup shown in Fig. 4, three micro-thermocouple wires are placed at a different location of the test vehicle. The details of the micro-thermocouple temperature measurement are briefed in the following sections. It should be noted that when the micro-thermocouple with a thickness of 105 μm is inserted in the interface between the chip and flexible substrate for temperature measurement, the micro-bumps would not make a contact with the associated mating electrodes. Likewise, the flexible substrate would be also impossible to contact the steel handling platform when there is an inserted micro-thermocouple between them. In addition, the width of the micro-thermocouple wires is as large as 3700 μm, thermal conductance through the wires could not be neglected. It is thus essential to develop a corresponding thermal FE model for the scenario. The thermal properties, including specific heat and thermal conductivity, are listed in Table 2 Due to symmetry, only a quadrant of the TFCOF technology and the steel handling platform is considered in the modeling with adiabatic boundary conditions defined on the symmetric planes.

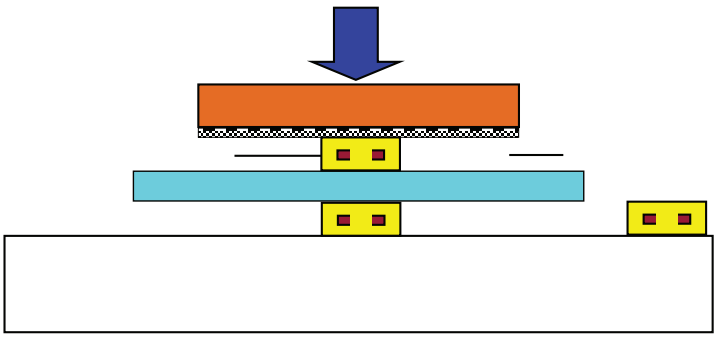


Figure 4: Temperature measurement setup

Table 2: The mechanical properties of the TFCOF interconnect technology

	E (GPa)	ν	κ (Watt/mK)	CTE (ppm/°C)	C_P (J/kg°C)
Silicon die	131.7	0.3	150	2.7	830
Au bump	Table 3	0.42	298	15	132.3
Cu trace	Table 3	0.34	402	16.7	390
PI substrate	9.6	0.3	1.475	14	1080
Steel platform	460	0.3	60	11.7	470
ACF	Table 4	0.2	1.045	Table 5	710

3.2 Thermal-mechanical FE modeling

There are two main sources of the contact forces at the ACF joints during the thermal-compression bonding process: 1) the imposed external pressure, and 2) the thermal contraction of the ACF. It should be noted that because of the weak material strength of the ACF resin during curing shrinkage, the mechanical stresses induced from the curing related volume shrinkage (or contraction) can be neglected [Cheng, Chen and Cheng (2008)]. The contact pressure at the contact interface is averaged in a volume-weighted manner [Cheng, Chiang, Chen and Lin (2001)]. Unlike the transient thermal FE model, the air trapped between the bonding head and flexible substrate is not taken into consideration in all the four thermal-mechanical FE models. All the materials of the interconnect technology are considered linearly elastic, as shown in Table 2, except the Cu electrodes and Au micro-bumps, which are assumed elastoplastic, as shown in Table 3. The ACF is assumed a temperature-dependent material, and the corresponding temperature-dependent CTE and Young's modulus are presented in Table 4 and 5, respectively. Also because of symmetry, only a quadrant of the TFCOF technology and steel handling platform of the main bonder are considered in the FE models. On the symmetry planes of the FE models, symmetry boundary condition is imposed. Figure 5 shows an example of the 3D thermal-mechanical FE model.

Table 3: The elastoplastic models of Cu and Au alloy (bilinear model)

Materials	E (GPa)	Yield stress (MPa)	Tangent modulus (MPa)
Cu	117	200	170
Au	77.2	110	900

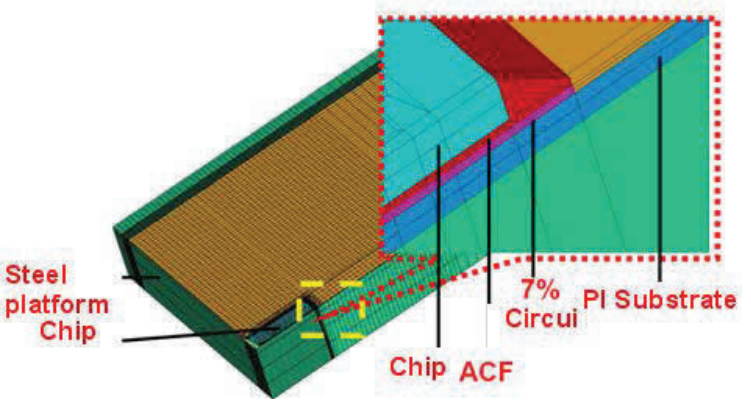


Figure 5: 3D thermal-mechanical FE model

Figure 6: Universal Materials Testing (5542)

Table 4: Temperature-dependent Young's modulus of the ACF

Temperature (°C)	21	115	135	300
E (GPa)	1.7	0.85	0.06	0.05

Table 5: Temperature-dependent CTE of the ACF

Glass transition temperature (T_g)(°C)	CTE before T_g (ppm/°C)	CTE after T_g (ppm/°C)
117	77	337.8

3.3 Thermal-mechanical FE modeling for SB and FPB test

After the process simulation, static bending (SB) and four-point bending (FPB) tests at room temperature are subsequently carried out using FE modeling and four-point probe electrical resistance measurement. The focuses of the investigation are placed on the contact performance at the ACF joints and the peeling stress at the ACF/chip interface. Since the TFCOF technology has a very weak bending rigidity, it is not feasible to directly undergo a FPB test. To ease the difficulties, the TFCOF specimen is attached onto an acrylic plate with a dimension of $80\times40\times2$ (mm^3). A schematic plot of the FPB test setup is shown in Fig. 3(a), where the curvature of the assembly (i.e., concave up/down) is controlled through an enforced displacement (upward/downward) by the indenters. The radius of curvature considered ranges from 0 to 5.5 mm. Note that the FPB test is done by a universal materials testing instrument. Furthermore, the SB test setup is schematically shown in Fig. 3(b), where the TFCOF technology is attached to a round pipe with a radius in the range of 25 mm to infinity (i.e., no curvature) for 100 hours. Due to symmetry, only a quadrant of the TFCOF assembly (i.e., the TFCOF technology bonded onto an acrylic plate) is considered in the FE modeling. It should be noted that the process-induced residual behaviors of the assembly after the ACF bonding process are also included in the calculation.

4 Experimental Validation

Four different experimental works are made to validate the proposed thermal and thermal-mechanical FE simulations. The first one is temperature measurement using a micro-thermocouple technique. Three T-type micro-thermocouples with a measurable range -200$\sim$400 °C are, respectively, inserted at the interfaces between the chip and substrate (i.e., reference point "1" in Fig. 4) and between the substrate and steel handling platform (i.e., reference point "2"), and also placed about 3$\sim$5 mm from the edge of the flexible substrate (i.e., reference point "3") on the top surface of the steel handling platform. A schematic plot of the measurement setup is presented in Fig. 4. The micro-thermocouples are connected to a computer-based, automated data recording system for in-situ temperature measurement. The test

specimen embedded with thermocouples is then placed on the steel platform for thermal-compression bonding. In the meantime, the temperature is also recorded using the thermocouple measurement system. Besides the aforementioned mechanical loading (i.e., 15 kgw), a two-step thermal bonding process is also applied, in which it is first preheated to 60 °C, followed by heating up to 234 °C with a 15 second duration. The second-step heating process is unlike that used in the present thermal-compression bonding process, i.e., 180 °C and a 30 second duration. The second and third experimental works are the out-of-pane deformation (warpage) measurement of the interconnect technology subjected to an isothermal swing loading soon after the ACF bonding process is completed. For facilitating the measurements, a precision micro-figure measuring instrument (ET-3000) (briefly termed MFMI) (Fig. 7) is applied to determine the warpage of the silicon chip, and a laser scanner is used to identify that of the substrate.

Figure 7: Micro figure Measuring Instrument (ET-3000)

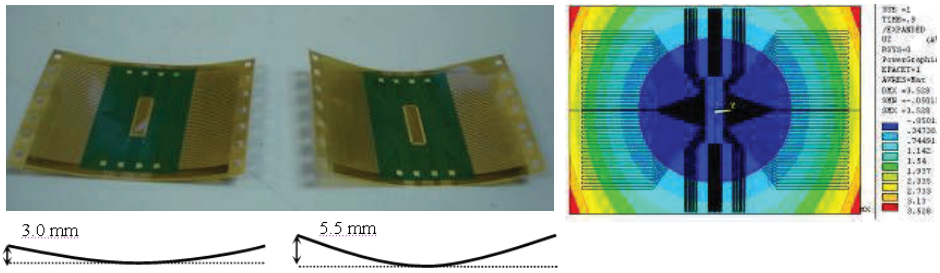
It should be noted that before the external compressive load reaches a threshold level, an increasing contact force would result in a less contact resistance [Gaskell, Lee and Thompson (2010)], and hence better electrical connection at the ACF joints. To date, directly assessing the contact stress through experiments still presents a great challenge. Thus, the last experiment is conducted for assessing the contact performance of the ACF joints under the SB and FPB test. It is an electrical

resistance measurement using four-point probe method together with an equivalent circuit.

5 Results and Discussions

5.1 Validation of the thermal-mechanical FE modeling of the flexible substrate

The validity of the proposed FE modeling for the flexible substrate is first demonstrated through warpage measurement using a laser scanner technique. The test specimen (i.e., a piece of a flexible substrate, as shown in Fig. 8) is subjected to an isothermal temperature swing of 165 °C (i.e., temperature elevation from 25 to 190 °C). The initial and final configurations of the flexible substrate under the isothermal loading are shown in Fig. 8(a) and 8(b). As can be seen in Fig. 8(a), the flexible substrate comprises a considerable, initial out-of-plane deformation, which can be as much as about 3.0 mm. By the isothermal loading, the flexible substrate is further deformed to about 5.5 mm. The net deformation as a result of the isothermal loading is about 2.5 mm. The out-of-plane deformations of the flexible substrate are also calculated using FE modeling, and the results are shown in Fig. 8(c). The modeled warpage of the substrate is about 2.53 mm. It should be noted that the FE modeling did not account for the initial residual warpage, suggesting that the modeled result is nothing but the warpage strictly induced by the isothermal loading. By comparing the modeled result with the experimental, the difference is only about 1.2%.



(a) 25 °C (b) 190 °C (c) Modeled warpage

Figure 8: Measured/modeled substrate's warpage under a temperature swing

5.2 Validation of the bonding temperature

The temperatures at those three reference points to which the thermocouples are attached are in situ characterized by using the thermocouple technique. It should be particular to note that because of the thermocouples, the TFCOF test specimen for the temperature measurement contains no ACF. The measured and modeled temperature at these three reference points are shown in Fig. 9, as a function time. It shows that due to preheating, the initial temperatures at these three reference points are all 60 °C. Furthermore, after about 1∼3 second heating, the temperatures at these reference points would all reach a steady-state temperature. It is also clear to see that except the transient period, the modeled temperature follows closely with the measured one nearly throughout the heating duration. In addition, the temperature at the first reference point, i.e., at the chip-substrate interface, is much larger than that of the other two reference points, indicating that there is a significant temperature gradient across the interconnect technology. The measured steady-state temperature at time t=15 seconds is 234.5 °C at the reference point "1", 186.1 °C at the reference point "2", and 119.8 °C at the reference point "3", while the corresponding modeled results are 232.2, 172.1 and 112.9 °C. The differences between them are about 0.98%, 7.5% and 5.7%, respectively. The insignificant amount of differences between the modeled and measured temperatures suggests the effectiveness of the proposed thermal FE modeling.

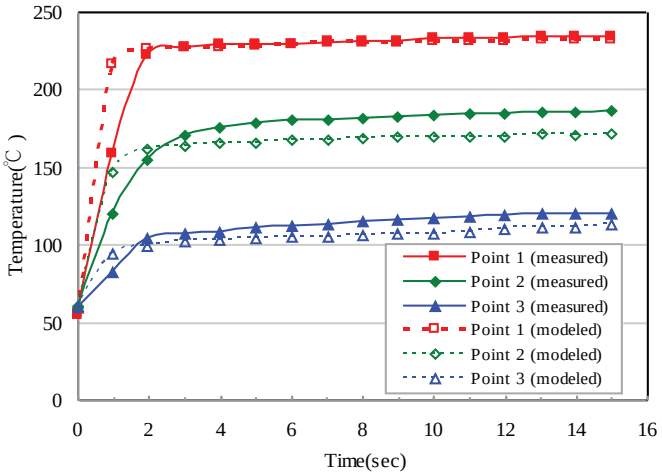


Figure 9: The modeled and measured temperature histories at the three reference points

5.3 Thermal-mechanical behaviors of the TFCOF technology after the bonding process

The process-induced warpage of the chip along the longitudinal symmetry plane is shown in Fig. 10, associated with the aforementioned four process simulation steps. The first two process simulation steps are to, respectively, simulate the thermal-compression loading process and the mechanical action of the ACF material after being fully cured. The simulation results show that the warpage of the thin silicon chip is trivial due to the compression of the bonding head. As the compressive force is released (i.e., the third process simulation step), due to the mismatch of the temperature and CTE between the thin silicon chip and flexible substrate, the chip deforms in a concave shape. As the TFCOF technology is cooled down to the room temperature (i.e., the last process simulation step), the thin silicon chip ends up with a convex deformation mainly owing to that the flexible substrate has a larger CTE than the chip, thereby resulting in a larger contraction as the temperature decreases. From Fig. 10, it is clear to see that the maximum warpage of the thin silicon chip is happened at the third process simulation step rather than the last step. The process-induced residual warpage along the longitudinal symmetry plane of the thin silicon chip is plotted in Fig. 11 (i.e., "Simulation (w/o initial warpage)" in the figure). It is found that the maximum process-induced warpage is located at the chip edge and the value is about 16.70 μm. The measured warpage of the silicon chip along the longitudinal axis using the MFMI is also illustrated in Fig. 11 (i.e., "Experiment" in the figure) and the maximum warpage is about 22.13 μm. By comparing the modeled and measured maximum warpage, the difference can be as much as about 24.5%, and it could not be considered trivial. One of the possible main causes of the nontrivial difference can be that the simulation takes no account of the initial warpage of the thin silicon chip. The initial warpage of the thin silicon chip along the longitudinal axis is also measured by MFMI, and the result is also shown in Fig. 11 (i.e., "Initial warpage"). By simply adding the initial warpage to the above simulation data (i.e., "Simulation (w/o initial warpage)"), the result is presented in "Simulation (w/initial warpage)" of Fig. 11. The final maximum warpage of the thin silicon chip is increased from 16.7 to 20.11 μm, and the deviation from the experimental data can be greatly reduced down to 9.1%.

5.4 Contact/peeling stress under the FPB and SB test

Followed by the process modeling of the ACF bonding process, simulations of FPB and SB tests are also performed. In the FPB test, the TFCOF specimen is imposed with a 4 cm upward enforced displacement through the indenters, which makes the assembly bend downward or convexly, and in the SB test, the specimen is attached to a circular pipe with a radius of 30 cm. The calculated peeling stresses at the

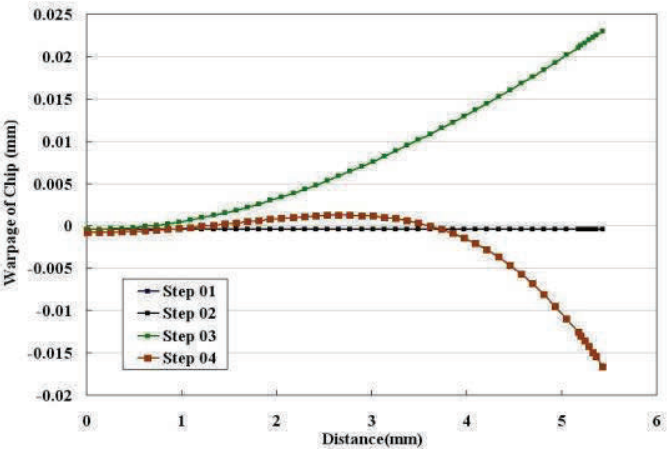


Figure 10: Process-induced warpage of the chip versus 4 simulation steps

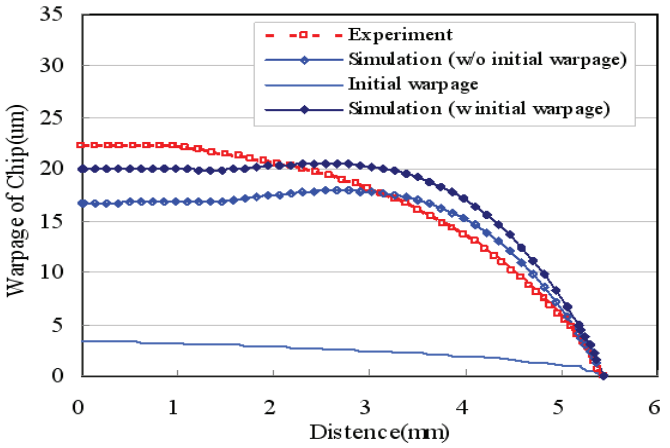


Figure 11: The modeled and measured warpage of the chip

specific finite element of the ACF component associated with these two bending tests can be also seen in Fig. 12. It is found that under the SB and FPB tests, the associated peeling stresses become more significant than the process-induced ones (i.e., the peeling stress at "Step 04").

The contact stresses at the ACF joints after the FPB and SB tests are presented in Fig. 13. A major surprise is that for the FPB test, the contact stress at the ACF joints that are closer to the symmetry planes tends to outperform those farther away from them. The result is totally opposite to that of the bonding process simulation (see

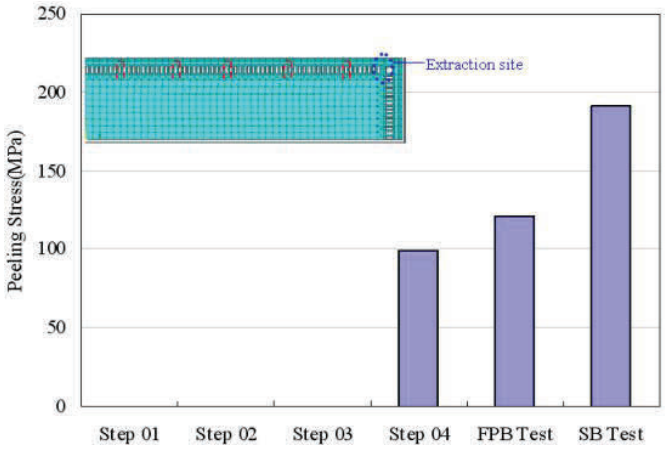


Figure 12: Peeling stresses of ACF versus 4 simulation steps and FPB and SB tests

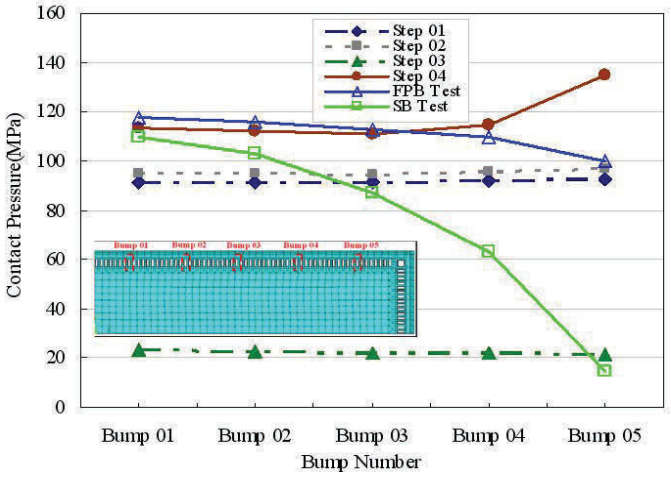


Figure 13: Contact stress of ACF joints versus 4 simulation steps and FPB and SB tests

the result of "Step 04"), in which the ACF joints farthest away from the symmetry planes would yield the maximum contact stress. This could be mainly attributed to that when the TFCOF assembly is subjected to an enforced displacement through the indenters of the FPB system, the PI substrate that is attached to the acrylic plate would deform in a convex shape. Since the bending rigidity of the PI substrate is weaker than that of the silicon chip, the silicon chip would deflect less than the substrate, as can be seen in Fig. 3. Accordingly, the cornered ACF joints would

have a less contact stress and so a larger electrical resistance than the central ones. On the other hand, as compared to the FPB test and process simulation, the SB test would hold a much smaller contact stress at the ACF joints, in particular the cornered joints, mainly due to that the resulting bending curvature or deflection of the deformed TFCOF assembly under the SB test is much larger than that of the FPB test.

5.5 Electrical performance at the ACF joints under the FPB and SB test

The contact electrical resistances at the ACF joints under the FPB test are measured by four-point probe method and the results are shown in Fig. 14, as a function of the deflection of the assembly. Results show that the measured contact electrical resistance would increase with an increasing deflection or bending curvature. However, as the deflection becomes larger than 5.5 μm, the contact resistance would decrease with deflection. This is mainly owing to that delamination takes place at the interface of the TFCOF assembly and thin acrylic plate. In other words, after the reflection point, the assembly gradually resumes its undeformed configuration due to the delamination. The FE modeling results are shown in Fig. 15. As can be seen in the figure, the contact stress or pressure at the cornered ACF joints drops significantly with an increasing deflection, suggesting that an increasing deflection would raise the contact electrical resistance at the ACF joints. The result trend is consistent with that of the measured contact electrical resistance before the onset of the delamination.

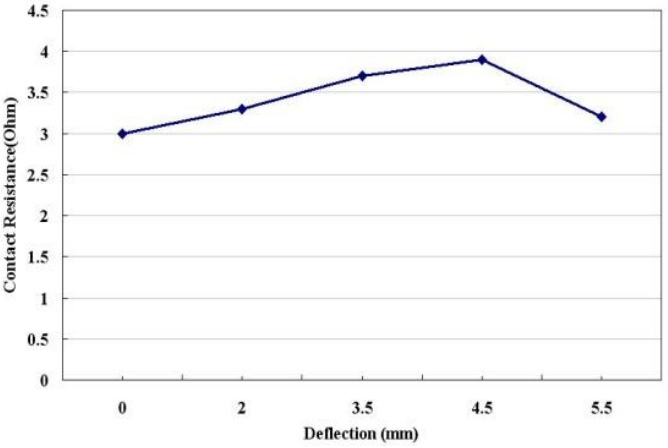


Figure 14: Measured contact electrical resistance versus deflection under FPB using four-point probe method

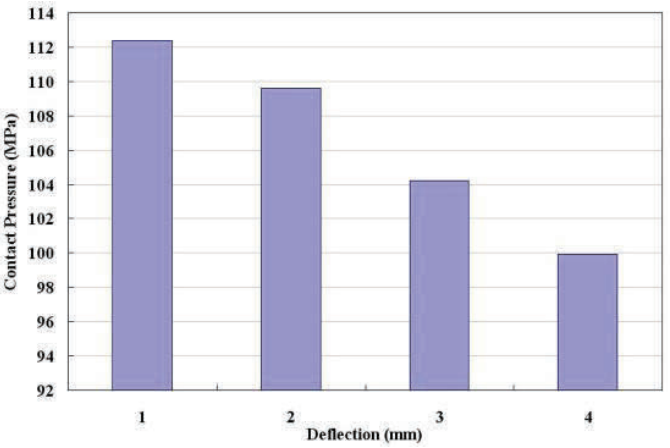


Figure 15: Modeled contact pressure versus deflection under FPB

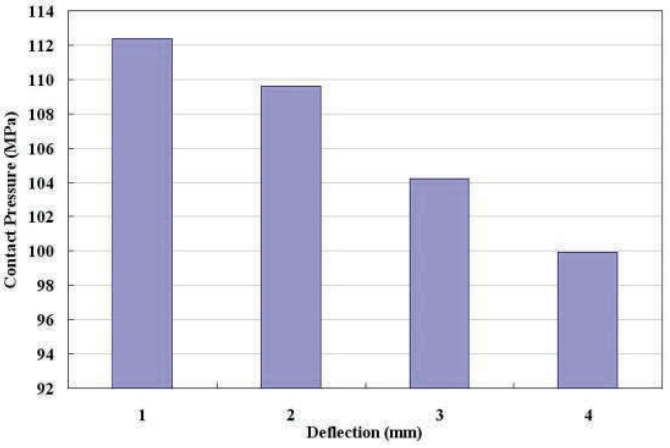


Figure 16: Measured contact electrical resistance versus bending curvature under SB using four-point probe method

The contact electrical resistance at the I/O interconnects can be an essential measure of the electrical performance and even the feasibility of electronic packages. It has been well addressed in previous literature reports [see, e.g., Cheng; Ho; Chiang and Chang (2004)] that for adhesive-based flip chip technologies, such as the TFCOF technology, the contact electrical resistance at the bonding line or I/O interconnects (such as ACF joints) would be strongly dependent on the contact stress before a critical bonding stress value is reached. It should be, however, noted that an excessive

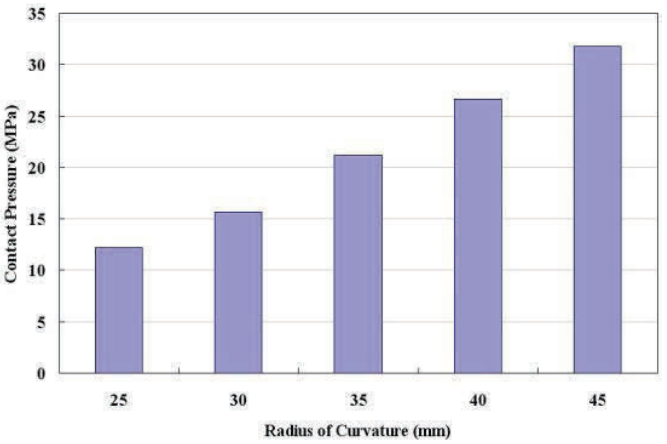


Figure 17: Modeled contact pressure versus bending curvature under SB

bonding stress may not only result in a significant peeling stress, thereby considerably increasing the risk of delamination in the adhesive, but also likely damage the metal-coated polymer particles and even the contacting electrodes. To maximize the contact or bonding stress at the ACF joints so as to provide a minimal contact resistance while still maintain or even reduce the corresponding peeling stress at the adhesive is a rather crucial issue. Accordingly, the critical bonding stress for the TFCOF technology is evaluated. The contact performance at the ACF joints of the TFCOF assembly under the SB test with a different radius of curvature is theoretically and experimentally assessed. The measured contact electrical resistance using four-point probe method is shown in Fig. 16, versus bending curvature. It is clear to see that the measured contact electrical resistance would reduce with a decreasing curvature or an increasing radius of curvature, and eventually reach a converged value as the radius of curvature becomes larger than 45 mm. This indicates that beyond the value, the contact resistance would somewhat be independent of the radius of curvature of the assembly or the contact stress of the ACF joints. Furthermore, Fig. 17 presents the calculated contact stresses using FE modeling as a function of the radius of curvature. Clearly, the modeled contact stress would increase with the increase of the radius of curvature. By correlating the measured contact electrical resistances with the calculated contact stresses, it turns out that the contact stress corresponding to the threshold value of the contact electrical resistance is about 32 MPa. This value is also regarded as the critical bonding stress for the TFCOF technology. Beyond the threshold value, the increase of the contact pressure or stress would no longer minimize the contact electrical resistance.

6 Conclusions

This paper introduces an advanced ACF-typed TFCOF technology for flexible electronics packaging. The thermal-mechanical behaviors of the interconnect technology during the ACF bonding process and also under the SB and FPB tests are extensively explored by virtue of the proposed process-dependent FE simulation methodology incorporating ANSYS birth-death modeling technique. The effectiveness of the process simulation is demonstrated through various experiment measurements. By correlating the simulated contact stresses with the measured electrical resistance data using four-point probe method, the minimum requirement in the contact stress for achieving a reliable contact electrical performance is determined.

Some essential concluding remarks are drawn as follows:

1. All the modeled results show a good agreement with the experimental data, suggesting that the proposed process-dependent FE simulation methodology can be very reliable and effective in predicting the process-induced thermal-mechanical behaviors during the ACF bonding process.

2. Even though the TFCOF assembly is preheated to 60°C by way of the steel handling platform prior to the main bonding process, there still exists a significant temperature gradient across the interconnect technology, which may result in a significant warpage and mechanical stress in the assembly.

3. A significant initial out-of-plane deformation of as much as about 3.0 *mm* is observed in the small thin PI substrate, which would have a considerable impact on the process-induced residual warpage of the TFCOF technology.

4. From the process simulation, it is found that after the ACF bonding process, an excessive residual warpage in the thin silicon chip and a considerable peeling stress in the ACF/chip interface can be observed. Further minimization of them is crucial to the success of the realization of the technology.

5. Substantial residual contact or bonding stresses are generated after the bonding process, demonstrating the feasibility of the interconnect technology for providing reliable electrical connection or contact between the PI substrate and chip.

6. The maximum process-induced warpage of the thin silicon chip is happened after the release of the compression load, instead of after the cooling of the assembly to room temperature or at the end of the ACF bonding process.

7. After the ACF bonding process, the cornered ACF joints would yield a larger contact stress than the central ones, leading to a better electrical performance.

On the other hand, for the SB and FPB tests, a totally opposite result is derived, in which the contact stress of the cornered joinyd under the SB test would dramatically drop to below 20 GPa.

8. From the SB and FPB tests, it is demonstrated that a larger bending curvature or deflection would lead to a more significant peeling stress at the ACF/chip interface while creating a lesser contact stress at the ACF joints, thereby resulting in a higher contact electrical resistance and thus increasing the risk of ACF delamination and open circuit failure.

9. Furthermore, the critical bonding stress at the ACF joints for the TFCOF technology is found to be about 32 MPa. A bonding stress larger than this threshold value would no longer provide a better electrical performance but may jeopardize the mechanical integrity or reliability of the bonding line.

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