Suppression of Ambipolar Conduction in Schottky Barrier Carbon Nanotube Field Effect Transistors: Modeling, Optimization Using Particle Swarm Intelligence, and Fabrication

P. Reena Monica[1, *] and V. T. Sreedevi[2]

Abstract: A mathematical model and experimental analysis of the impact of oxide thickness on the ambipolar conduction in Schottky Barrier Carbon Nanotubes (CNTs) Field Effect Transistor (SB CNTFETs) is presented. Suppression of ambipolar conduction in SB CNTFETs is imperative in order to establish them as the future of IC technology. The ambipolar nature of SB CNTFETs leads to a great amount of leakage current. Employing a gate oxide dielectric of thickness, $t_{ox} \sim 50$ nm suppresses the ambipolar behavior. In an SB CNTFET, it is the electric field at the source/drain contacts that control the conductance and the band bending length at the contacts is defined by t_{ox}. Therefore, t_{ox} is the prime parameter that influences the width of the Schottky barrier and the current in the subthreshold region. Due to the wide SB, there is a loss in on-current due to tunneling, but the current due to thermionic emission is increased by employing a high-κ dielectric such as Zirconium dioxide (ZrO_2). This work proposes an approach to suppress ambipolar behavior in SB CNTFETs without decreasing the on current. The thickness and dielectric constant of the gate oxide are optimized using the particle swarm optimization (PSO) algorithm to achieve suppression of ambipolar conduction without any loss in on-current. The proposed SB CNTFET was modeled using Verilog-A. Experimental demonstration of the suppression of ambipolar property is also presented. Two SB CNTFETs are fabricated using high-κ dielectric such as ZrO_2 with different thickness. A device with thin (~5 nm) gate oxide and another device with thick (~50 nm) gate oxide were fabricated. From the experimental results, it is observed that the device with the thin gate oxide exhibited ambipolar characteristics and the device with the thick gate oxide did not exhibit ambipolar characteristics. The increase in thickness, t_{ox}, ensures suppression of ambipolar behavior.

Keywords: Ambipolar conduction, Carbon nanotubes, high-κ gate oxide, Schottky barrier.

1 Introduction

The emerging trend towards Internet of Things (IoT) has increased the demand for scaled down low power devices with high performance [Atzori, Iera and Morabito (2010)]. The development in nanoelectronics with novel materials such as semiconducting carbon nanotubes (CNTs) addresses this need. CNTs exhibit excellent carrier mobility at

[1] School of Electronics Engineering, VIT Chennai, Vandalur-Kelambakkam Road, Chennai, 603103, India.

[2] School of Electrical Engineering, VIT Chennai, Vandalur-Kelambakkam Road, Chennai, 603103, India.

[*] Corresponding Author: P. Reena Monica. Email: reena.monica@vit.ac.in.

nanoscale [Dürkop, Getty, Cobas et al. (2004)]. They are capable of carrying high currents without scattering due to their ballistic electron transport [Zhang, Zhu, Wang et al. (2004)]. The Carbon Nanotube field effect transistors (CNTFETs) are in the limelight among all novel nanoelectronic devices for their promising device characteristics [Avouris, Appenzeller, Martel et al. (2003)]. The high-frequency characterization of CNTFETs up to 10 GHz was reported by Huo et al. [Huo, Zhang, Chan Philip et al. (2004)]. In the recent years, CNTFETs are found in the IoT space in gas sensing, CNT based antennas and in RF interconnects [Xuan, Thuy, Luyen et al. (2017); Chen, Zhang, Feng et al. (2008); Liu, Chen, Zhang et al. (2009); Bhatt, Vijay, Joshi et al. (2017); Taghavi, Carta, Meister et al. (2017); Bayat, Ramin and Kashani-Nia (2017); Li, Tianjian, Jing et al. (2018)]. CNTs have the potential to be used as the next-generation ultrasensitive gas sensors [Thai, Yang, DeJean et al. (2011)]. Despite all these credentials, there are certain hurdles which limit the usage of CNTFETs. This paper addresses one such hurdle, i.e., the ambipolar conduction which imposes a concern when the CNTFETs are stacked. Ambipolar behavior is not desirable as it increases the OFF state leakage current and degrades the performance of CNTFETs. The OFF current is due to the tunneling of holes through the Schottky Barrier (SB). Negative gate to source voltages will result in high leakage currents. A metal contacted CNTFET is preferred over a highly doped semiconductor contacted CNTFET because the metals have notably lower parasitic resistance [Javey and Kong (2009)]. This work focuses on the metal contacted Schottky Barrier CNTFET (SB CNTFET). Earlier, the only solution to make the device unipolar was to dope the contacts heavily [Javey and Kong (2009)]. Other effective ways of suppressing ambipolar behavior in SBCNTFET are demonstrated: Halo doping of the channel in CMOS technologies is one of the techniques to decrease short channel effects [Ieong, Narayanan, Singh et al. (2006); Hwang, Lee and Hwang (1996); Zanchetta, Todon, Abramo et al. (2002); Endoh and Momma (2007)]. This technique is used in CNTFETs to suppress ambipolar behavior. For some particular length of the CNT channel, p-type dopants are added. Since the source side of the channel is p-doped, it is screened from all variations in the drain potential. It has been demonstrated [Zahra and Orouji. (2009)] that the leakage current can be lowered by the halo doping technique. Another novel device, a linear doped channel (LDC) CNTFET is presented by Naderi et al. [Naderi, Keshavarzi and Orouji (2011)]. Instead of a halo doping on one end of the channel, the doping is linearly distributed throughout the channel with a maximum concentration at the source side decreasing linearly to zero as it goes to the drain side of the channel. The suppression of ambipolar behavior of CNTFETs can also be achieved by engineering the gate structure. A vertical partial gate where the gate covers only a part of the channel suppresses the ambipolar behavior [Yoon, Fodor and Guo (2008)]. The absence of gate at the drain side makes the SB thick at this side ensuring unipolar behavior. A deep trench introduced under the CNT near the source or drain contact can also create the same impact of the gate not controlling the channel. The trench area under the CNT is not controlled by the back gate [Lin, Appenzeller and Avouris (2004)]. Therefore the lack of control over that part of the channel makes the SB thick at the source/drain side, thus suppressing ambipolar behavior. All of these methods rely on sophisticated fabrication techniques. A much simpler solution is demonstrated by Guo et al. [Guo, Datta and Lundstrom (2004)]. The impact of gate oxide thickness and the role of nanotube diameter are studied. The study revealed that the CNTFETs with thin gate oxide (4 nm) exhibited ambipolar characteristics

[Guo, Datta and Lundstrom (2004)]. The thickness of the SB is approximately the thickness of the gate oxide [Odintsov (2000)]. The gate capacitance, C_{ox}, in long channel devices is inversely proportional to the logarithm of the oxide thickness, t_{ox}, due to the one dimensional nature of the CNTs. Aggressive scaling of t_{ox}, makes the Schottky barrier thin which enables tunneling through the barrier and ambipolar conduction. In silicon MOSFET, the charge in the channel is affected by t_{ox} through the gate capacitance and thus affecting the conductance in the ON state. However, in an SB CNTFET, it is the electric field at the source/drain contacts that controls the conductance and the band bending length at the contacts is defined by t_{ox}. Therefore, t_{ox} is the prime parameter that influences the width of the Schottky barrier and the current in the subthreshold region [Odintsov (2000)]. There are experimental results revealing the fact that CNTFETs with thin gate oxide has a tendency to be ambipolar with nearly symmetrical characteristics [Radosavljevic, Heinze, Tersoff et al. (2003)]. A back-gated SB CNTFET with 2 nm and 5 nm thick gate oxide exhibited ambipolar characteristics. When the gate insulator was thick (40 nm), an asymmetric barrier height led to asymmetric electron and hole conduction [Guo, Datta and Lundstrom (2004)]. Thus the ambipolar behavior is suppressed by having a thick gate dielectric.

Thus it is important to get optimal values of gate oxide thickness to suppress the ambipolar conduction. Particle swarm intelligence based optimization is carried out to get the optimal gate oxide thickness in order to suppress the ambipolar conduction.

The result of the optimization suggested thick gate dielectric of 50 nm. Therefore, in this work, in order to suppress the ambipolar behavior, gate dielectric of thickness ~50 nm is employed. However, the thick gate dielectric reduces the on current due to tunneling. In order to compensate this reduction in on current, a high-κ dielectric such as zirconium dioxide (ZrO_2) is used. Generally, high-κ dielectrics are used to reduce leakage current in scaled-down devices with thin gate oxides. The purpose of a high-κ dielectric in this work is to increase the conductance by thermionic emission. Thereby, the on-current is not affected. This proposed SB CNTFET is modeled and written in Verilog-A. In order to demonstrate the occurrence of ambipolar conduction in SB CNTFETs with CNTs as a channel and thin gate oxide, an SB CNTFET with $t_{ox} \approx 5$ nm was fabricated and characterized. Also, to demonstrate the suppression of ambipolar conduction in an SB CNTFET with thick gate oxide, an SB CNTFET with $t_{ox} \approx 50$ nm was fabricated and characterized. The results clearly indicate that the high-κ dielectric ensures better on-current when compared to the on-currents reported in the literature, where low-k dielectric such as SiO_2 is used [Javey, Guo, Wang et al. (2003)]. The increase in thickness, t_{ox}, ensures suppression of ambipolar behavior.

This paper is organized as follows: Section 2 presents the mathematical model of the proposed SB CNTFET and the optimization using particle swarm intelligence. Section 3 presents the fabrication procedure followed in this work. The results and inferences are discussed in Section 4. Section 5 concludes the paper.

2 The model

2.1 Modeling the SB CNTFET

An SB CNTFET with a single-walled CNT as the channel exhibits ambipolar behavior. In the SB CNTFET model shown in Fig. 1 [Javey and Kong. (2009)], when the source side

SB and the drain side SB are taken into account, the distribution functions as shown in Eq. (1) and Eq. (2) are derived.
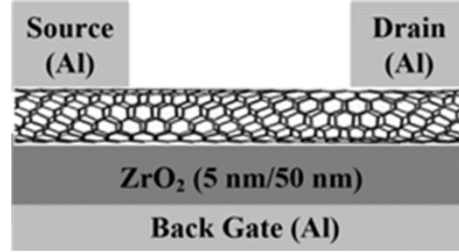

Figure 1: Cross-sectional view of SB CNTFET

$$f^+ = \frac{T_s f_s + T_d f_d - T_s T_d f_d}{1 - (T_s - 1).(T_d - 1)} \tag{1}$$

$$f^- = \frac{T_d f_d + T_s f_s - T_s T_d f_s}{1 - (T_s - 1).(T_d - 1)} \tag{2}$$

The ballistic current, I_d is calculated from the Landauer - Büttiker formula as in Eq. (3).

$$I_d = \frac{2q}{h} \sum_{k_l} \int_{E_{i\,min}}^{E_{i\,max}} (f^+(E,\mu) - f^-(E,\mu)) dE \tag{3}$$

The approach in John et al. [John, Castro, Pereira and Pulfrey (2004)], was followed for the self-consistent simulations of SB CNTFETs, solving Schrödinger equation as in Eq. (4),

$$-\frac{h^2}{2m^*}\frac{\partial^2 \varphi_s}{\partial x^2} + (U - \varepsilon)\varphi_s = 0 \tag{4}$$

where m^* is the effective mass and ε is the energy of a carrier's wave function, φ_s .

U is the local potential energy and is given for electron and holes as in Eq. (5) and Eq. (6)

$$U_e = -q\phi(x) - \chi_{cnt} \tag{5}$$

$$U_h = -U_e + \varepsilon_g \tag{6}$$

χ_{cnt} is the electron affinity.

$n_{s,d}$, the induced charge in the nanotube from the source and drain side is calculated from Eq. (7)

$$n_{s,d} = \frac{4}{2\pi} \int f_{s,d} |\varphi_{s,d}|^2 dk_{s,d}$$

$$= \int \frac{\sqrt{2m^*}}{\pi h \sqrt{\varepsilon_{s,d}}} f_{s,d} \left| \varphi_{s,d} \right|^2 d\varepsilon_{s,d} \tag{7}$$

The total carrier concentrations given as in Eq. (8)

$$n = n_s + n_d$$

$$p = p_s + p_d \tag{8}$$

are entered into the Poisson's equation as in Eq. (9)

$$\nabla \varepsilon \nabla \emptyset = - \frac{q(p-n)\delta(\rho - \rho_{CNT})}{2\pi\rho} \tag{9}$$

The δ here denotes the Dirac-delta function which describes the charge density of CNT. The electrons and holes are considered as charged sheets. We assume that the charges are uniformly distributed around the surface of the nanotube. The Poisson equation in Eq. (9) is solved with the Schrödinger equation in Eq. (4) self-consistently.

The model was written using Verilog-A in Cadence Virtuoso EDA tool. A symbol was created to be employed for circuit simulations. Fig. 2 shows the symbol of SB CNTFET. The model's functionality was verified in Cadence Virtuoso.
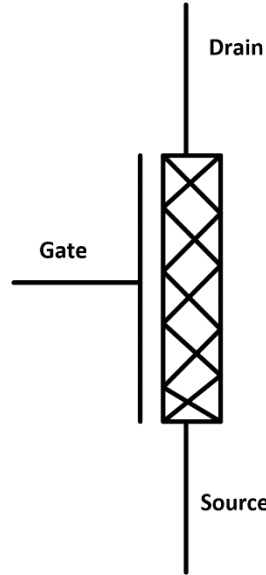

Figure 2: Symbol of the model in Cadence EDA tool

2.2 Optimization of the model using particle swarm optimization

A number of intelligent computing techniques, based on evolutionary computing and Swarm Intelligence (SI), are presented to solve various engineering applications. Particle Swarm Optimization (PSO) [Eberhart and Kennedy (1995)] have been proved to be efficient and is widely used. The major inspiration for all these methods stems from biological systems in nature. Some of the common characteristics of all these unconventional algorithms are that they are all population based, independent of

derivatives and have employed probabilistic approach. These algorithms start with a set of solutions (called a parent population) instead of one trial solution, and generate a new set of trial solution by carrying out proper transitions, which is unique for each algorithm, in a stochastic manner. Using heuristic optimization techniques, best results can be obtained for the parameters available to model CNTFET. There are various optimization techniques available to optimize the devices in nano scale region. The high OFF-state leakage current due to band-to-band tunneling (BTBT) under high reverse gate voltages is still a major issue in CNTFETs. Many researchers have tried to suppress leakage current caused by BTBT by varying the doping profile and asymmetry between source/drain regions.

In this work, we propose PSO based optimization method to suppress the ambipolar conduction. The main objective of the optimization process is to extract an optimal value of the thickness and dielectric constant of the gate oxide to achieve suppression of ambipolar conduction without any loss in on-current.

The ith particle $(1 \leq i \leq N, i \in Z)$ location is a viable solution in S and is represented as $\vec{x_i} = (x_{i1}, \ldots \ldots x_{id}, \ldots \ldots x_{iD})$ in particle swarm optimization. *pbest* represented as $\vec{p_i} = (p_{i1}, \ldots \ldots p_{id}, \ldots \ldots p_{iD})$ is the value of the ith particle's best fitness i.e., its best position. *gbest* represented as $\vec{g}$ or $\vec{p_g}$ is the best of pbest amongst all particles. The ith particle's velocity is given as $\vec{v_i} = (v_{i1}, \ldots \ldots v_{id}, \ldots \ldots v_{iD})$. With the acceleration constants c_1 and c_2, the inertia weight, the ith particle is handled by the Eq. (10) for every time step. $U_R()$ are some random values taken between 0 and 1.

$$v_{id} = w.v_{id} + c_1 U_R(\,).(p_{id} - x_{id}) + c_2.U_R(\,).(g_d - x_{id}) \qquad (10)$$

where $x_{id} = x_{id} + v_{id}$

The objective function is to maximize the I_{on}/I_{off} ratio which translates to suppression of ambipolar conduction. The parameters to be optimized are the gate oxide thickness and the dielectric constant.

In this work, the fitness function, f with M samples is taken as the ith particle's drain current mean squared error and is given as in Eq. (11).

$$f = \frac{1}{M}\sum_{V_{GS}}\sum_{V_{DS}}\left[\frac{I_{DS,Num} - I_{DS,PSO}}{I_{DS,Num}}\right]^2 \qquad (11)$$

The calculated drain current based on the computation of PSO is the predicted value $I_{DS,PSO}$. The targeted numerical function is given as $I_{DS,Num}$. The PSO parameters are shown in Tab. 1.

Table 1: PSO parameters

PSO Parameters	
Swarm size	20
Maximum number of generations	5000
c_1, c_2	1,1
Inertia weight, w	Random values
r_1 and r_2	Random values
Obtained fitness	$1.8*10^{-3}$
Computation time	2500 s

The steps of the PSO are shown in the flowchart in Fig. 3. Tab. 2 shows the optimized values of the thickness and gate dielectric constant for good I_{on}/I_{off} ratios. The thickness is found to be 50 nm and the dielectric constant is 25. Therefore, zirconium dioxide (ZrO_2) whose dielctric constant is close to 25 is chosen. With the extracted optimized values from PSO, the SB CNTFET with 50 nm ZrO_2 dielectric was fabricated and is presented n the next section.
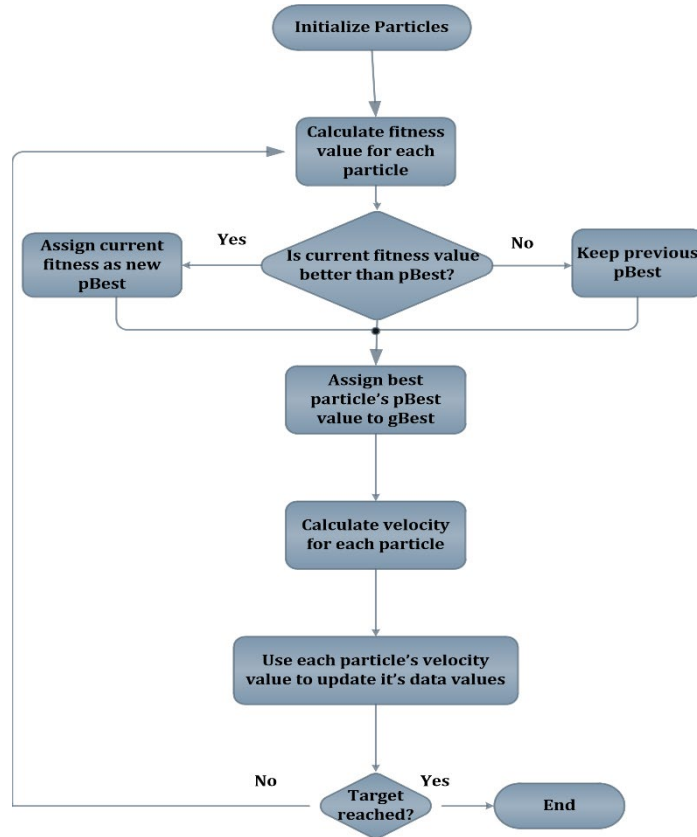

Figure 3: Flowchart of PSO

Table 2: Optimized parameters

Quantity	Optimized values
Gate oxide thickness, t_{ox}	50 nm
Gate dielectric constant, ε	25 (ZrO_2)
Off current, I_{off}	10^{-18} A
On current, I_{on}	10^{-6} A

3 Fabrication of SB CNTFET

Fig. 1 shows the structure of the SB CNTFET. Two devices were fabricated. One device was fabricated with thin gate oxide, ZrO_2 (~5 nm) and the other device was fabricated with thick gate oxide, ZrO_2 (~ 50 nm). The methodology for fabrication is as follows and is shown in Fig. 4: On one side of a double side polished silicon wafer of 350 μm thickness, ZrO_2 was deposited by E-beam physical vapor deposition (EBPVD) method. The thickness was measured to be ~5 nm for the first device and ~50 nm for the second device. The back side of the silicon wafer was coated with aluminum for the back gate electrode for both the devices.
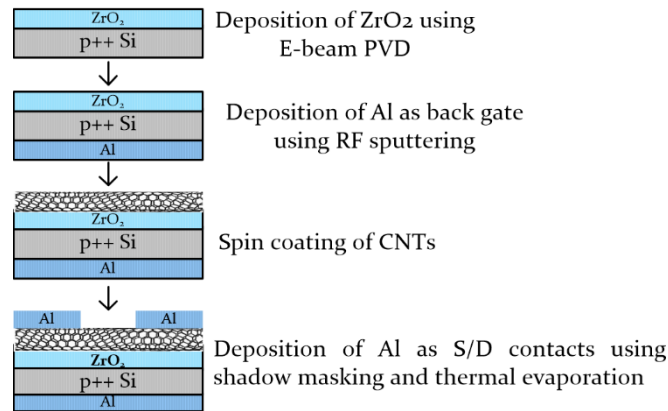

Figure 4: Fabrication steps of the back gated SB CNTFET

The CNTs were spin coated over the dielectric layer to form a thin film of CNTs on both the devices. Deposition of CNTs by dispersing them in a solvent and spin coating is an excellent method to form a thin film of CNTs. The obvious advantages being the simplicity of the procedure, it's speed and to top it all it can be performed at room temperature. This process of dispersing CNTs and spin coating them, in due course, will enable large-scale fabrication of CNTFETs. The CNTs were bought in powdered form from Amorphous and Nanostructure Ltd., USA. The SWCNTs are semiconducting and are 5-30 μm long with a purity of 95% CNTs and 90% SWCNTs. The outside diameter is measured as 1-2 nm and the inside diameter is 0.8-1.6 nm. The material characterization results showing that the SWCNTs are semiconducting can be found in http://www.nanoamor.com/inc/sdetail/9539.

For Spin coating, the CNTs were dispersed in a solvent Triton X 100. Triton X 100 gives better dispersion as well as good viscosity [Santagata, Baglieri and Tsantilis (2015)]. It is 5% in aqueous solution. 5mg of CNT was mixed with 1% of Triton X 100. The amount of Triton X required for 20 ml solution was calculated as follows:

Amount of Triton X 100 (N_0) in aqueous solution=5%. The required total percentage (N_1) of Triton X 100 is 1%. Total volume of solution (V_1)=20 ml.

Total volume of Triton X 100 required (V_0) was calculated to be 4 ml using the relation in Eq. (12)

$$N_0 V_0 = N_1 V_1 \tag{12}$$

Therefore, 4 ml of Triton X 100 was added with 16 ml of pure distilled water. 5 mg of CNTs were added to this mixture and was dispersed by sonication. The dispersion was carried out using a tip sonicator. The time taken for proper dispersion of CNT was calculated using Eq. (13)

$$E = Pt/V \tag{13}$$

where E is the sonication energy which is 320J/ml and P is the output power of the sonicator [Kun and DaoHui (2013)] which is 80 W. V is the volume of the solution to be sonicated which is 20ml in this case. Therefore the time, t for sonication was calculated to be 80 minutes. Tip sonication gives a homogeneous solution with 0.229 poise viscosity which is favorable for spin coating. The SEM image of the dispersed CNT is shown in Fig. 5. The dispersed CNTs were spin coated on to the dielectric surface of the silicon wafer of both the devices. A good coating ensures proper connectivity between electrodes. Both the spin-coated devices were annealed at 150˚C for ten minutes. The patterned metal electrodes were deposited over the CNT layer. Shadow masking or stencil lithography was used which gives patterns as imprints of the mask. Aluminium was deposited by thermal evaporation for the contact electrodes.
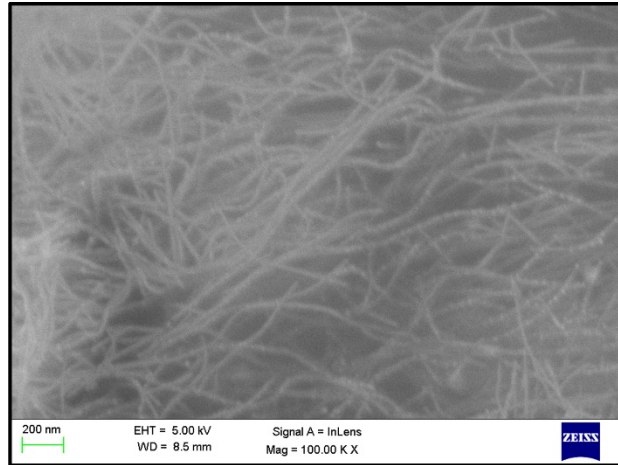

Figure 5: SEM image of the dispersed CNTs

4 Results and discussion

Ideally, the SB height can be tuned to any value just by selecting an appropriate metal with high work function for holes and low work function for electrons. Due to the Fermi level pinning at the metal interfaces, it is practically difficult to tune the SB height to zero. However, the Metal Induced Gap States does not establish Fermi level pinning for 1D channel materials [Javey, Guo, Wang et al. (2003)]. This makes the metal contacted CNTFETs extremely desirable as the SB heights can be tuned by the work function of the metal contacts.

Guo et al. [Guo, Datta and Lundstrom (2004)] performed a numerical comparative study of the effect of thickness of oxides on the ambipolar behavior of CNTs. They have numerically proved that a thick dielectric suppresses the ambipolar behavior of CNTs. The same result is demonstrated experimentally. Fig. 6 shows the comparison between the numerical simulation result by Guo et al. [Guo, Datta and Lundstrom (2004)] and our experimental result. The difference in the range of drain current is due to the small channel length in Guo et al. [Guo, Datta and Lundstrom (2004)] (~15 nm).
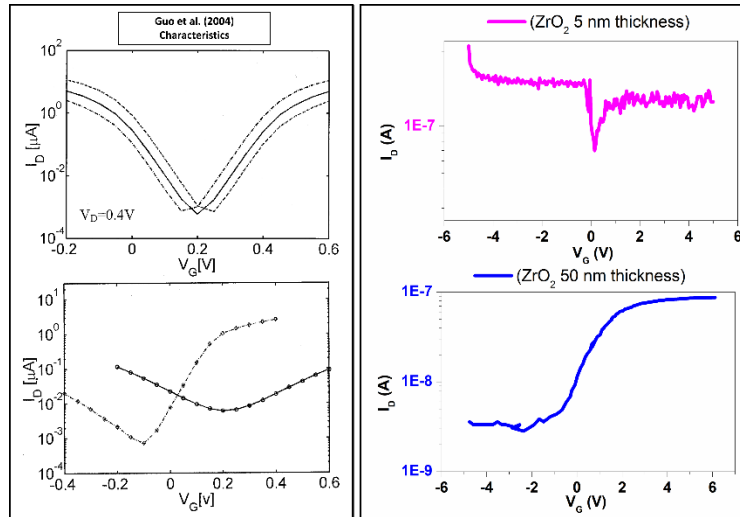

Figure 6: Comparison with the numerical simulation in Guo et al. [Guo, Datta and Lundstrom (2004)]. Left plot shows the IV characteristics of the numerical simulation in Guo et al. [Guo, Datta and Lundstrom (2004)]. Right plot is the IV characteristics for different gate oxide thickness (5 nm and 50 nm) of our experimental work

Aggressive scaling down of the gate oxide thickness makes the Schottky barriers very thin. This is because of the one-dimensional nature of CNTs [Odintsov (2000)]. Therefore, when the gate dielectric is thin, the tunneling of electrons and holes occur since both SBs (source and drain side) become transparent resulting in ambipolar conduction. The length scale over which the bands bend at the source/drain metal contacts is defined by the gate oxide thickness. When the gate dielectric is thick, the SBs are not transparent for tunneling. The gate to source voltage alters the band such that tunneling of electrons or holes takes place.

The I_D-V_G characteristics of the ambipolar devices exhibit a V-shaped plot as shown in Fig. 9. In devices with thick gate dielectric, the minimum of the V-shaped plot is shifted due to the trapped charges in the oxide. The suppression of ambipolar behavior can be observed. However, due to the increased thickness of the gate oxide layer, the on-current due to tunneling is reduced. A high-κ dielectric such as ZrO_2 with ε_k=22 is employed to increase the on-current due to thermionic emission. Thereby, the on-current is not affected.

Arijit Ray Chowdri [Chowdri (2007)] has demonstrated that on-current (I_{on}) can be improved by tube diameter modulation with thin high-κ dielectrics. It is proved that for smaller diameters (0.6 nm) of the nanotube the I_{on}/I_{off} ratio is better, but the on-current is

poor. Nanotubes with a diameter of 2 nm resulted in higher on-current, but the I_{on}/I_{off} ratio is poor. The proposed work modulates the thickness of the barrier by increasing the thickness of the high-κ gate oxide to suppress ambipolar behavior without affecting the on-current. An experiment to measure IV characteristics of a device with a low-κ gate oxide such as SiO_2 with ε=3.9 and with thickness ~50 nm was conducted. The characteristics show a suppression of the ambipolar conduction, but the on-current was less (in the order of pico Amps) as shown in Fig. 7(right). However, the measured characteristics for a device with high-κ gate oxide such as ZrO_2 with the same thickness (~50 nm) showed a higher on current while suppressing the ambipolar conduction. The current is in the order of micro amps as shown in Fig. 7(left). The suppression is due to the thick gate oxide whereas the higher on-current is due to the high-κ gate oxide. Thus it is validated that the increased thickness of high-κ gate oxide suppresses the ambipolar behavior and gives good on-current. A comparative graph showing the decrease in on-current for a low-κ gate oxide and increase in on-current for a high-κ gate oxide is presented in Fig. 7.
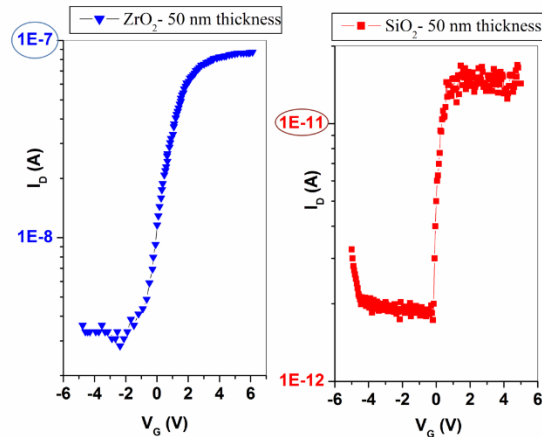

Figure 7: Comparison graph with different dielectrics. The plot in blue shows the characteristics for device with ZrO_2 (50 nm thickness) and plot in red shows the characteristics for device with SiO_2 (50 nm thickness)

The I_D-V_G characteristic for the device with thin gate oxide is shown in Fig. 8. The SB CNTFET with thin gate oxide exhibited ambipolar behavior. The reason behind this is that the SB is thin and transparent to electrons and holes when the gate oxide is thin.

Fig. 9 [Pourfath (2007)] shows the actual behavior of thin SB CNTFETs where the conduction is ambipolar due to the increased band to band tunneling of holes as a result of the barrier lowering at the drain side for drain voltages greater than the gate voltage. The thickness of the barrier at the drain side is also reduced, thereby contributing tunneling current. This causes a damaging effect on the device operation in both the on and off state. In the proposed fabricated device with thick gate oxide, the barrier lowering and the reduction in barrier thickness at the drain side does not take place due to the thick gate oxide. Therefore by introducing an asymmetry, the ambipolar conduction is suppressed.
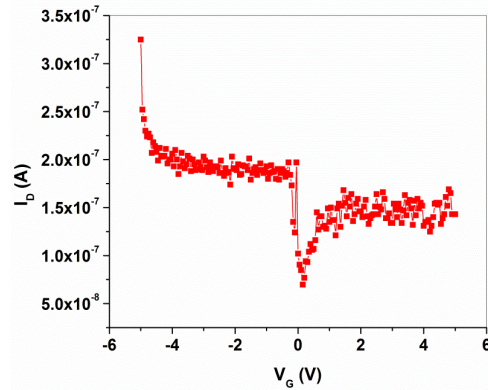
Figure 8: I_D- V_G Characteristics of the fabricated SB CNTFET with thin gate oxide (~5 nm) exhibiting ambipolar conduction
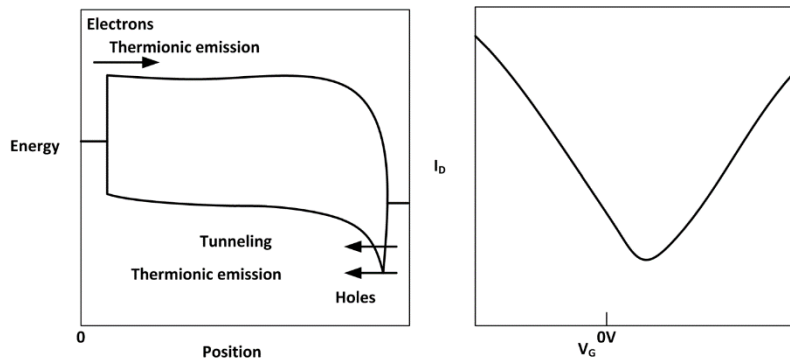

Figure 9: Band edge profile and output characteristics of an ambipolar CNTFET [Pourfath (2007)]

Fig. 10 shows the I_D-V_G characteristics of the device with thick gate oxide, t_{ox} of 50 nm for V_D=0.5 V and 1 V. This device did not exhibit ambipolar behavior. They exhibit unipolar characteristics when compared to the characteristics of the first device with the thin gate oxide. Thick SB is the reason for the suppression of the ambipolar conduction which is the result of thicker gate oxide. The SB limits the current at the metal-CNT contact. By changing the thickness of the tunneling barrier, the fringing field of the gate modulates the current. It is concluded that, in the second device, the conduction of electrons for negative gate voltages is suppressed due to the asymmetry introduced by the thick gate oxides. However, the on-current is compensated by the high-κ dielectric.
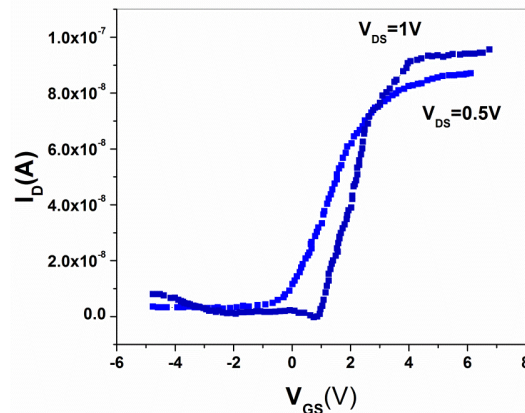
Figure 10: I_D- V_G characteristics of the device with thick gate oxide with suppressed ambipolar conduction

5 Conclusion

A mathematical model and an experimental demonstration of the suppression of the ambipolar property of CNTFETs are presented. The optimal gate oxide thickness and oxide dielectric constant were given by the particle swarm optimization. The ambipolar conduction is suppressed by employing thick high-κ gate oxides. The suppression is evident from the I_D-V_G characteristics of both the devices. The use of thin high-κ dielectric improves the on-current like in a scaled down MOSFET. However, the ambipolar behavior was still observed. A thick high-κ dielectric ensured suppression of this behavior. The experimental results show that the device with thin gate oxide (~5 nm) exhibited ambipolar behavior, whereas the device with thick gate oxide (~50 nm) exhibited unipolar characteristics. The loss in on-current due to the thick gate oxide is compensated by the use of a high-κ dielectric ZrO_2. The model was written in Verilog-A. Since the ambipolar conduction is suppressed, CNTFETs can be the next generation device for building robust digital circuits and reliable sensors and actuators for the IoT framework.

References

Atzori, L.; Iera, A.; Morabito, G. (2010): The internet of things: a survey. *Computer Networks*, vol. 54, pp. 2787-2805.

Avouris, P.; Appenzeller, J.; Martel, R.; Wind, S. J. (2003): Carbon nanotube electronics. *Proceedings of the IEEE* , vol. 91, no. 11, pp. 1772-1784.

Bhatt, V. D.; Joshi, S.; Becherer, M.; Paolo, L. (2017): Flexible, low-cost sensor based on electrolyte gated carbon nanotube field effect transistor for organo-phosphate detection. *Sensors*, vol. 17, no. 5, pp. 1147.

Chen, W.; Zhang, Z.; Feng, Z.; Chen, Y.; Jiang, K. et al. (2008): Measurement of polarized nano-material (PNM) for microwave applications. *IEEE MTT-S International Microwave Symposium*, vol. 2, pp. 1577-1580.

Chowdri, **A.** (2007): *Designing Low-Power and High-Performance Digital Circuits with Carbon Nanotube Transistors (Ph.D. Thesis)*. Purdue University, Indiana.

Dürkop, T.; Getty, S. A.; Cobas, E.; Fuhrer, M. S. (2004): Extraordinary mobility in semiconducting carbon nanotubes. *Nano Letters*, vol. 4, no. 1, pp 35-39.

Eberhart, R.; Kennedy, J. (1995): A new optimizer using particle swarm theory. *Proceedings of the Sixth International Symposium on IEEE Micro Machine and Human Science, 1995. MHS'95*, pp. 39-43.

Endoh, T.; Momma, Y. (2007): Study of 30-nm Double-Gate MOSFET with halo implantation technology using a two-dimensional device simulator. *IEICE Transactions on Electronics*, vol. 90, no. 5, pp. 1000-1005.

Guo, J.; Datta, S.; Lundstrom, **M.** (2004): A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors. *IEEE Trans. Electron Devices*, vol. 51, pp. 172.

Huo, X.; Zhang, M.; Chan Philip, C. H.; Liang, Q.; Tang, Z. K. (2004): High frequency S parameters characterization of back-gate carbon nanotube field-effect transistors. *IEEE IEDM*, vol. 4, pp. 691-694.

Hwang, H.; Lee, D. H.; Hwang, J. M. (1996): Degradation of MOSFETs drive current due to halo ion implantation. *International Electron Devices Meeting*, pp. 567-570.

Ieong, M.; Narayanan, V.; Singh, D.; Topol, A.; Chan, V. et al. (2006): Transistor scaling with novel materials. *Materials Today*, vol. 9, pp. 26-31.

Javey, A.; Guo, J.; Wang, Q.; Lundstrom, M.; Dai, H. J. (2003): Ballistic carbon nanotube field effect transistors. *Nature*, vol. 424, pp. 654-657.

Javey, A.; Kong, J. (2009): *Carbon Nanotube Electronics*. Springer Science & Business Media.

John, D. L.; Castro, L. C.; Pereira, P. J. S.; Pulfrey, D. L. (2004). A Schrödinger-Poisson solver for modeling carbon nanotube FETs. *Proceedings of NSTI Nanotech*, vol. 3, pp. 65-68.

Kun, Y.; DaoHui, L. (2013): Sonication-assisted dispersion of carbon nanotubes in aqueous solutions of the anionic surfactant SDBS: the role of sonication energy. *Journal of Material Science*, vol. 58, pp. 2082-2090.

Li, J.; Tianjian, L.; Jing, N.; Kim, N. S.; Guo, M. et al. (2018): CNFET-based high throughput SIMD architecture. *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 37, no. 7, pp. 1331-1344.

Lin, Y.; Appenzeller, J.; Avouris, P. (2004): Ambipolar-to-unipolar conversion of carbon nanotube transistors by gate structure engineering. *Nano Letters*, vol. 4, no. 5, pp. 947-950.

Liu, F.; Chen, W.; Zhang, Z.; Feng, Z.; Chen, Y. et al. (2009): Measurement on dipole antenna with light polarized nano-material (PNM) textile reflector. *IEEE International Microwave Symposium Digest*, vol. 2, pp. 1069-1072.

Pourfath, M. (2007): *Numerical Study of Quantum Transport in Carbon Nanotube-Based Transistors (Ph.D. Thesis)*. Institute for Microelectronics, Austria.

Naderi, A.; Keshavarzi, P.; Orouji, A. A. (2011): LDC-CNTFET: a carbon nanotube field effect transistor with linear doping profile channel. *Superlattices and Microstructures*, vol. 50, pp. 145-156.

Nouri-Bayat.; Ramin; Kashani-Nia, A. (2017): Designing a carbon nanotube field-effect transistor with high transition frequency for ultra-wideband application. *Engineering*, vol. 9, no. 1, pp. 22.

Odintsov, A. (2000): Schottky barriers in carbon nanotube heterojunctions. *Physics Review Letters*, vol. 85, pp. 150.

Radosavljevic, M.; Heinze, S.; Tersoff, J.; Avouris, P. (2003): Drain voltage scaling in carbon nanotube transistors. *Applied Physics Letters*, vol. 83, pp. 2435-2437.

Santagata, E.; Baglieri, O.; Tsantilis, L. (2015): Effect of sonication on high temperature properties of bituminous binders reinforced with nano-additives. *Journal of construction and building materials*, vol. 7, pp. 395-403.

Taghavi, A.; Carta, C.; Meister, T.; Ellinger, F.; Claus, M. et al. (2017): A CNTFET oscillator at 461 MHz. *IEEE Microwave and Wireless Components Letters*, vol. 27, no. 6, pp. 578-580.

Thai, T. T.; Yang, L.; DeJean, G. R.; Tentzeris, M. M. (2011): Nanotechnology enables wireless gas sensing. *IEEE Microwave Magazine*, pp. 85-95.

Xuan, C. T.; Thuy, N. T.; Luyen, T. T.; Huyen, T. T.; Tuan, M. A. (2017): Carbon nanotube field-effect transistor for DNA Sensing. *Journal of Electronic Materials*, vol. 46, no. 6, pp. 3507-3511.

Yoon, Y.; Fodor, J.; Guo, J. (2008): A computational study of vertical partial-gate carbon-nanotube FETs. *IEEE Transactions on Electron Devices*, vol. 55, no. 1, pp. 283-288.

Zahra, A.; Orouji, A. A. (2009): Novel attributes in the performance and scaling effects of carbon nanotube field-effect transistors with halo doping. *Superlattices and Microstructures*, vol. 45, pp. 535-546.

Zanchetta, S.; Todon, A.; Abramo, A.; Selmi, L.; Sangiorgi, E. (2002): Analytical and numerical study of the impact of halos on short channel and hot carrier effects in scaled MOSFETS. *Solid-State Electronics*, vol. 46, pp. 429-434.

Zhang, W.; Zhu, Z. Y.; Wang, F.; Wang, T. T.; Sun, L. T. et al. (2004): Chirality dependence of the thermal conductivity of carbon nanotubes. *Nanotechnology*, vol. 15, no. 8, pp. 936-939.