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A Pathway to Explore the Hidden Specialty in the Design of Fifteen Level Inverter in Grid Connected PV System

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Abstract: This research paper proposes a single phase fifteen level inverter for a grid connected PV system. The proposed inverter is also called cascaded asymmetric multilevel inverter. By adopting appropriate hybrid modulation technique improved output voltage is obtained with minimum number of power electronic switches. By reducing the number of gate triggering circuits of the switches, the size and power consumption of the driving circuits can be reduced. The total harmonic distortion of the output of the inverter is improved by this inverter. The proposed inverter developed by cascading a full bridge inverter with modified H bridge multilevel inverter. The validity of the proposed system is verified through MATLAB simulations.

Keywords: Hybrid modulation, multilevel inverter, photo voltaic system, grid connected inverter.

1 Introduction

In current scenario, there is thirst for advanced inverter designs which lead the design of multi level inverters, More commonly single-phase five-level inverter are controlled by two novel Pulse Width PWM techniques are designed based on minimum switching power loss and minimum Total Harmonic Distortion (THD). In a single-phase five-level inverter employing six switches, in all the PWM proposed techniques. It requires four switches operate at switching frequency and the other two switches in turn operate at line frequency, whereas there are also some PWM proposed technique which requires only two switches operate at switching frequency and the others operate at line frequency [Sonti, Jain and Bhattacharya (2017)]. Broad applications of dc-dc converters are conceptually explained in many surveys and summarized with comparative study of different voltage-boosting techniques. DC-DC converters with voltage boost capability are widely used in a large number of power conversions. The permutations and combinations of the various voltage-boosting techniques with additional components in a circuit allow for numerous new topologies and configurations, which are often confusing and difficult to follow. Therefore, to present a clear picture on the general law and framework of the development of next-generation step-up DC-DC converters, this paper aims to comprehensively review for classifying various step-up dc-dc converters based

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on their characteristics and voltage-boosting techniques. In addition, the advantages and disadvantages of these voltage-boosting techniques and associated converters are discussed in detail. Finally, broad applications of dc-dc converters are presented and summarized with comparative study of different voltage-boosting techniques [Sonti and Jain (2017)]. A power conditioning system (PCS) using multiple module-integrated converters and a single sourced 27-level asymmetric cascaded H-bridge multilevel inverter without regeneration for photovoltaic applications. There is a scheme called PCS with the control scheme which is implemented similar to the work that we have included in this research work. It gives a perfect floor to establish effective results [Kadam and Shukla (2017)]. The common mode (CM) leakage current needs to be addressed carefully in order ensure the smooth operation of transformerless grid connected PV system, In present scenario the conceptual implementation of novel multilevel transformerless inverter topology which completely eliminates CM leakage current by connecting grid neutral point directly to the PV negative terminal, thereby bypassing the PV stray capacitance. It provides a low-cost solution consisting of only four power switches, two capacitors, and a single filter inductor [Liu, Abu-Rub, Ge et al. (2016)].

Pulse width modulation (PWM) technique is purely meant for the minimization of the leakage current in the grid-connected/stand-alone transformerless photovoltaic (PV)-cascaded multilevel inverter (CMLI).PWM technique is integrated with the MPPT algorithm and is applied to the five-level CMLI. Furthermore, using the proposed PWM technique the high-frequency voltage transitions in the terminal and common mode voltages are minimized [Chattopadhyay and Chakraborthy (2017)]. Among the various kinds of renewable energy sources solar and wind energy become very attractive due to the abundant nature and advancement in power electronic equipments. Photovoltaic sources are employed in many solar based applications to extract the electrical energy from the sun as they have an advantage of being reliable and pollution free. Also it is maintenance free. Photovoltaic (PV) sources are employed in many solar based applications to extract the electrical energy from the sun as they have an advantage of being reliable and pollution free, also it is maintenance free. PV inverter is the main part of the PV system used to convert the dc voltage from the PV panel into AC Voltage to be fed into the grid. Enhancing the output waveform diminishes its corresponding harmonic content also size of the filter. There are numerous inverter topologies are available for grid connected PV system [Sonti and Jain (2017)]. The main problem focused in the paper is total harmonic distortion and to improve the output voltage. If a power electronic switch used in a high voltage inverter, then it cannot be operate at high switching frequency. Hence their switching frequency is restricted. Hence the operating voltage of the device must be reduced to use high speed switches. High speed switches contributes very low harmonic content compared to low speed switches. Multilevel inverters can reduce device voltage and output harmonics by increasing number of output voltage levels. In single-phase multilevel inverters, the most widely used techniques are diode clamped inverters, flywheel capacitor inverters and cascaded H-bridge inverter (CHB). Among all this inverter cascade H bridge inverter drawn more attention due to its simplicity and circuit modularity. Varity of modulation techniques can be implemented only in CHB.

2 Proposed method

The Block diagram of the proposed inverter is shown in Fig. 1. This proposed single phase inverter is combination of a modified H-bridge inverter (seven level inverter) and conventional H bridge inverter connected in parallel. The upper H bridge inverter is conventional, whereas the lower H bridge is a modified H bridge inverter developed in [Rahim, Chaniago and Selvaraj (2011)]. The intention of using the modified H-bridge configuration is to reduce the switching devices, power diodes, capacitors and isolated DC source. Upper and lower inverters are connected with individual PV arrays. Since the proposed inverter is an asymmetrical inverter voltage of the lower inverter is higher than the upper inverter. Voltage from the PV array is boost up by the dc-dc converter to the level required by grid. Current injected into the grid is filtered by Lf.

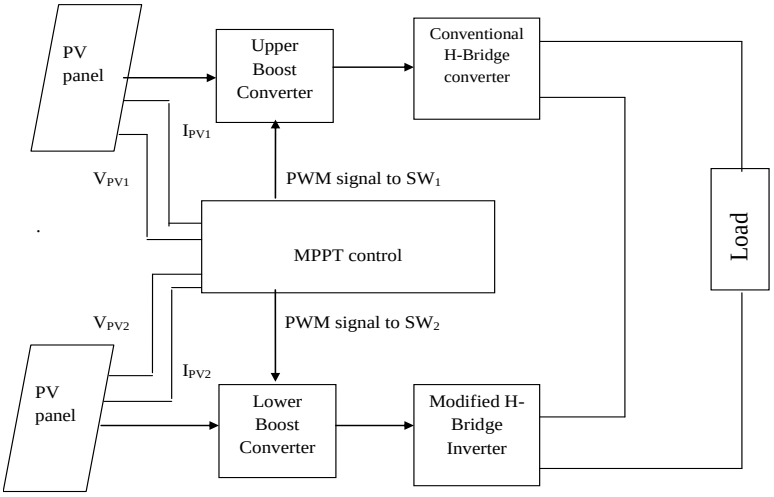

Figure 1: Block diagram of the proposed inverter

2.1 Hybrid modulation

Hybrid modulation technique reduces the switching losses of the proposed inverter by appropriate switching pattern. Proposed inverter is asymmetric inverter hence the input voltages of upper and lower inverter are not the same. Since power fed from the lower inverter is more than the upper inverter, it is switched at low frequency and the upper inverter is switched at high frequency.

2.2 Lower inverter

Three reference signals (V_{ref1} V_{ref2} V_{ref3}) were compared with the carrier signal ($V_{carrier}$). The reference signals has the equal magnitude and frequency and was in phase with each other by an offset value. But they were shifted consequently in y axis by a constant value. V_{ref1} was compared with $V_{carrier}$ until its amplitude is higher. $V_{carrier}$ compared with V_{ref2} till its amplitude is higher. V_{ref3} compared with $V_{carrier}$ until it reaches zero. Once V_{ref3} had reached zero, V_{ref2} would be compared until it reaches zero. Then V_{ref1} would be compared with $V_{carrier}$. Fig. 4 shows the resulting switching pattern. Switches S_1, S_3, S_5

and S_6 switched at a frequency of carrier signal were as S_2 and S_4 switched at fundamental frequency. Lower inverter produces seven level output voltage. Lower inverter supplies more voltage (240 V) to the grid and switched at low frequency.

2.3 Reference wave and carrier wave generation

The simulation results were carried out by using MATLAB/SIMULINK environment to prove that the proposed inverter can be implemented practically. It helps to observe the switching strategy of fifteen level inverter. Switching pattern for the lower inverter is generated by comparing three reference signals and triangular carrier signal shown in Fig. 1. The resulting PWM signals are shown in the Fig. 2. The modulation index determines the shape of the inverter output voltage. The lower inverter is switched at low frequency (50 Hz) and the upper inverter has high frequency (10 kHz). Upper inverter dc input voltage is 65 volts and lower inverter dc bus voltage is six times of upper inverter that is 390 volts. The switching signals are developed by the equations as described. Finally the desired waveform of seven level stepped waveform is obtained at lower level inverter which is shown in Fig. 3.

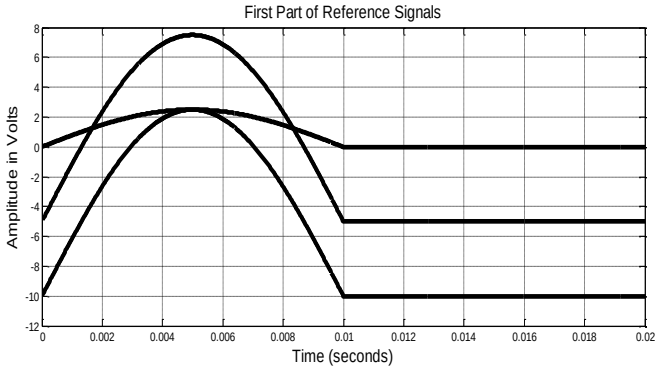

Figure 2: First part of reference signals

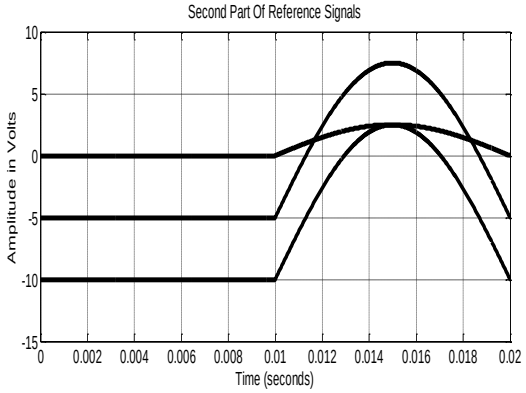

Figure 3: Second part of reference signals

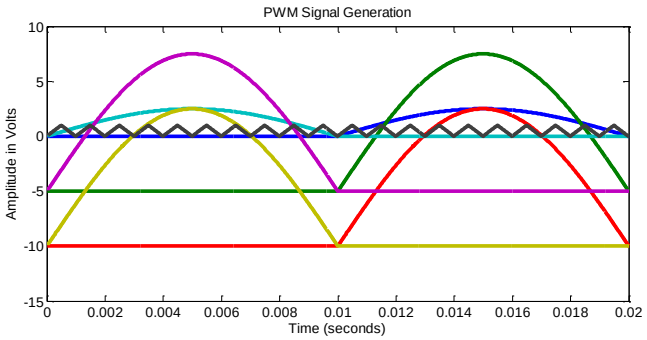

Figure 4: PWM signal generation of lower inverter

2.4 Arithmetic equation for reference signal and pulses generation

Reference wave form of the lower inverter is generated by the following equations,

The overall reference signal, $V_{ref} = \sin \omega t$

Three reference signals,

$V_{ref1} = |V_{ref}|*12.5$

$V_{ref2} = |V_{ref}|*2$

$V_{ref3} = |V_{ref}|*12$

These reference signals are further divided into two parts.

$V_{ref1} = \{V_{ref11}$ if $0<t<T/2$

V_{ref12} if $T/2<t>T$

$V_{ref2} = \{V_{ref21}$ if $0<t< T/2$

V_{ref22} if $T/2<t>T$

$V_{ref3} = \{V_{ref31}$ if $0<t<T/2$

V_{ref32} if $T/2<t>T$

T = Time period

PWM switching signals generation

$K_1 = \{1$ if $V_{ref11}>0$

0 if $V_{ref11}<0$

$K_2 = \{1$ if $V_{ref12}>0$

0 if $V_{ref12}<0$

$K_3 = \{1$ if $V_{ref21}>0$

0 if $V_{ref21}<0$

$K_4 = \{1$ if $V_{ref22}>0$

0 if $V_{ref22}<0$

$K_5 = \{1$ if $V_{ref31}>0$

0 if $V_{ref31}<0$

K_6= {1 if V_{ref32}>0

0 if V_{ref32}<0

Switching signals

C= Carrier wave "||" represents comparison

"+ "denotes logical OR operation

Q_1 = (K_3+ K_5)|| C

Q_2 = (1 for 0.01<t<0.02)

Q_3= (K_1+K_3)|| C

Q_4 = (1 for 0<t<0.01)

Q_5 = Q_1'+ (K_2 +K_3+K_4)||C

Q_6 = Q_3'+ (K_1+K_2+K_3)||C

Q'= compliment of Q

Q_1, Q_2, Q_3, Q_4, Q_5 and Q_6 are the switching signals of lower inverter.

Each reference signal is identical with each other and displaced by an offset value -5. These three signals are generated and compared with the carrier wave (triangular wave) of frequency 10 KHz. Frequency of the reference signal is 50 Hz.

In order to reduce the switching losses of the proposed inverter hybrid modulation scheme is used. Switching pulses are generated by comparing three reference signals V_{ref1}, V_{ref2}, and V_{ref3} and a carrier signal $V_{carrier}$. Fig. 2 shows the switching pulse generation of seven level inverter. All three reference signal had same frequency and amplitude with an offset value equivalent to the amplitude of carrier signal. The reference signals were compared with the carrier signal simultaneously. Frequency of the reference signal is 50Hz and the carrier signal is 1 KHz.

Triangular wave is a carrier signal of frequency 1 KHz and amplitude one and modified sine wave is modulation signal of frequency 50 Hz (fundamental frequency) with the amplitude of 2.5 each waves are displaced by a constant value as shown in Fig. 4.

- Switching pulses for switch Q_1: First part of the reference signal V_{ref3} is compared with the carrier signal until $V_{carrier}$ is greater than V_{ref3} and V_{ref1} is compared with the $V_{carrier}$ until V_{ref1} is greater than $V_{carrier}$.
- Switching pulses for switch Q_2: It is an ordinary gate pulse of fundamental frequency with first half of the period turned OFF and second of the period turned ON.
- Switching pulses for switch Q_3: Reference signal V_{ref1} is compared with the carrier signal until it exceeds the peak amplitude of the carrier signal $V_{carrier}$ and second part of the V_{ref3} is compared with $V_{carrier}$ until carrier wave amplitude is greater than the reference signal.
- Switching pulses for switch Q_4: It is an ordinary gate pulse of fundamental frequency with first half of the period turned ON and second of the period turned OFF.
- Switching pulses for switch Q_5: First part of V_{ref2} reference signal is compared with $V_{carrier}$ until less than V_{ref2} for a first carrier frequency and both are compared until

$V_{carrier}$ greater than V_{ref2} and (inverted signal of first part of Q_5) first part of reference signal V_{ref3} is compared with the carrier signal until $V_{carrier}$ is lesser than V_{ref3} and V_{ref1} is compared with the $V_{carrier}$ until V_{ref1} is lesser than $V_{carrier}$. The second part of Q_5 is obtained by comparing V_{ref1} and V_{ref2} with the carrier signal as shown in Fig. 2.

- Switching pulses for switch Q_6: First part of the Q_6 is obtained by comparing V_{ref1} and V_{ref2} with the carrier signal as shown in the Fig. 2 and the second part is obtained by V_{ref2} and V_{ref3} with the carrier signal and second part of V_{ref3} compared with the carrier until V_{ref3} lesser than carrier amplitude.

Table 1: The inverter output voltage for various time duration

Duration	**Output Voltage**
$0<\omega t<\theta_1$ and $\theta_4<\omega t<\pi$	$0<V_{inv}<V_{dc}/3$
$\theta_1<\omega t<\theta_2$ and $\theta_1<\omega t<\theta_2$	$V_{dc}/3<V_{inv}<2V_{dc}/3$
$\theta_2<\omega t<\theta_3$	$2V_{dc}/3<V_{inv}<V_{dc}$
$\pi<\omega t<\theta_5$ and $\theta_8<\omega t<2\pi$	$0<V_{inv}<-V_{dc}/3$
$\theta_5<\omega t<\theta_6$ and $\theta_7<\omega t<\theta_8$	$-V_{dc}/3<V_{inv}<-2V_{dc}/3$

The inverter operating voltage for various time duration is shown in Tab. 1.

Theoretically modulation index can be defined as the ration of amplitudes of modulating signal to the carrier signal.

$$M = \frac{A_m}{A_c}$$

Since the proposed inverter uses three carrier signals, the modulation index is,

$$M = \frac{A_m}{3A_c}$$

Where A_c is the peak-to-peak value of the carrier signal and A_m is the peak value of the voltage reference signal V_{ref}. Level of the output voltage can be varied by varying the modulation index.

2.5 Upper inverter

Reference wave form of an upper inverter is combination of saw tooth and positive half cycle of sine wave. Fig. 5 shows the reference wave form of upper inverter.

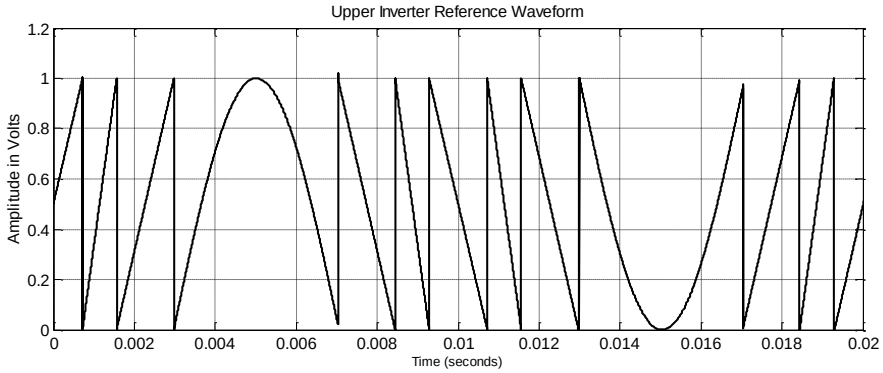

Figure 5: Upper inverter-reference waveform

The above reference wave is compared with the carrier wave to generate PWM pulses for power switches in upper inverter. The above reference wave is compared with the carrier wave to generate PWM pulses for power switches in upper inverter. Upper inverter produces three level output voltage. Carrier wave of the upper PWM is triangular wave form of 1 KHz with unity magnitude. Upper inverter supplies less voltage to the grid and switched at high switching frequency.

2.6 Grid connected PV system

The schematic diagram of grid connected PV system is shown in the Fig. 6. Cascaded upper and lower inverter generates fifteen level output voltage. Output Voltages of both inverters summed up and gives the resultant voltage. Proposed inverter is of asymmetrical type; hence voltage across the capacitor in lower H-bridge is two time the magnitude of upper bridge capacitor. (i.e. $V_{dc2} = V_{dc3} = V_{dc3} = 2V_{dc1}$).

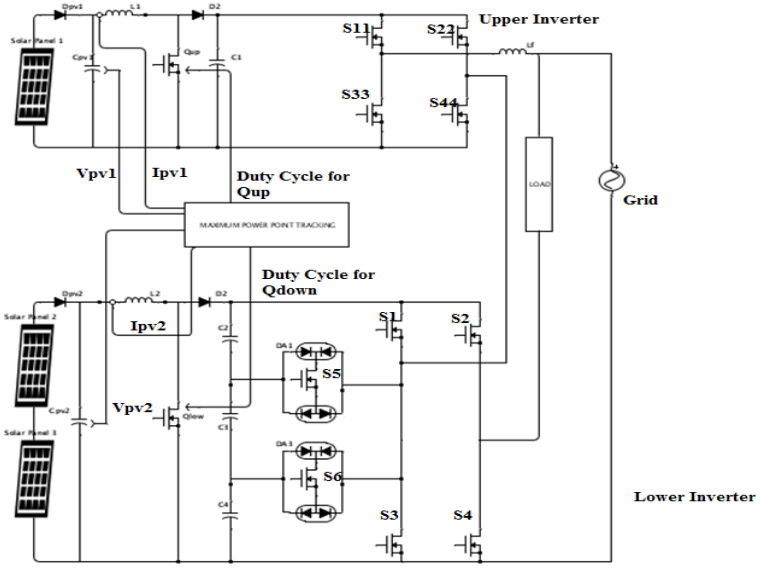

Figure 6: Schematic diagram of grid connected PV system

Hence DC-link voltage of lower H-bridge is six times that of upper H-bridge. (i.e. $V_{dc, low}=6V_{dc1}$). If we take PV panels of equal rating upper H-bridge inverter needs single PV panel as input, whereas lower H-bridge inverter needs six PV panels. Thus most of the power fed to the load is from lower level inverter. Lower H-bridge inverter is of generating seven level output ($6V_{dc1}$, $4V_{dc1}$, $2V_{dc1}$, 0, $-2V_{dc1}$, $-4V_{dc1}$, $-6V_{dc1}$). Upper conventional inverter generates three level output (V_{dc}, 0, $-V_{dc}$).

2.7 Boost converter

Boost converter boost up the voltage to the inverter output matches voltage the grid voltage. Input of the boost converter is output of the PV panel. According to the duty cycle which is being calculated by the MPPT algorithm the boost converter output also varies to track the maximum power from the PV panel. There are two boost converters are used in proposed system, there are upper boost converter and lower boost converter.

3 Results and discussion

Fig. 7 shows the simulink model of fifteen level inverter. Here both the upper and lower inverters are cascaded together and forms an asymmetrical fifteen level inverter. Three level output voltage of upper inverter and seven level output voltage of lower inverter are cumulatively added and produce fifteen level output voltage.

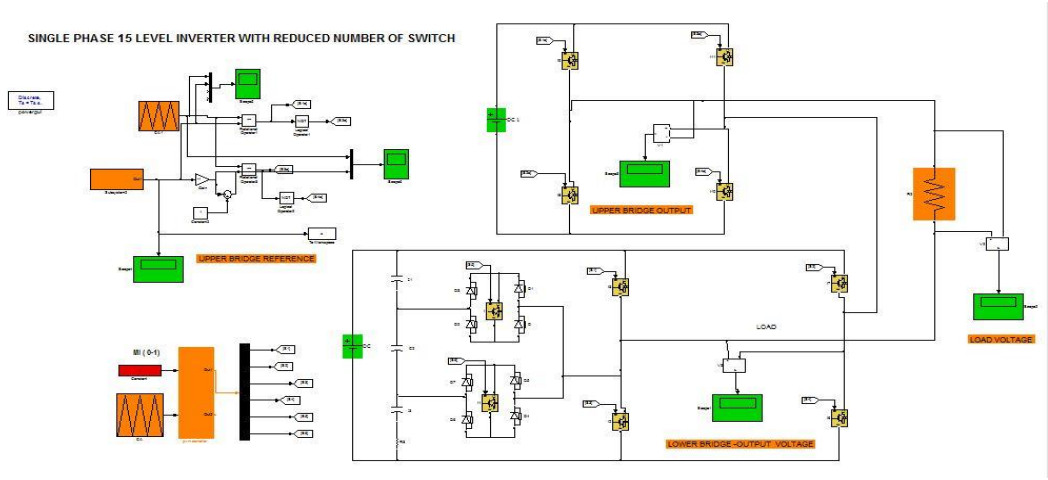

Figure 7: Simulink model of fifteen level inverter

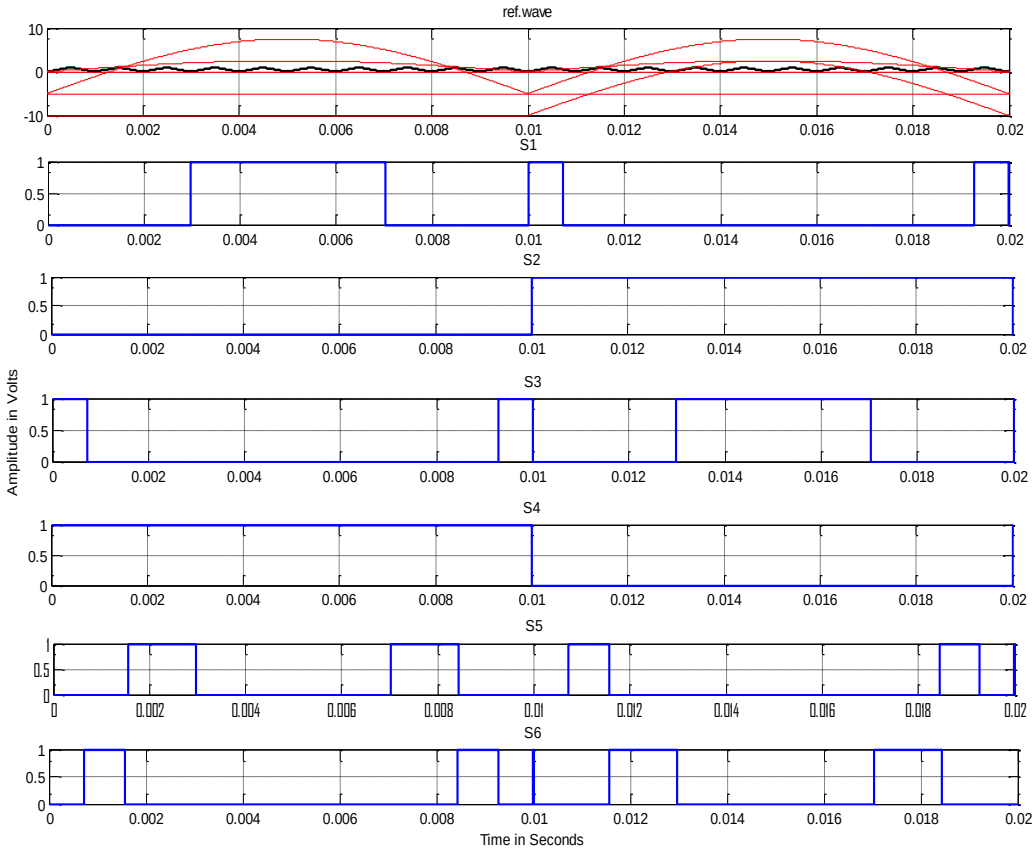

Figure 8: Switching signals of lower inverter

The Fig. 8 shows the switching signals of the switches, where the switching frequency of Q_1, Q_3, Q_5 and Q_6 pulses propositional to the carrier frequency but the switching frequency of the pulses Q_2 and Q_4 are equal to the fundamental frequency 50 Hz.

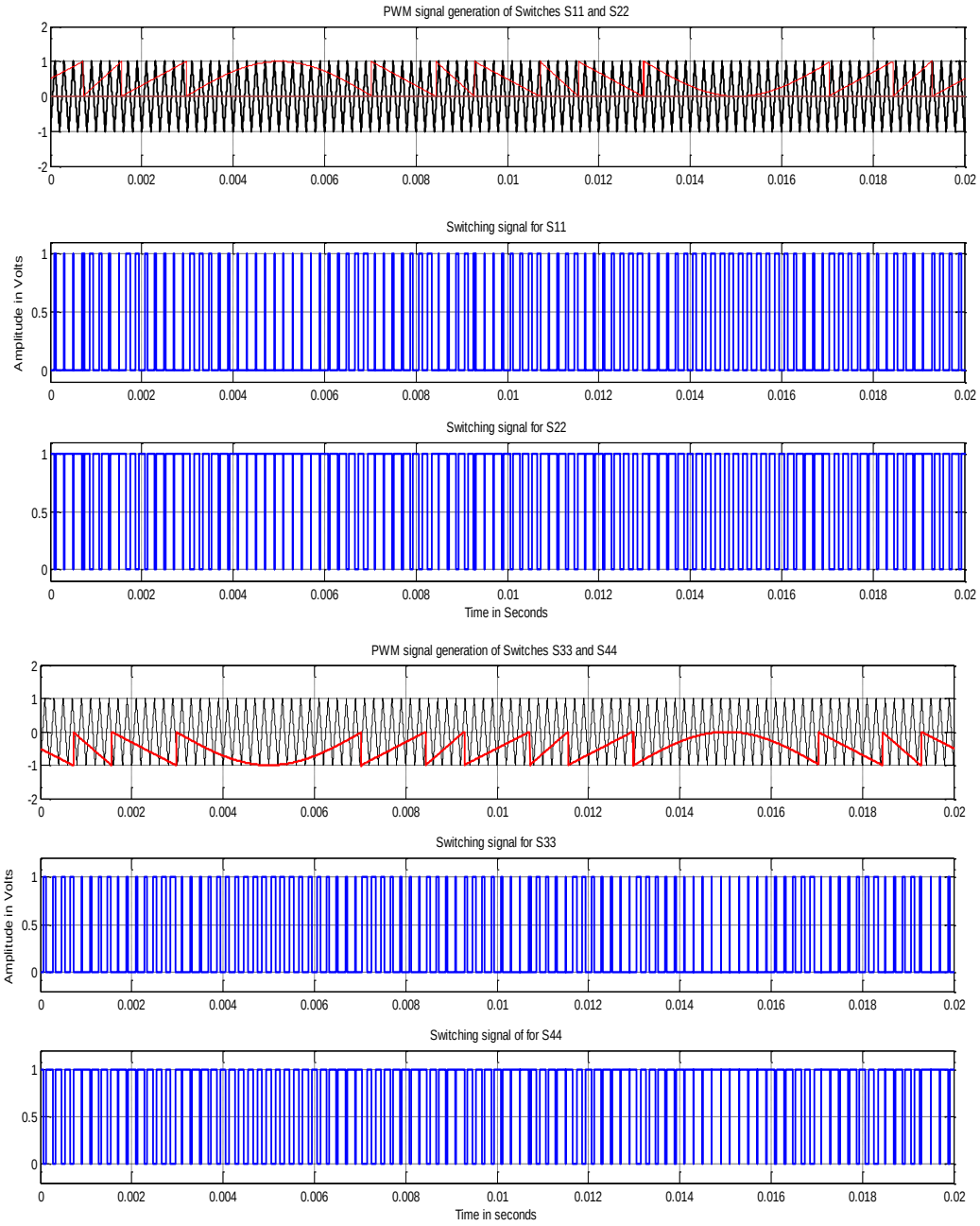

Figure 9: Switching signal of upper inverter

Switching pulses of upper Inverter is shown in Fig. 9 whose frequency is 5 Khz. Output voltage of upper and lower Inverter is shown in Fig. 10 and Fig. 11 respectively.

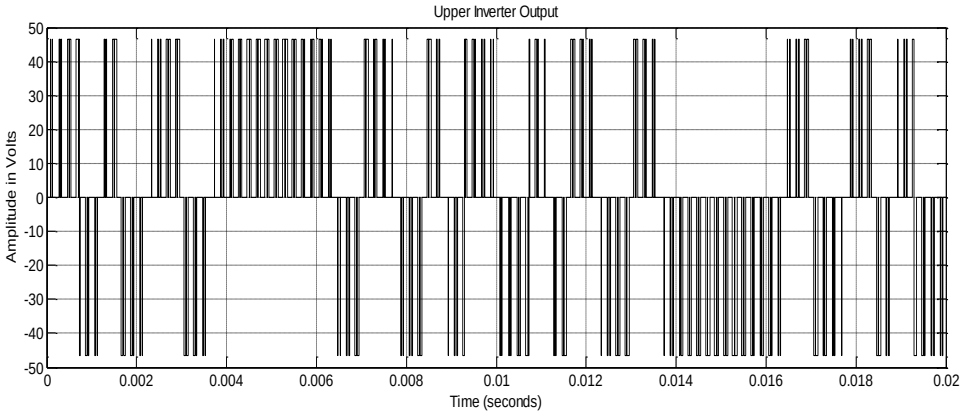

Figure 10: Upper inverter output voltage

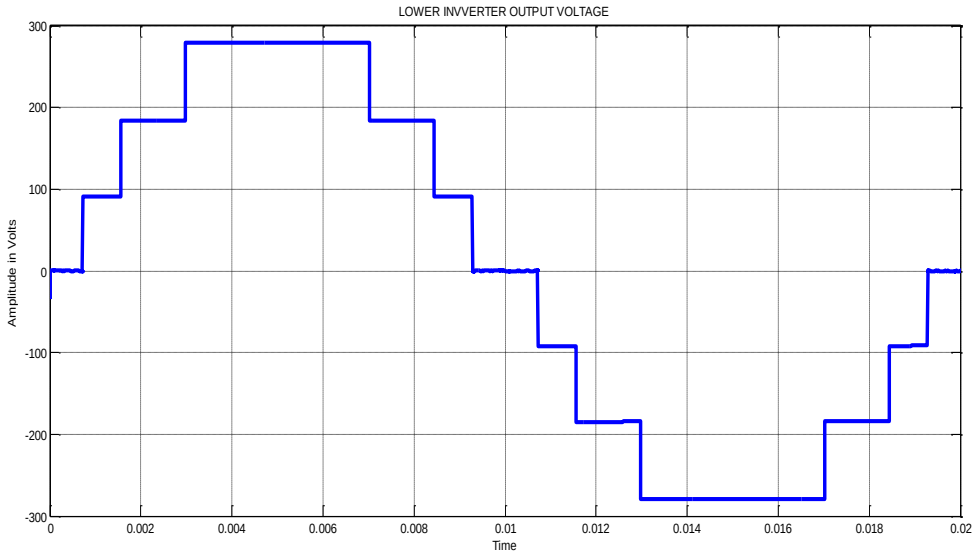

Figure 11: Lower inverter output voltage

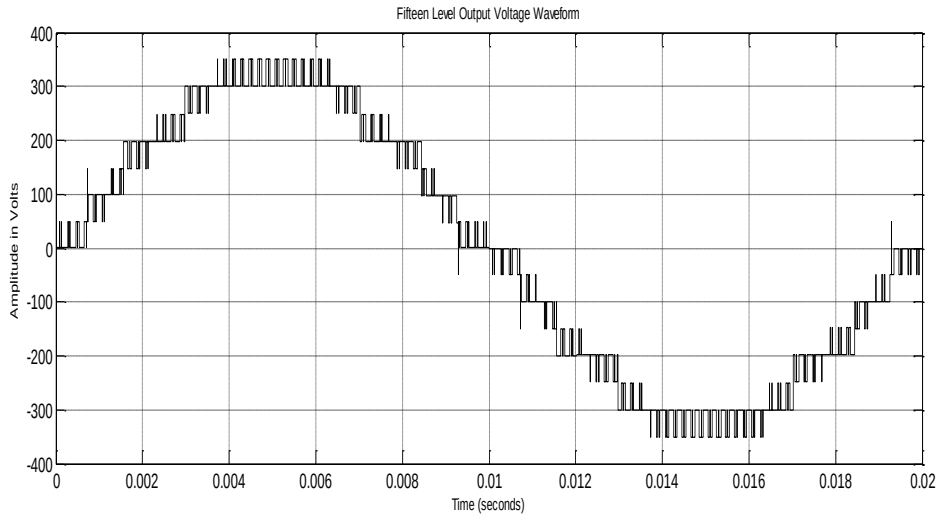

Figure 12: Fifteen level inverter output voltage

Output Voltage of Cascaded Inverter (upper and lower) of frequency 50 Hz shown in Fig. 12.

3.1 Simulink model of fifteen level grid connected inverter for PV system

Fig. 13 shows the simulink model of grid connected inverter fed PV system. Input to the inverter is taken from the PV panel. Output power from the PV panel is not constant because of the change in solar irradiance. MPPT algorithm is implemented to optimize the input power to the inverter from the PV panel and maintain the output voltage constant even though the solar irradiance changes with respect to time.

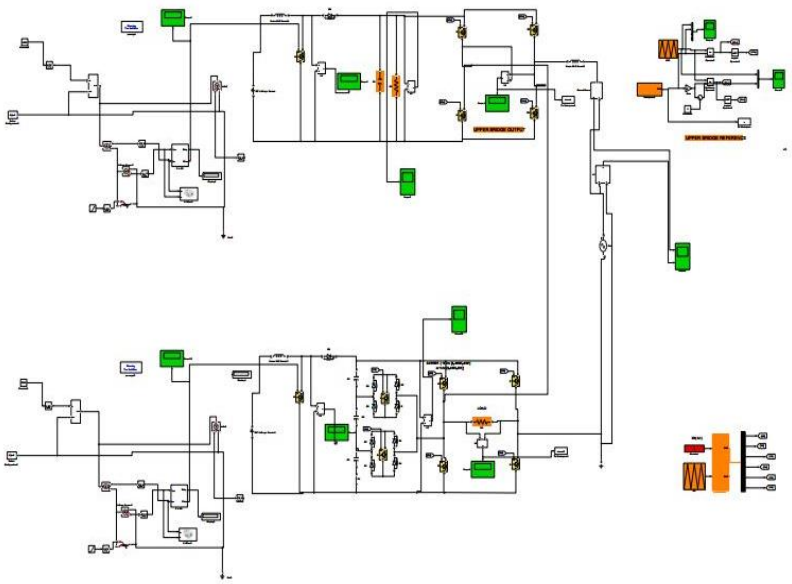

Figure 13: Simulink model of grid connected fifteen level inverter for PV system

3.2 Simulink model of Perturb and Observe (P&O) MPPT algorithm

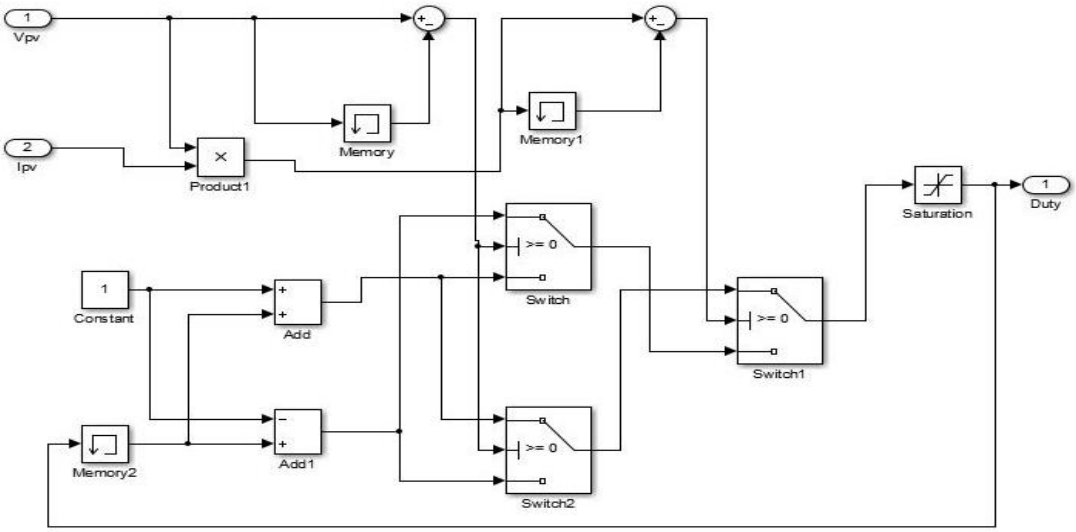

Figure 14: Simulink model of Perturb and Observe MPPT algorithm

Fig. 14 shows the simulink model of Perturb and Observe MPPT algorithm. The above simulink model is formed as per P&O algorithm. Saturation value is set between 0.33 to 0.23 by duty cycle calculation (Appendix).

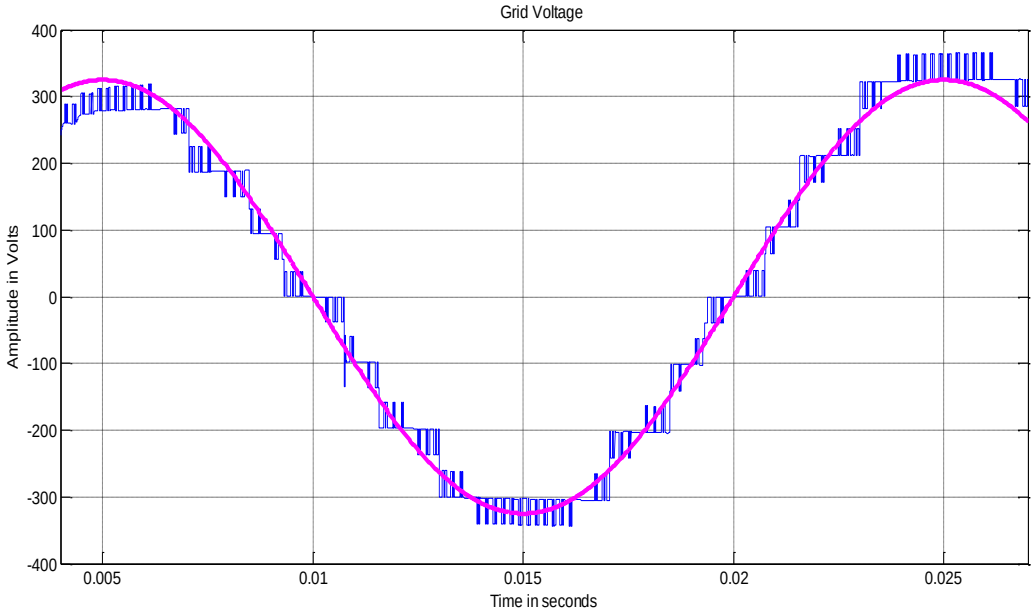

Figure 15: Grid voltage

Inverter output voltage is approximately matches with the grid voltage as shown in Fig. 15.

Analysis of total harmonic distortion (THD)

The THD analysis of three level inverter is shown in the Fig. 16 whose value is 31.70%.

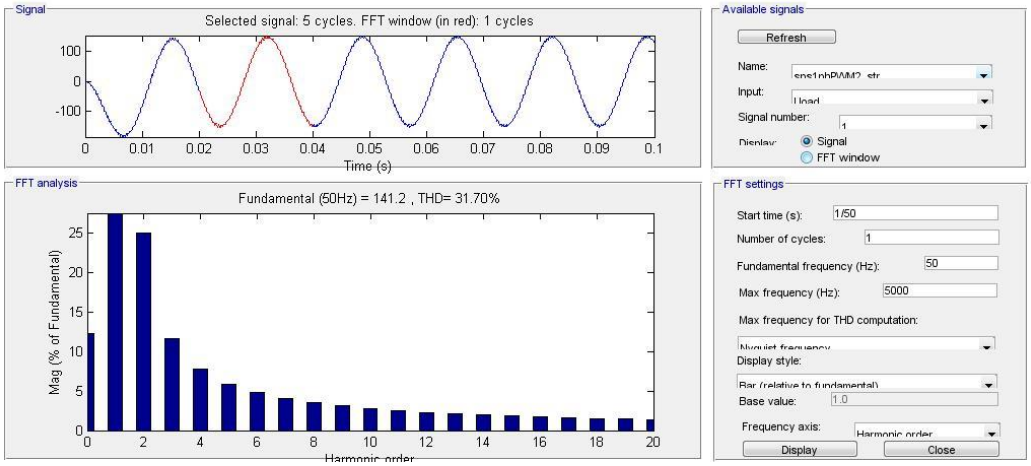

Figure 16: THD analysis of three level inverter

The THD seven level inverter is shown in the Fig. 17 whose value is 11.90%.

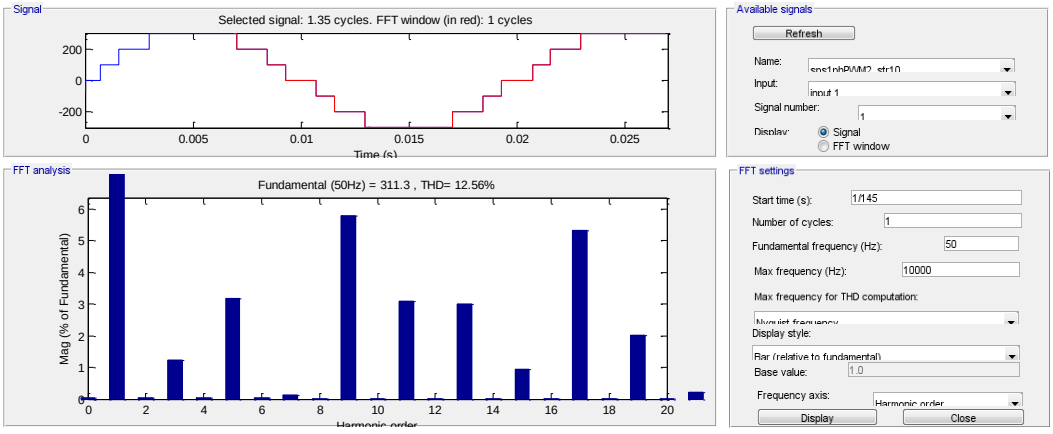

Figure 17: THD analysis of seven level inverter

The THD analysis of grid connected fifteen level inverter is shown in the Fig. 18 whose value is 4.99%.

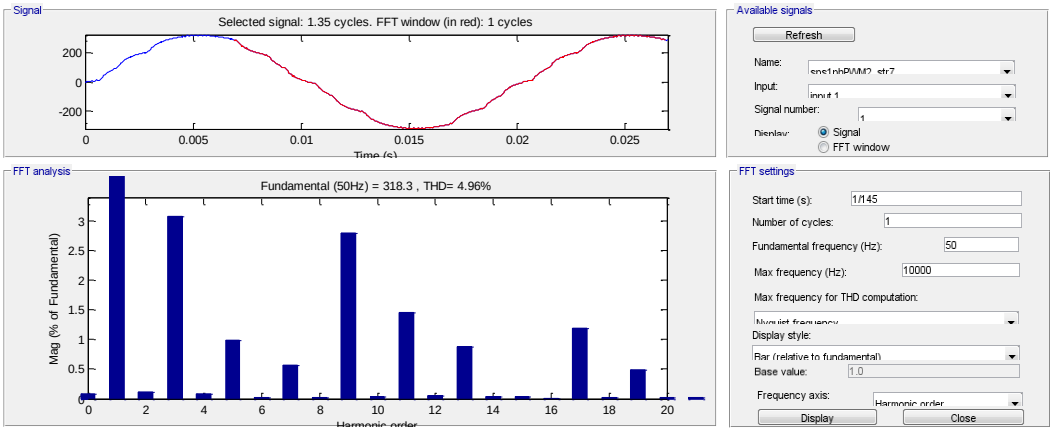

Figure 18: THD analysis of grid connected fifteen level inverter

It is observed that the THD value of grid connected fifteen level inverter for PV system is less than 5% which is clearly depicted in Tab. 2.

Table 2: Comparison of different multilevel inverters with respect to the THD

S. No.	LEVEL	THD
1	Three Level	31.70%
2	Seven Level	12.56%
3	Fifteen Level	4.99%

4 Conclusions

This paper has proposed a novel single phase fifteen level grid connected inverter for PV systems. The PV uses P&O MPPT algorithm for maximizing the energy to the inverter. Hybrid modulation scheme is adopted to reduce the switching losses of the proposed inverter.

The simulations are carried out in MATLAB/Simulink environment. The proposed inverter has upper and lower inverter. The upper inverter produces three level output voltage and lower inverter produces seven level output voltages. By cascading both these inverters produces fifteen level inverter. The proposed inverter has improved the output voltage of the inverter. The total harmonic distortion is also reduced to less than 5%.

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Appendix A: Calculation of duty cycle

Modelling of boost converter

The desired specification of the grid is 230 V (RMS) @ 50 Hz. Hence the proposed inverter also has to supply 230 V (RMS) @ 50 Hz. In the proposed inverter, the upper inverter is supplied from one PV module and the lower inverter is fed from six PV modules. So the total 230 V (RMS) has to be supplied by these seven modules. Thus the desired output of the upper boost converter is given by,

$$V_{DC} = \frac{V_m}{n}$$

$V_{m=}$ Peal Voltage

n = Number of PV panels

$$V_{DC} = \frac{230 * \sqrt{2}}{7} = 46.47$$

The desired output of the lower boost converter is given by,

$$V_{DC2} = (230 * \sqrt{2}) - 46.47$$

Modeling of upper boost converter

Since the upper DC/DC boost converter is connected one PV module, the input voltage (V_{in}) of the upper boost converter is approximately 35.8 Volts at 1kW/m^2 and 31.12 Volts at 200 W/m^2 (assuming that the minimum irradiance at the installed location). From the output (V_{out}) of the upper boost converter should be equal to 46.47 Volts. The relationship between input voltage and output voltage of boost converter in terms of duty cycle is given by,

$$V_{out} = \frac{V_{in}}{1-D}$$

So the maximum and minimum duty cycle is given by,

$$D_{\max} = 1 - \frac{V_{in}}{Vout} = 1 - \frac{31.12}{46.46}$$

$$D_{\min} = 1 - \frac{V_{in}}{Vout} = 1 - \frac{31.80}{46.47}$$

Limit of duty cycles is 0.23-0.33. The duty cycle is not fixed due to the tracking process of the maximum power point voltage. In the above expression the worst condition is the minimum input voltage condition, thus maximum and minimum duty cycle is taken into consideration for further designing.

Modeling of lower boost converter

Since the lower DC/DC boost converter is connected six PV modules in series, the input voltage ($V_{in\ (low)}$) of the lower boost converter is approximately 214.8 Volts at 1 kW/m^2 and 186.72 Volts at 200 W/m^2 (assuming that the minimum irradiance at the installed location). From the output $V_{out(low))}$ of the lower boost converter should be equal to 278.8 Volts.

$$D_{max} = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{186.72}{278} = 0.33$$

$$D_{out} = 1 - \frac{V_{in}}{V_{out}} = 1 - \frac{214.8}{278.8} = 0.23$$

Limit of duty cycles is 0.23-0.33. The duty cycle is not fixed due to the tracking process of the maximum power point voltage. In the above expression the worst condition is the minimum input voltage condition, thus maximum and minimum duty cycle is taken into consideration for further designing.

Appendix B: Modes of operation of proposed inverter

Mode 1: Switches S_{11} and S_{44} in the upper bridge and S_1 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates Vdc and lower inverter supplies the whole input voltage $6V_{dc}$. Hence resultant $7V_{dc}$ is appeared across the load.

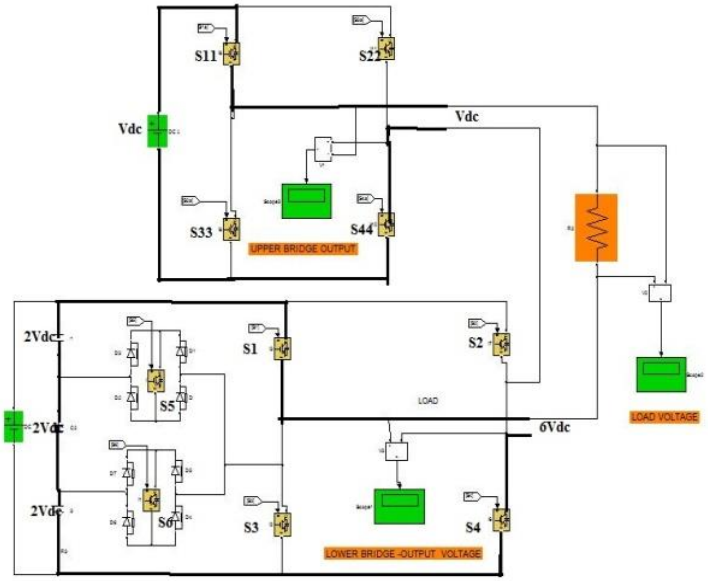

Figure a: Mode 1 operation of the proposed inverter

Mode 2: Switches S_{22} and S_{33} in the upper bridge and S_1 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 and lower inverter outputs $6V_{dc}$. Hence resultant $6V_{dc}$ is appeared across the load.

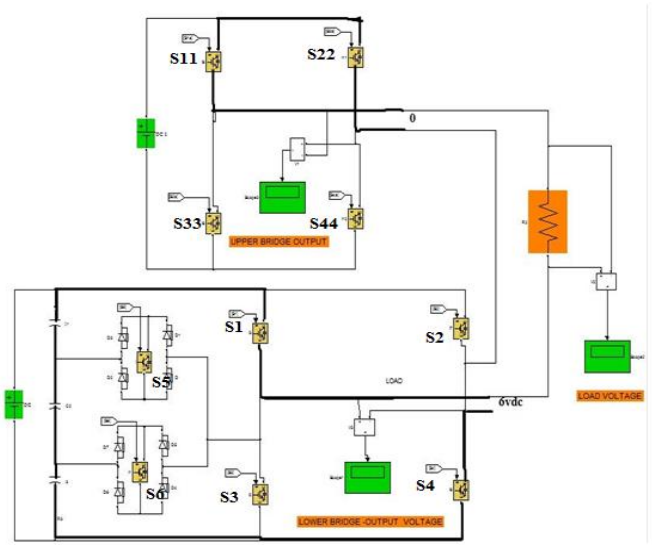

Figure b: Mode 2 operation of the proposed inverter

Mode 3: Switches S_{11} and S_{44} in the upper bridge and S_5 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates V_{dc} and lower inverter outputs $4V_{dc}$. Hence resultant $5V_{dc}$ is appeared across the load.

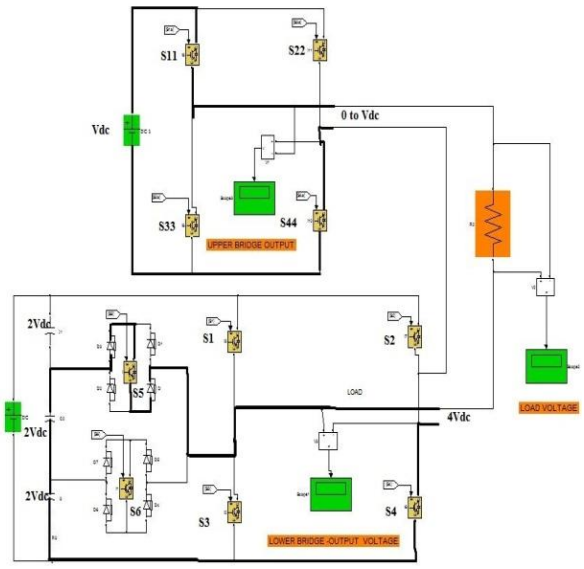

Figure c: Mode 3 operation of the proposed inverter

Mode 4: Switches S_{22} and S_{33} in the upper bridge and S_5 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 and lower inverter outputs $4V_{dc}$. Hence resultant $7V_{dc}$ is appeared across the load.

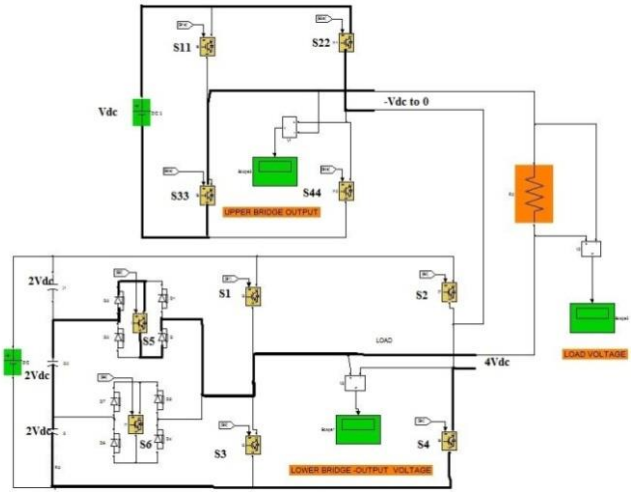

Figure d: Mode 4 operation of the proposed inverter

Mode 5: Switches S_{11} and S_{44} in the upper bridge and S_6 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates V_{dc} and lower inverter outputs $2V_{dc}$. Hence resultant $3V_{dc}$ is appeared across the load.

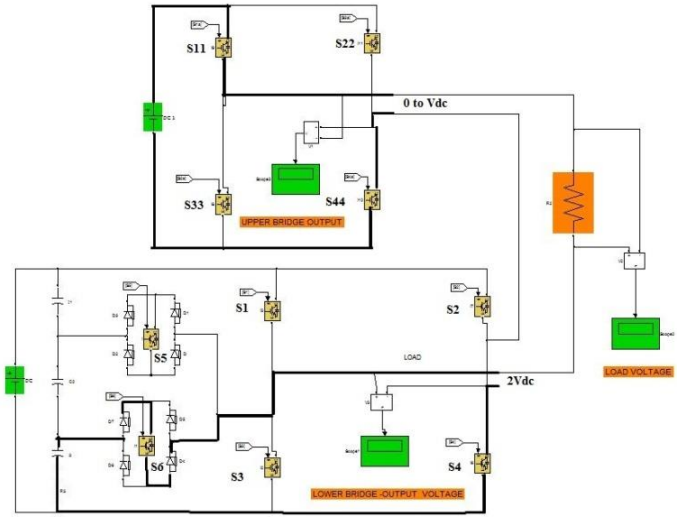

Figure e: Mode 5 operation of the proposed inverter

Mode 6: Switches S_{22} and S_{33} in the upper bridge and S_3 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates $-V_{dc}$ and lower inverter outputs $2V_{dc}$. Hence resultant V_{dc} is appeared across the load.

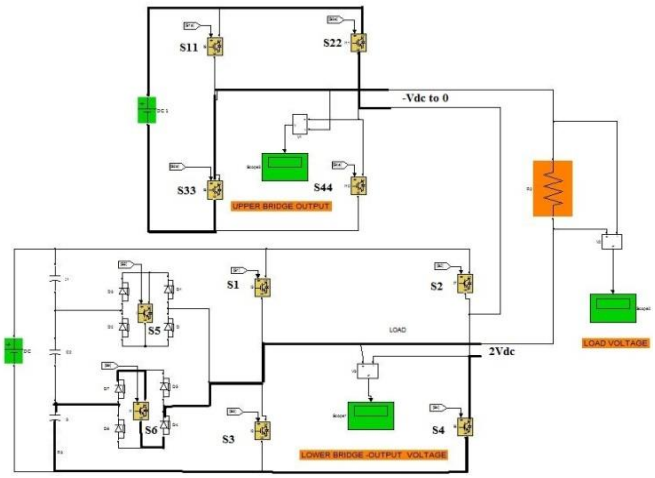

Figure f: Mode 6 operation of the proposed inverter

Mode 7: Switches S_{11} and S_{44} in the upper bridge and S_1 and S_2 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates V_{dc} volts and lower inverter outputs 0 volts. Hence resultant 0 is appeared across the load.

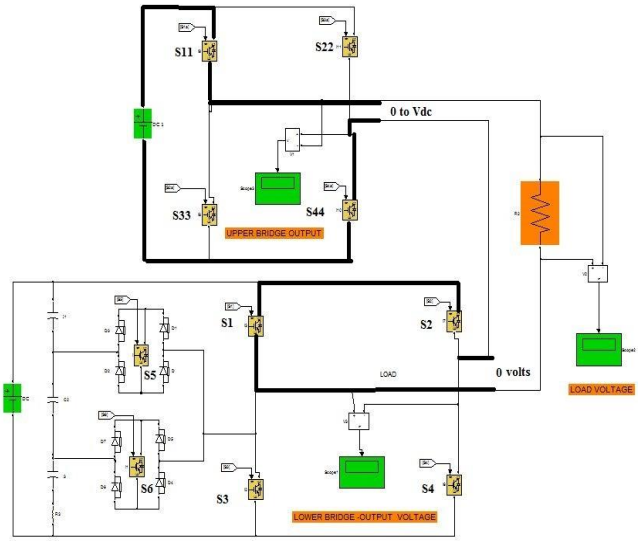

Figure g: Mode 7 operation of the proposed inverter

Mode 8: Switches S_{22} and S_{33} in the upper bridge and S_3 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates $-V_{dc}$ and lower inverter outputs 0. Hence resultant 0 is appeared across the load.

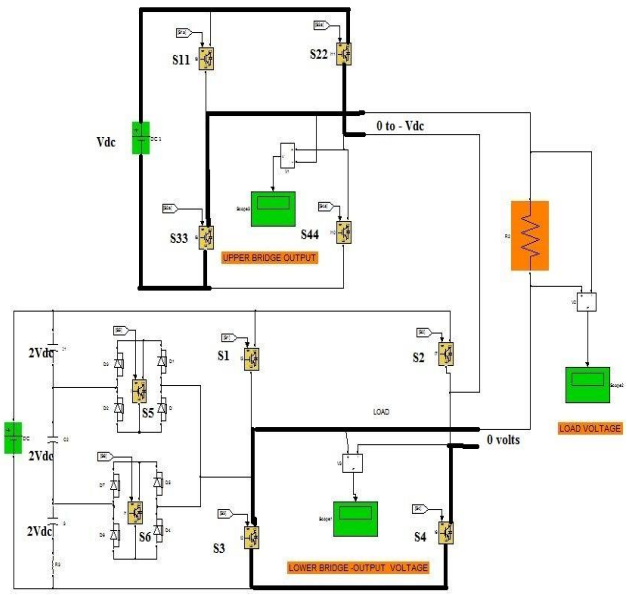

Figure h: Mode 8 operation of the proposed inverter

Mode 9: Switches S_{11} and S_{22} in the upper bridge and S_5 and S_2 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates V_{dc} and lower inverter outputs $-2V_{dc}$. Hence resultant $-V_{dc}$ is appeared across the load.

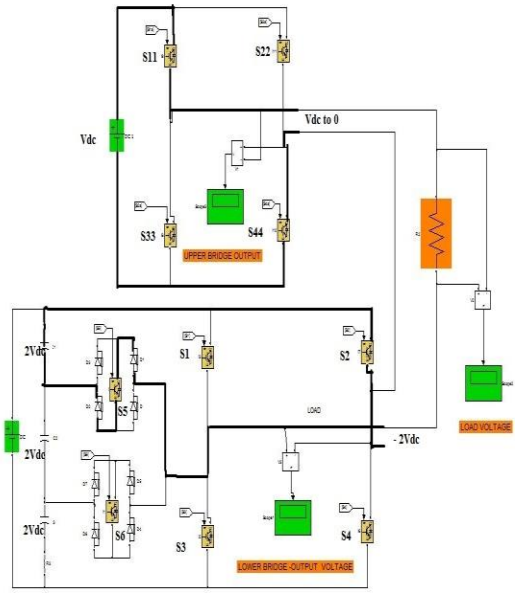

Figure i: Mode 9 operation of the proposed inverter

Mode 10: Switches S_{22} and S_{33} in the upper bridge and S_5 and S_4 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 and lower inverter outputs $-2V_{dc}$. Hence resultant $-2V_{dc}$ is appeared across the load.

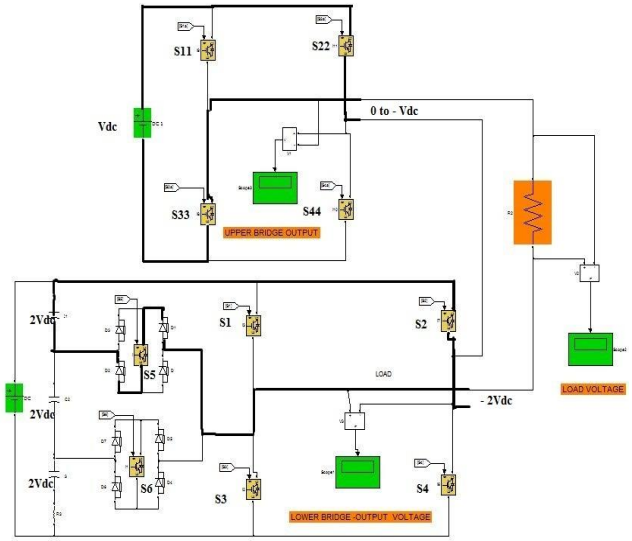

Figure j: Mode 10 operation of the proposed inverter

Mode 11: Switches S_{11} and S_{22} in the upper bridge and S_2 and S_6 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 and lower inverter outputs $-4V_{dc}$. Hence resultant $-4V_{dc}$ is appeared across the load.

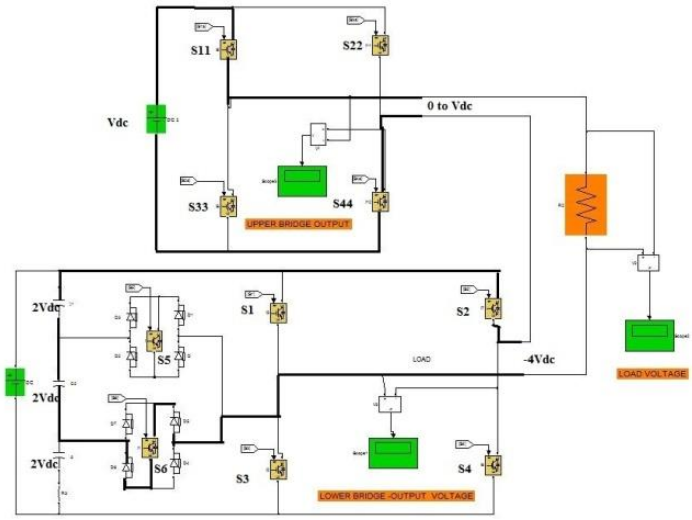

Figure k: Mode 11 operation of the proposed inverter

Mode 12: Switches S_{22} and S_{33} in the upper bridge and S_2 and S_6 in the lower bridge are turned ON; all other switches are in OFF state. Upper inverter generates 0 to $-V_{dc}$ and lower inverter supplies the whole input voltage $-4V_{dc}$. Hence resultant $-4V_{dc}$ to $-5V_{dc}$ is appeared across the load.

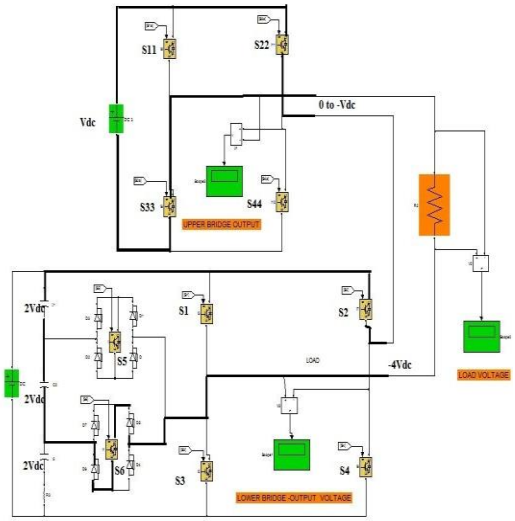

Figure l: Mode 12 operation of the proposed inverter

Mode 13: Switches S_{11} and S_{44} in the upper bridge and S_2 and S_3 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 to V_{dc} and lower inverter outputs $-6V_{dc}$. Hence resultant $-6V_{dc}$ to $-5V_{dc}$ is appeared across the load.

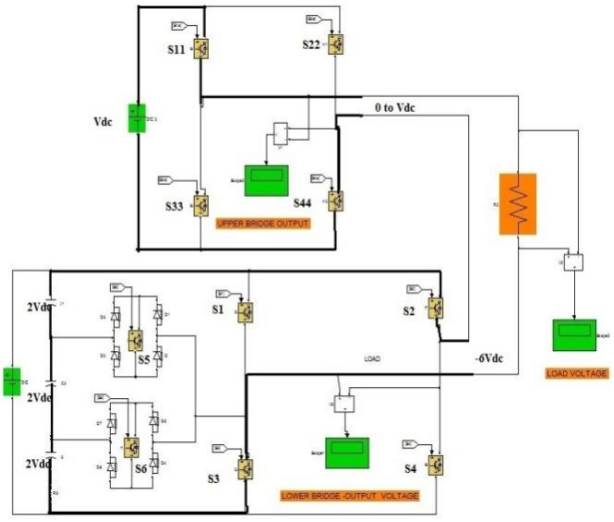

Figure m: Mode 13 operation of the proposed inverter

Mode 14: Switches S_{22} and S_{33} in the upper bridge and S_2 and S_3 in the lower bridge are turned ON, all other switches are in OFF state. Upper inverter generates 0 to $-V_{dc}$ and lower inverter outputs $-6V_{dc}$. Hence resultant $-6V_{dc}$ to $-7V_{dc}$ is appeared across the load.

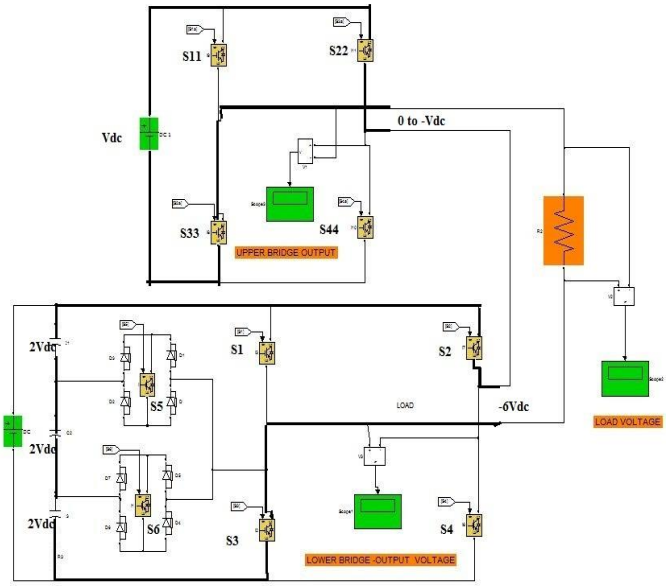

Figure n: Mode 14 operation of the proposed inverter

Appendix C: Switching sequence of proposed inverter

Switching combinations of the proposed inverter.

Upper H bridge switches (high frequency switches)				Lower H bridge switches (low frequency switches)						Mode	Output load voltage $V_{dc2} = V_{dc3} = V_{dc4} = 2V_{dc1}$		
MS_1	MS_2	MS_3	MS_4	MS_5	MS_6	MS_7	MS_8	AS_1	AS_2		V_{up}	V_{low}	$V_{total} = V_{up} + V_{low}$
ON	OFF	OFF	ON	ON	OFF	OFF	ON	OFF	OFF	I	$0 \leftrightarrow V_{dc1}$	$6V_{dc1}$	$6V_{dc1} \leftrightarrow 7V_{dc1}$
OFF	ON	ON	OFF	ON	OFF	OFF	ON	OFF	OFF	II	$-V_{dc1} \leftrightarrow 0$	$6V_{dc1}$	$5V_{dc1} \leftrightarrow 6V_{dc1}$
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	III	$0 \leftrightarrow V_{dc1}$	$4V_{dc1}$	$4V_{dc1} \leftrightarrow 5V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	IV	$-V_{dc1} \leftrightarrow 0$	$4V_{dc1}$	$3V_{dc1} \leftrightarrow 4V_{dc1}$
ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	ON	V	$0 \leftrightarrow V_{dc1}$	$2V_{dc1}$	$2V_{dc1} \leftrightarrow 3V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	ON	VI	$-V_{dc1} \leftrightarrow 0$	$2V_{dc1}$	$V_{dc1} \leftrightarrow 2V_{dc1}$
ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	VII	$0 \leftrightarrow V_{dc1}$	0	$0 \leftrightarrow V_{dc1}$
OFF	ON	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	VIII	$0 \leftrightarrow -V_{dc1}$	0	
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	ON	OFF	IX	$V_{dc1} \leftrightarrow 0$	$-2V_{dc1}$	$-V_{dc1} \leftrightarrow -2V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	X	$0 \leftrightarrow -V_{dc1}$	$-2V_{dc1}$	$-2V_{dc1} \leftrightarrow -3V_{dc1}$
ON	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	ON	XI	$V_{dc1} \leftrightarrow 0$	$-4V_{dc1}$	$-3V_{dc1} \leftrightarrow -4V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	XII	$0 \leftrightarrow -V_{dc1}$	$-4V_{dc1}$	$-4V_{dc1} \leftrightarrow -5V_{dc1}$
ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	XIII	$V_{dc1} \leftrightarrow 0$	$-6V_{dc1}$	$-5V_{dc1} \leftrightarrow -6V_{dc1}$
OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	XIV	$0 \leftrightarrow -V_{dc1o}$	$-6V_{dc1}$	$-6V_{dc1} \leftrightarrow -7V_{dc1}$

Figure o: Switching sequence of the propose inverter

Appendix D: Tabulation of different parameters and credentials involved in the design of the system

Table a: Inverter design parameters

Inverter Type	**H Bridge**	**Modified H Bridge**
Main Switches	6(N-1)	3((N-1) +4)
Main Diodes	6(N-1)	3((N-1) +4)
Clamping Diodes	0	0
DC Bus Capacitors	3(N-1)/2	3(N-1)/2
Flying Capacitors	0	0